

		Zynq™-7000 Extensible Processing Platform				
		Z-7010	Z-7020	Z-7030	Z-7045	
		Device Name	Z-7010	Z-7020	Z-7030	Z-7045
		Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™				
	Processor Extensions	NEON™ & Single / Double Precision Floating Point				
	Maximum Frequency	800 MHz				
	L1 Cache	32 KB Instruction, 32 KB Data per processor				
	L2 Cache	512 KB				
	On-Chip Memory	256 KB				
	External Memory Support	DDR3, DDR2 LPDDR2				
	External Static Memory Support	2x Quad-SPI, NAND, NOR				
	DMA Channels	8 (4 dedicated to Programmable Logic)				
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Security	AES and SHA 256b for secure boot				
	Peripherals and Static Memory Multiplexed I/O <sup>(1)</sup>		54			
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)		2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts				
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGAs	Artix™-7 FPGAs	Kintex™-7 FPGAs	Kintex™-7 FPGAs	
	Programmable Logic Cells (Approximate ASIC Gates <sup>(3)</sup> )	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)	
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)	
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900	
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS	
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8	
	Agile Mixed Signal (AMS) / XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs				
	Security	AES and SHA 256b for secure configuration				
	Multi-Standards 3.3V I/O <sup>(2)</sup>	100	200	100	200	
	Multi-Standards High Performance 1.8V I/O <sup>(2)</sup>	—	—	150	150	
Serial Transceivers <sup>(2)</sup>	—	—	4	16		

- Notes: 1. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. A designer can use the Programmable Logic I/Os.  
 2. Total Number of I/O and Transceivers depends on package used.  
 3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.  
 4. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information

*Important: Product table subject to change*