



Xilinx® 7 Series FPGA Power Benchmark Design Summary

March, 2012

Application-centric Benchmarking Process



100G Packet Processor



OTN Muxponder



ASIC Emulation



Wireless Radio



Edge QAM



AVB Switcher



Military Radio



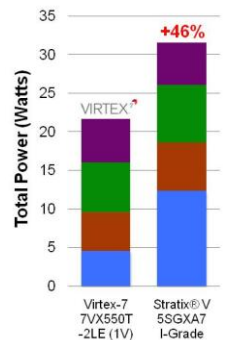
Beamformer (128 ch)

FPGA resource counts, toggle rates, clock speeds...

- **Xilinx XPower Estimator (XPE) version 13.4**
- **MAX condition used to estimate worst-case static power**



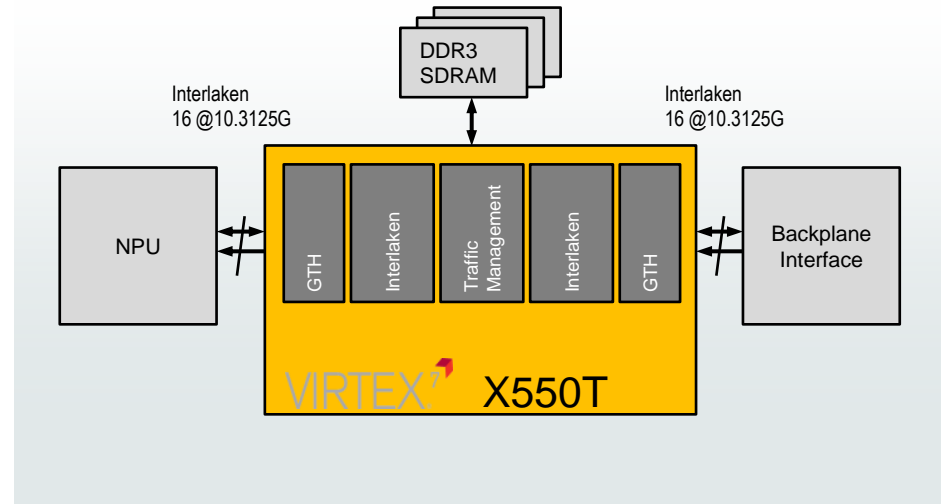
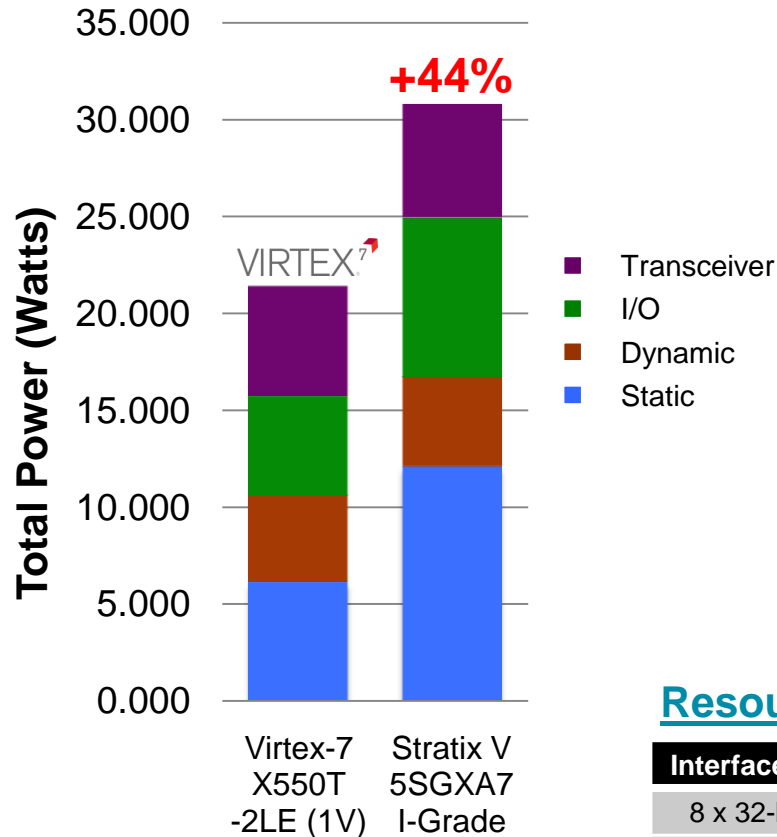
- **Early Power Estimator (EPE) version 11.1 SP2 B6**
- **MAX condition used to estimate worst-case static power**



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Traffic Manager in 100G Line Card

Virtex®-7 X550T



Resources

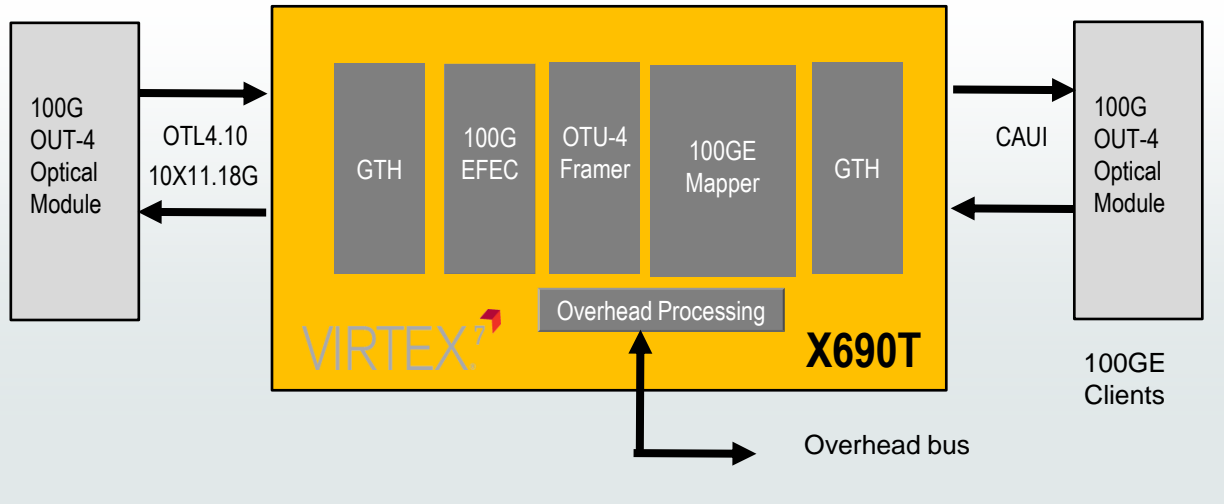
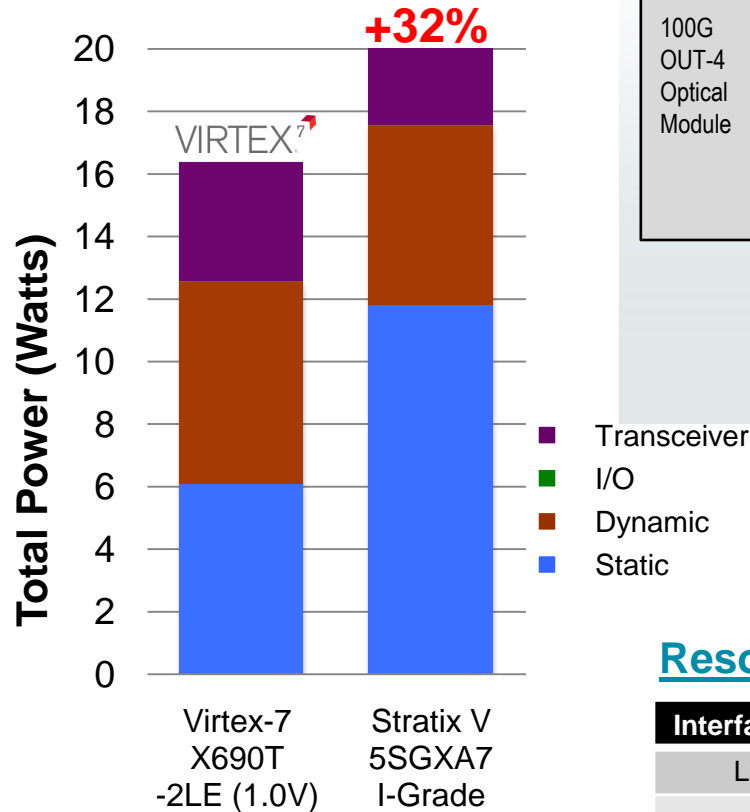
Interface	I/Os	GTs	Rate
8 x 32-bit DDR3	544	-	1600 Mbps
Interlaken	-	32	10.3 Gbps

Environment	Process
T _j =100C	Max
LC/LEs	232K
Flip Flops	167K
Block RAM	15516 Kb
DSP Blocks	2
PLLs	8
Core Freq.	250 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

100GE over OTU4 Transponder

Virtex-7 X690T



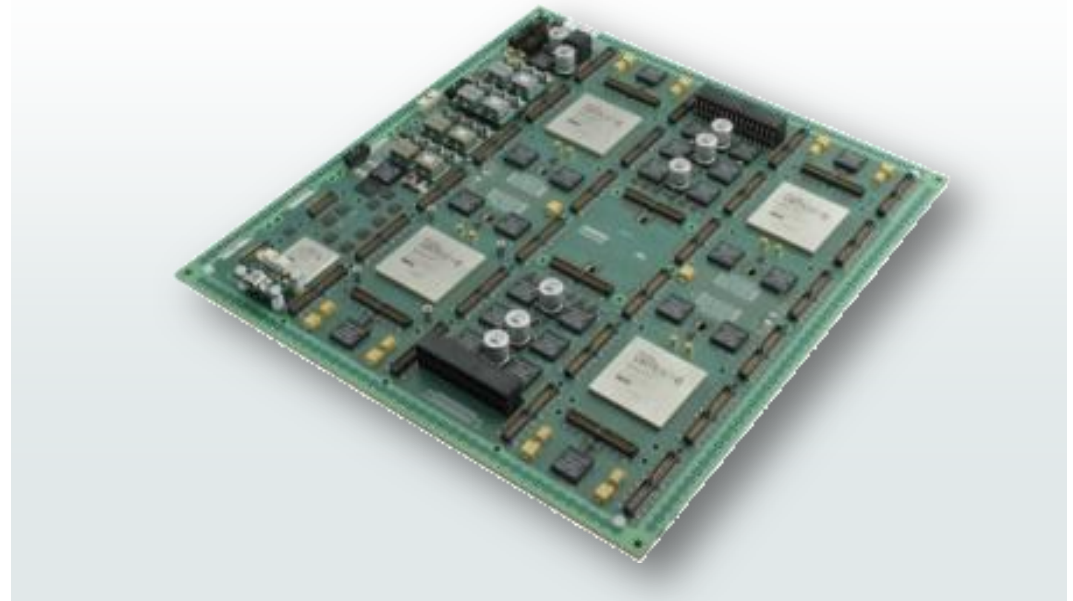
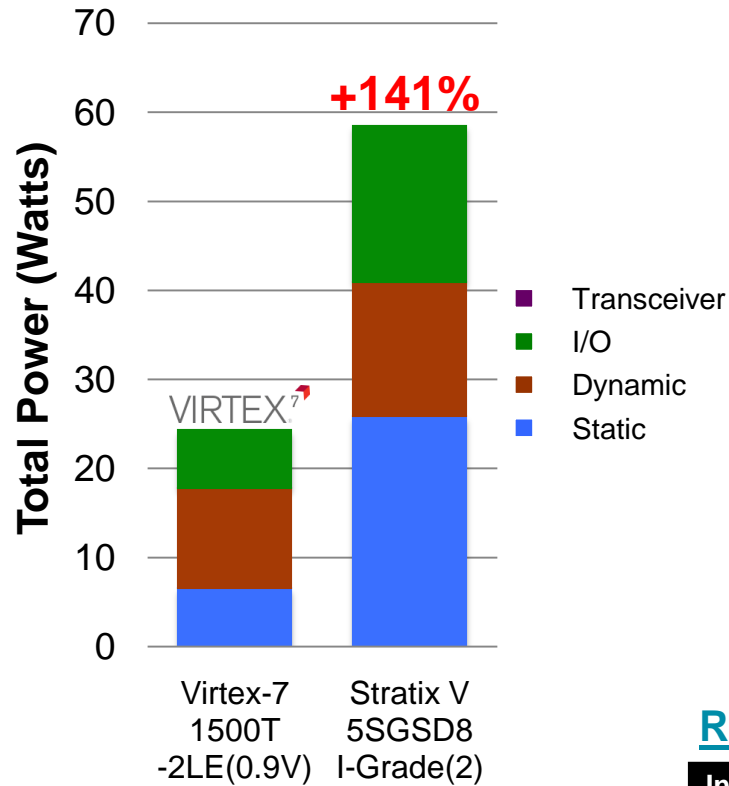
Resources

Interface	I/Os	GTs	Rate
LVC MOS	50	-	250 Mbps
GT	-	10	11.1 Gbps
GT	-	10	10.3 Gbps

Environment	Process
Tj=100C	Max
LC / LEs	392K
Flip Flops	245K
Block RAM	9,360Kb
Core Freq.	350, 175MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

ASIC Prototyping Virtex-7 1500T



Resources

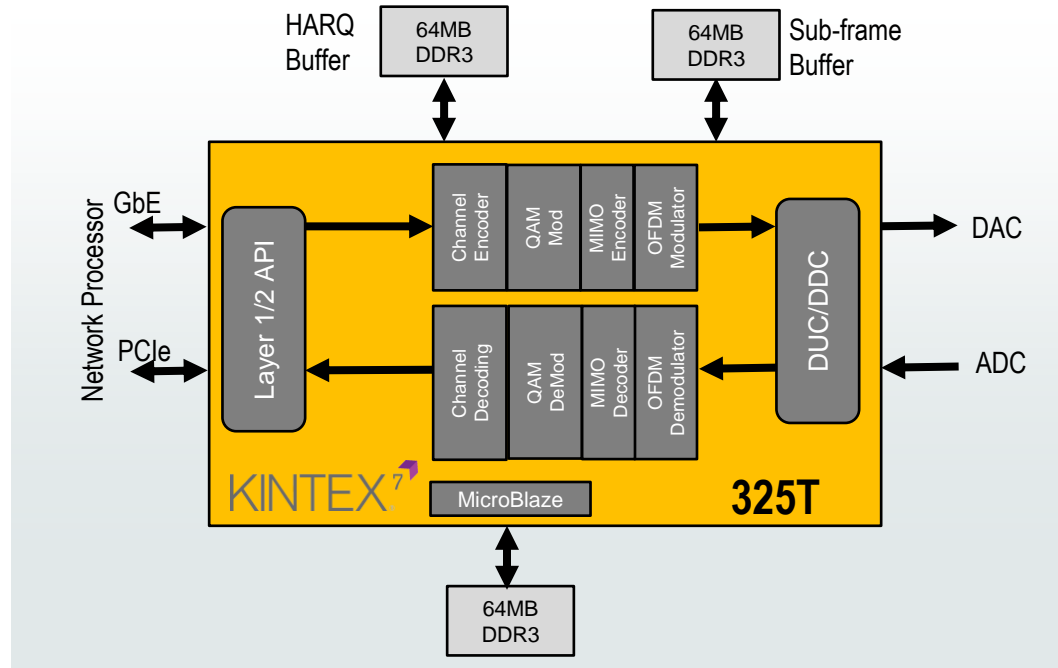
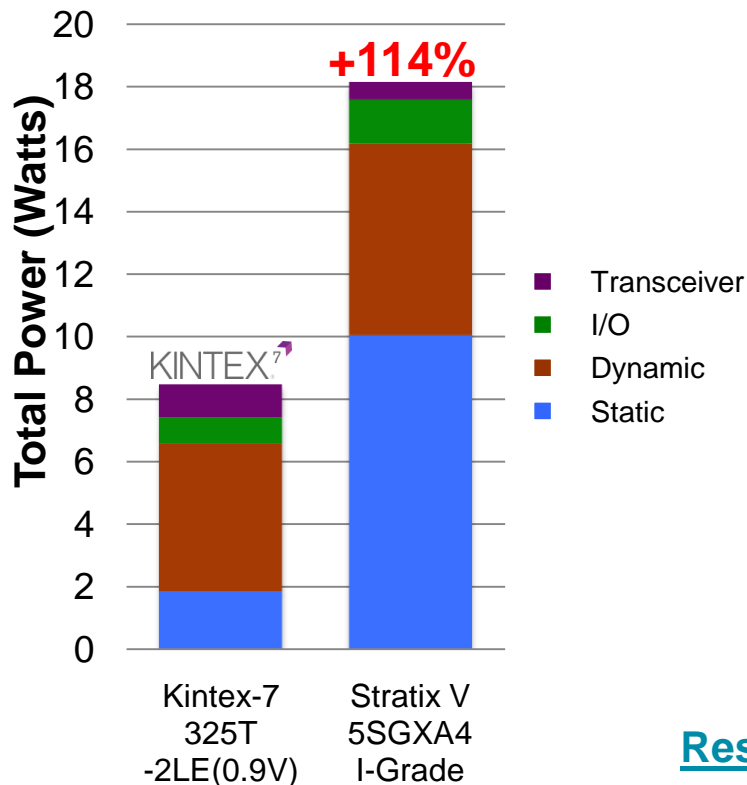
Interface	I/Os	GTs	Rate
3 64-bit DDR3	366	-	1066 Mbps
LVDS	408	-	1000 Mbps

Environment	Process
Tj=100C	Max
LC / LEs	1,224K
Flip Flops	765 K
Block RAM	21,600 Kb
Core Freq.	200 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

Wireless WCDMA/LTE Picocell Layer 1

Kintex™-7 325T



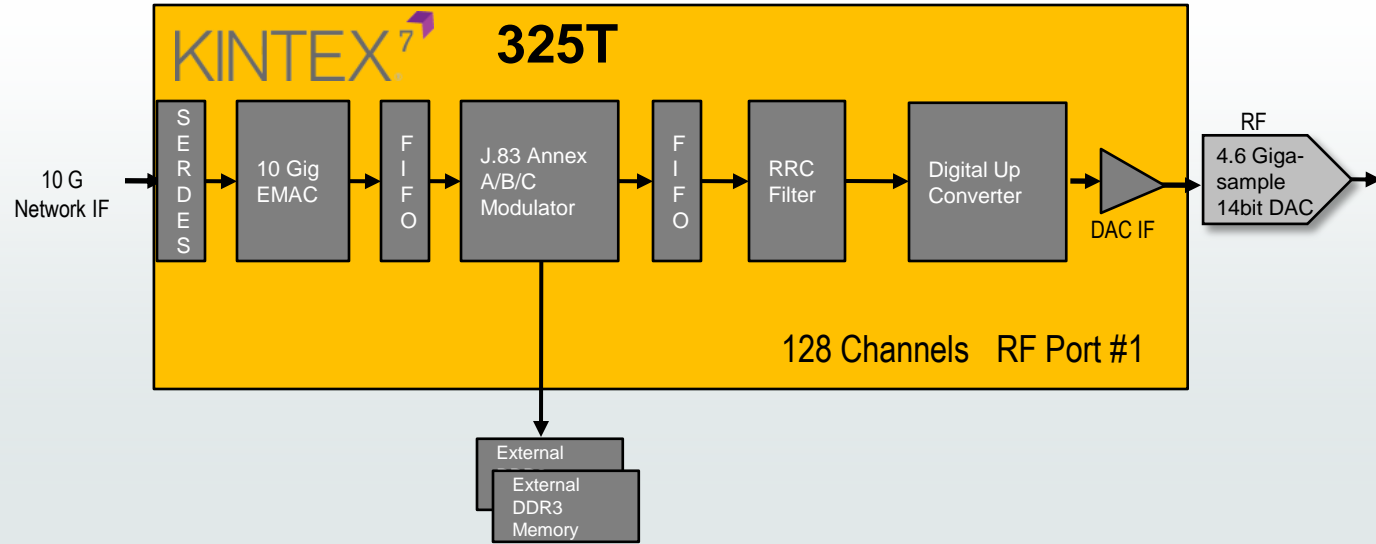
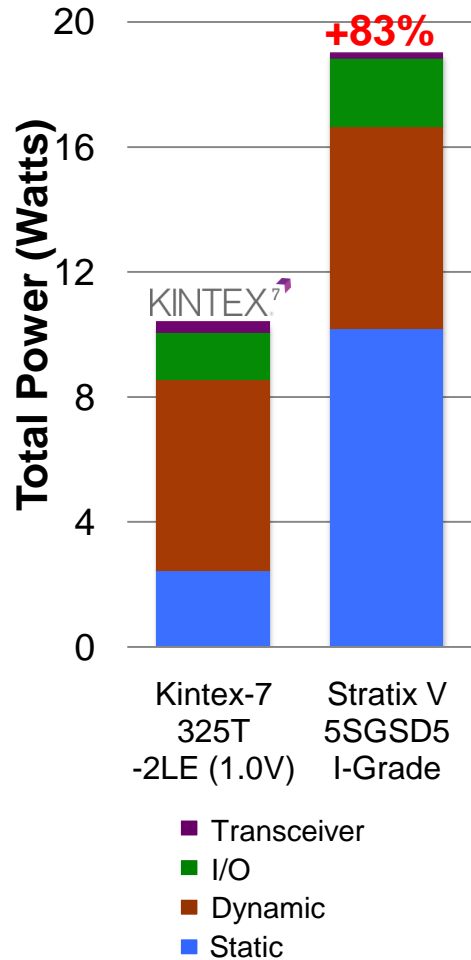
Resources

Interface	I/Os	GTs	Rate
3 x 16-bit DDR3	129	-	1066 Mbps
GT	-	2	4.0 Gbps
GT	-	1	1.25 Gbps
GT	-	1	2.5 Gbps

Environment	Process
T _j =100C	Max
LC / LEs	240K
Flip Flops	150K
Block RAM	14,562 Kb
DSP Blocks	342
PCle Blocks	1
Core Freq.	307.2 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

Dense Edge QAM Modulator Kintex-7 325T



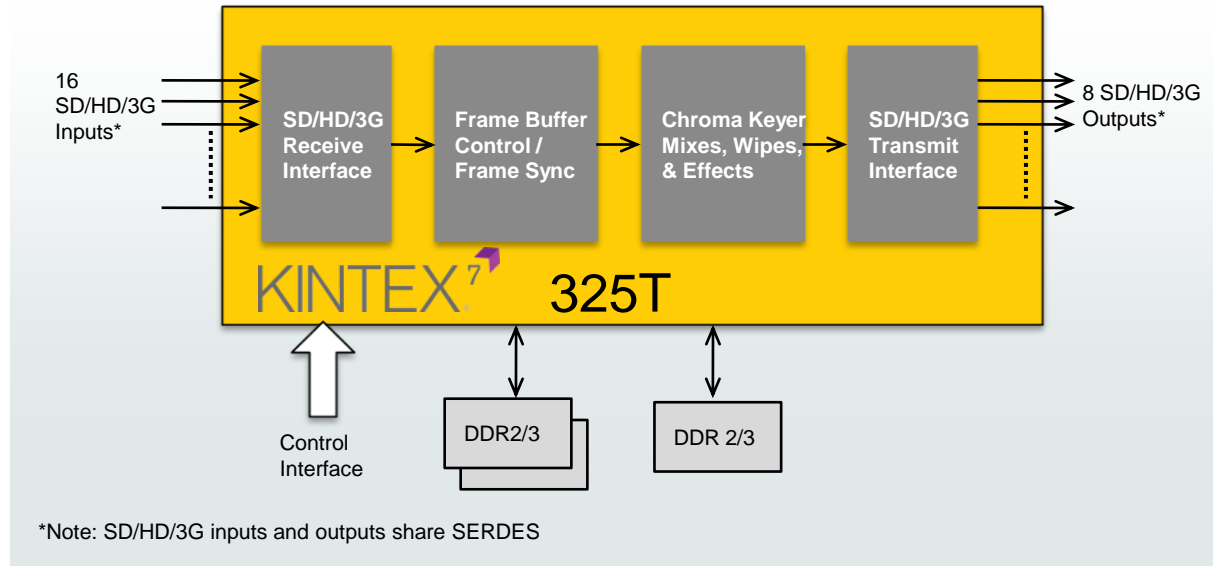
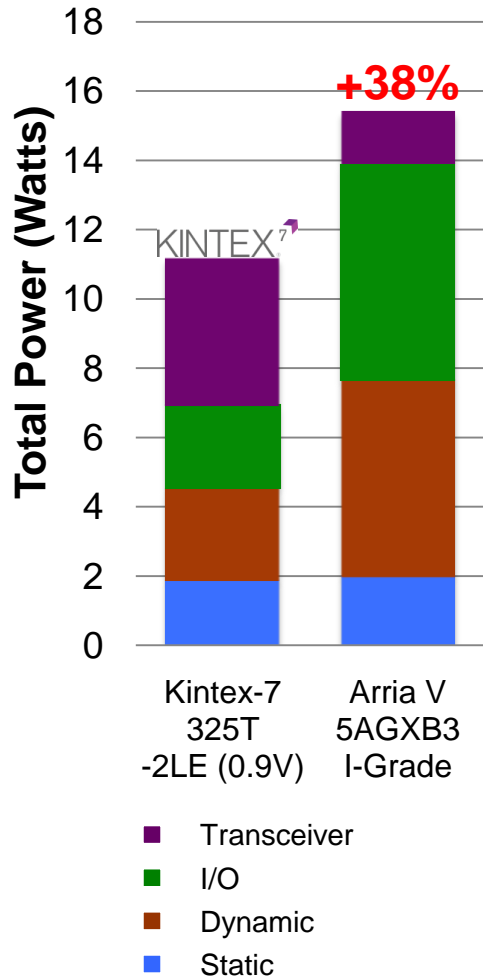
Resources

Interface	I/Os	GTs	Rate
LVDS	124	-	1152 Mbps
LVC MOS	12	-	15MHz
2x 8-bit DDR3	55	-	800 Mbps
GT	-	1	10.3 Gbps

Environment	Process
T _j =100C	Max
LC / LEs	182K
Flip Flops	157K
Block RAM	12,402 Kb
DSP Blocks	641
Core Freq.	384, 576, 156, 192, 200 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

AVB Switcher Kintex-7 325T



Resources

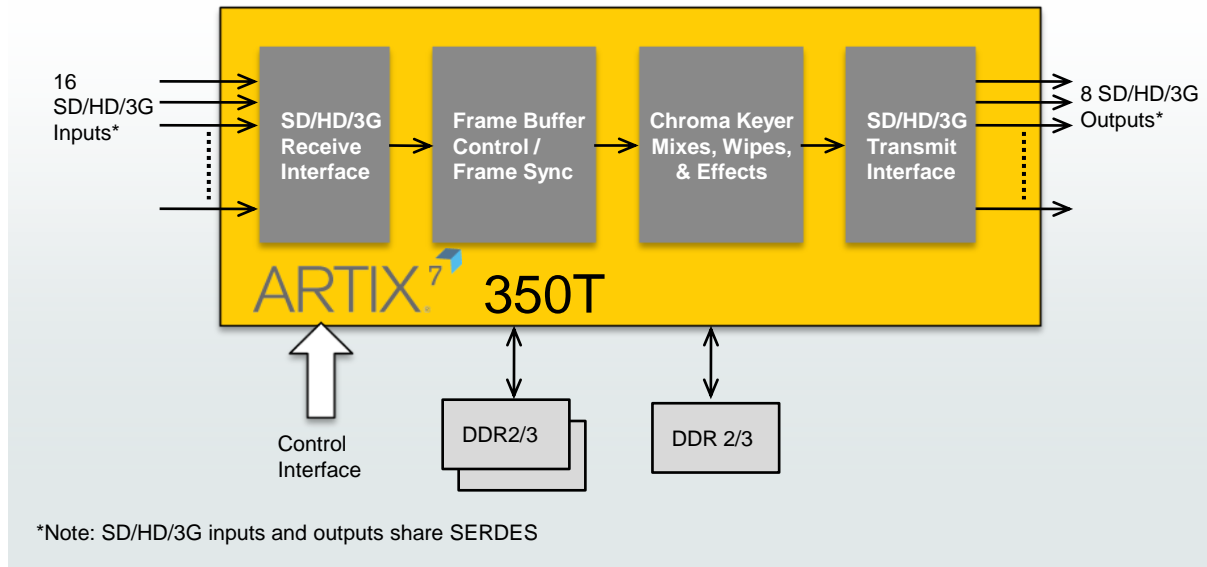
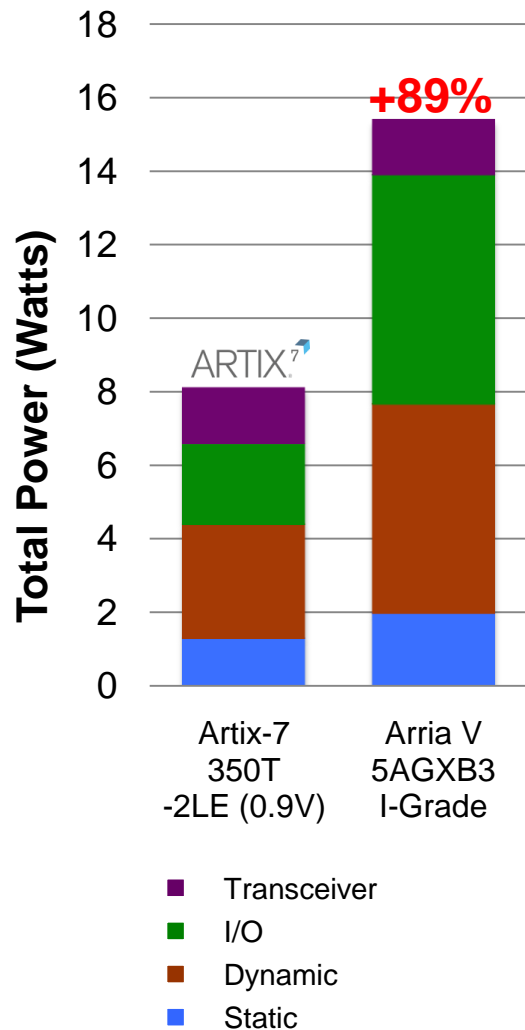
Interface	I/Os	GTs	Rate
3 x 72-bit DDR3	450	-	800 Mbps
GT	-	16	2.97 Gbps

Environment	Process
T _j =100C	Max
LC / LEs	300K
Flip Flops	188K
Block RAM	10,800 Kb
DSP Blocks	500
Core Freq.	148.5MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

AVB Switcher

Artix™-7 350T



Resources

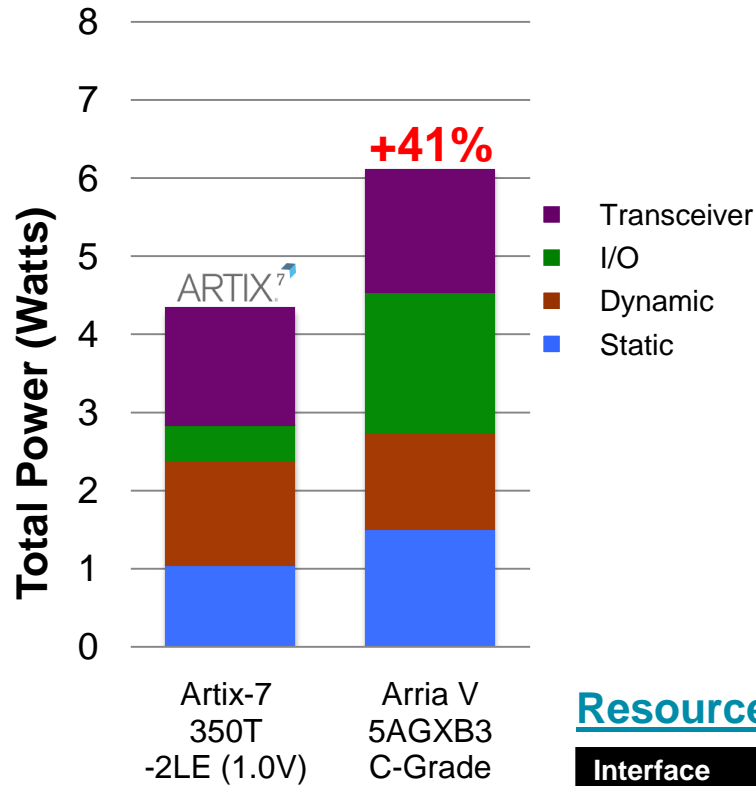
Interface	I/Os	GTs	Rate
3 x 72-bit DDR3	450	-	800 Mbps
GT	-	16	2.97 Gbps

Environment	Process
T _j =100C	Max
LC / LEs	300K
Flip Flops	188K
Block RAM	10,800 Kb
DSP Blocks	500
Core Freq.	148.5MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

Military Network Protocol Platform Data Aggregator

Artix-7 350T



Resources

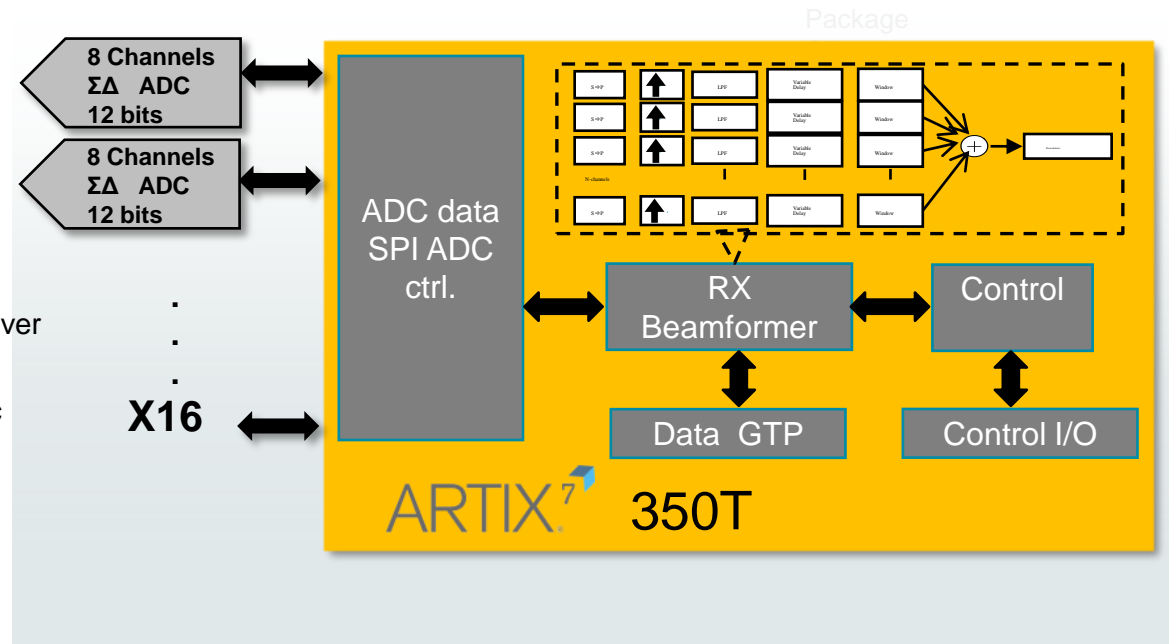
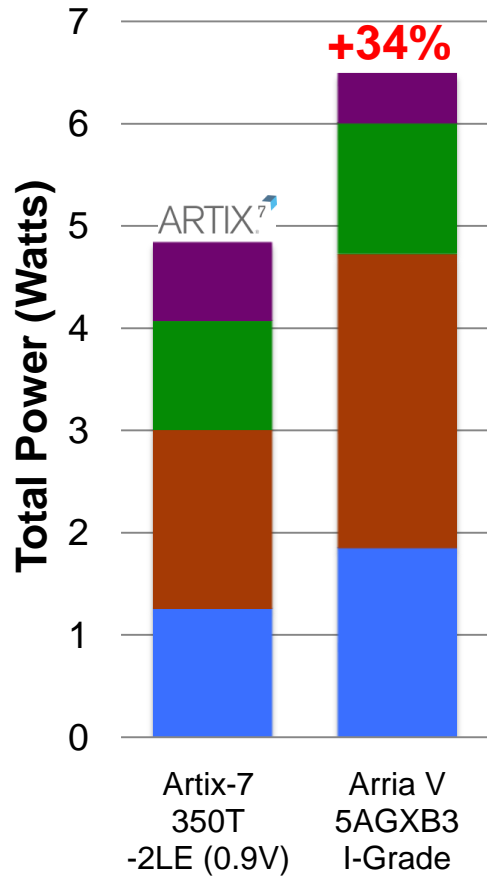
Interface	I/Os	GTs	Rate
2x 36-bit RLDRAMs	122	-	520 Mbps
GT	-	6	5 Gbps
GT	-	8	2.5 Gbps
GT	-	1	2.5 Gbps

Environment	Process
Tj=85C	Max
LC / LEs	63K
Flip Flops	58K
Block RAM	16,020 Kb
DSP Blocks	400
PCIe Blocks	1
Core Freq.	125 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6

Portable Ultrasound 128 CH Beamformer Rx Module

Artix-7 350T



Resources

Interface	I/Os	GTs	Rate
LVDS	288	-	250 Mbps
LVC MOS	48	-	125 Mbps
LVC MOS	256	-	40 Mbps
GT	-	6	3.125 Gbps
GT	-	2	2.5 Gbps

Environment	Process
T _j =100C	Max
LC / LEs	158K
Flip Flops	114K
Block RAM	3,744 Kb
DSP Blocks	226
PCIe Blocks	2
Core Freq.	40, 160 MHz

*Design results sourced from Xilinx XPower Estimator (XPE) version 13.4 and Altera Early Power Estimator (EPE) version 11.1 SP2 B6