Technical Viability of Stacked Silicon Interconnect Technology

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TECHNICAL VIABILITY OF STACKED SILICON INTERCONNECT TECHNOLOGY

1. Summary Conclusions

Xilinx has addressed the key need for early delivery of high-capacity FPGA products in 28nm by the following actions:

- Leveraging the repetitive structures of FPGAs, Xilinx has created partitions and combines them by N-number in order to create a single product that enables higher-yielding characteristics, earlier in the process node life cycle, compared to using one large-area product.
- Use of high-reliability microbumps that are used to connect the silicon die to a silicon interposer.
- Use of TSV technologies and high-density interconnects that have been proven in high-volume production to give an interposer that enables low-latency chip-to-chip communication and flip-chip packaging.
- Use of large area standard solder bumps that provide high-reliability connectivity from the interposer to the next-level.

The Stacked Silicon Interconnect Technology is ready for high-volume production enabling FPGA products that have high reliability and are high-capacity at 28nm. Xilinx has combined a number of proven high-volume technologies to provide a highly innovative solution to the system needs for high-capacity FPGAs.

2. Statement of Challenges

Xilinx's Virtex-7 products will have up to 2.0M usable logic gates, with power per gate reduction of 50% compared to the Virtex-6 family. The Virtex-7 family will also support high-speed SERDES, including rates up to 28Gbps and a large number of DSP blocks.

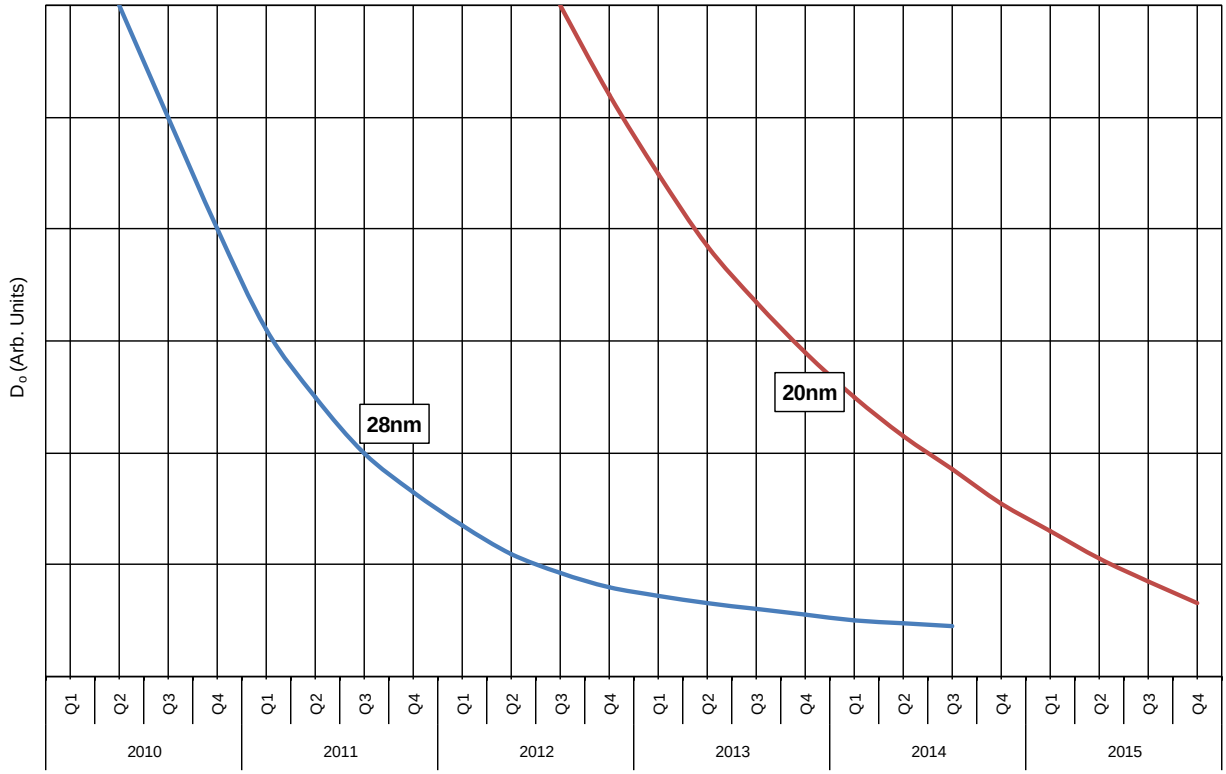
The higher-capacity FPGA products have the potential to become the core of the system design rather than being a support random-gate capability. There are, consequently, major benefits to customers to implement the new generation of products in a range of system types and application segments.

One key problem area that needs to be addressed is the low yields of the very large-area products in a new technology node. While yields increase over time when defect density levels are reduced, this time frame can be 18 to 24 months.

A perspective on the reduction in defect density for 28nm and 20nm technology is shown in the following figure.

FIGURE 1

Defect Density Levels for 28nm and 20nm Technology



IBS, Inc., "Technical Viability of Stacked Silicon Interconnect Technology", October 2010

The defect density levels decline relatively rapidly for a new technology, but it can take 18 or 24 months to give high yields for the large-area die. The approach Xilinx is taking uses the repetitive structure of FPGA products to create N-number of smaller die, where N could be 2, 4, or more, and are assembled in such a way as to have the same characteristics as one large die.

This overcomes the problem of packaging N-number of die in separate packages that result in interconnect delays going from chip to the package to the board and then back to the package and to the die can result in both higher power consumption and long delays in addition to the associated latencies.

By using the smaller die, there is the ability to ramp the wafer volumes rapidly without incurring the yield penalties associated with the large die.

As the defect density levels are reduced, there will be a reduction in the net yield differences between the multi-die and single-die solutions. However, the performance advantages from using the smaller die will remain.

High-capacity FPGAs on the large die have long interconnect lengths, and with the tight pitch of the interconnect structures at 28nm, any small variation in the physical parameters can have a large impact on the delays of the critical paths. As the technology matures, the wafer vendors such as TSMC, will reduce the variations of these delays.

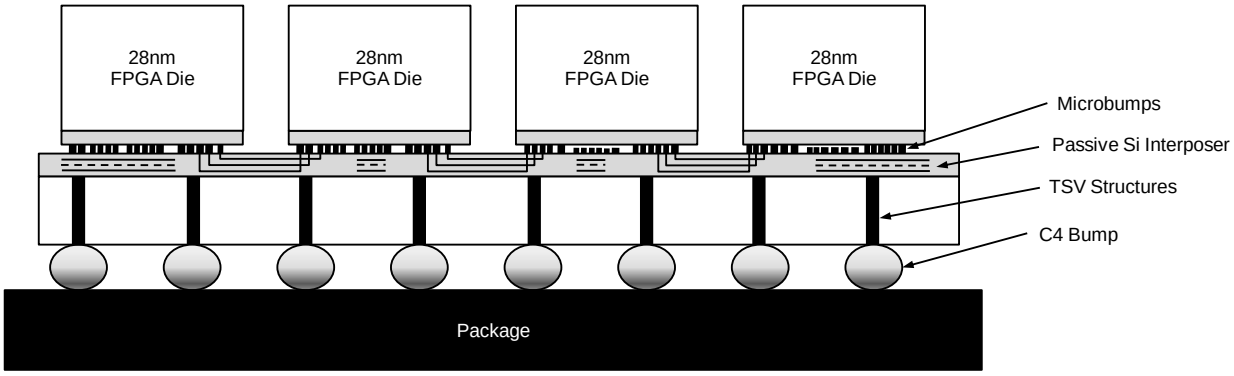
A key challenge, consequently, is how to use the multi-die approach and have low interconnect delays at an early stage of the availability of the new technology node.

3. Solution of Xilinx

The approach that Xilinx has taken to address the challenges of ramping up high-capacity FPGAs in 28nm technology is shown in the following figure.

FIGURE 2

Xilinx Stacked Silicon Interconnect Technology



The Xilinx solution uses a TSV-based silicon interposer, which is based on technology that has been proven in high-volume applications such as image sensors and power amplifiers. The interposer supports long interconnect structures that exhibit low delays and operate as an extension of the on-chip connectivity structures. This allows the use of an N-die solution, which can have performance levels approaching 400MHz. The multi-die package is similar to that of the monolithic solution allowing this to be an option once defect levels have reached maturity.

The FPGA die are connected to the silicon interposer with microballs, which support high pin count levels and high reliability. Because the thermal connectivity of the die and interposer are similar, thermal stress is low.

The interposer is connected to the next-layer carriers with C4 technology initially developed by IBM for its high-performance, high-reliability computer systems. The large solder balls are able to absorb the thermal stress between the silicon substrate and next-level carrier.

The multi-layer structures use technologies that are mature and are used in high-volume production for a range of high-volume products. Combining the different proven technologies is, however, innovative and a low-risk method to ramp up unit volumes of high-capacity FPGA products in 28nm technology.

While the current approach is to assemble four FPGA die on the interposer with similar characteristics and equivalent gate count as the fully integrated design, the Stacked Silicon Interconnect Technology also allows the assembly of FPGA die with different characteristics, i.e. SERDES, high-density CAM structures, processor engines, etc.

There is also the ability to develop programmable ASSP products, which could have two or three ASSP die and one or two FPGA die. There is also the potential to mix multiple process technology nodes for the building block functions that are assembled on the interposer.

While there can be the need to modify the FPGA architectures to support the application-specific platform solutions, this approach is much more cost-effective than designing a full ASSP or standard cell ASIC design.

Xilinx technologies provide both short-term as well as long-term benefits at the 28nm technology node, with the ability to continue to use the concepts at 20nm and smaller feature dimensions.

Xilinx is taking a systematic and low-risk approach to the implementation of multi-die manufacturing, which offers lower risk to the end customer. There is the ability to provide access to high gate count FPGA products that are also high-performance and power consumption-competitive.

Each part of the Stacked Silicon Interconnect Technology is already in high-volume production, and as a result, the technology, manufacturability, and reliability risks are low.

4. Application Leverage Potential

The analysis of the applications shows that a wide range of systems can utilize the technology. There is the ability to obtain portions of the standard cell ASIC and application-specific standard product marketshare. There is also the expansion of the legacy FPGA market by allowing enhancements to the functionality of the systems.

A perspective on the market for the hardware customization approaches is shown in the following table.

TABLE 1

Market for Standard Cell ASICs, ASSPs, and Programmable Logic

	2009	2010	2011	2012	2013	2014	2015
Standard cell ASICs ($M)	6,984	7,994	8,682	9,291	9,315	10,121	10,884
• Growth rate (%)	NA	14.5	8.6	7.0	0.3	8.7	7.5
• Percent subtotal (%)	12.67	11.69	11.62	11.28	11.64	11.28	10.95
Special-purpose logic ($M)	44,824	55,908	61,018	67,431	64,788	72,983	81,143
• Growth rate (%)	NA	24.7	9.1	10.5	(3.9)	12.7	11.2
• Percent subtotal (%)	81.35	81.74	81.66	81.88	80.97	81.35	81.65
Programmable logic ($M)	3,295	4,492	5,020	5,629	5,908	6,616	7,357
• Growth rate (%)	NA	36.3	11.8	12.1	5.0	12.0	11.2
• Percent subtotal (%)	5.98	6.57	6.72	6.84	7.38	7.37	7.40
Subtotal ($M)	55,103	68,394	74,720	82,351	80,011	89,720	99,384
• Growth rate (%)	NA	24.1	9.2	10.2	(2.8)	12.1	10.8

IBS, Inc., "System IC Market Trends" (Q2/2010 Global System IC Industry Service), August 2010

The analysis of the market for hardware customization shows growth, but with growth being constrained by the limitations of each design approach, i.e., standard cell ASICs have very high design costs, where the customer may wait 12 months to get prototypes.

The programmable logic market, however, has higher growth than the total IC market through 2015 because of the steady enhancements in the complexity and functionality of FPGA solutions. There is a slowing in growth in 2013 due to the expectation of a decline in the total semiconductor market because of the global economic environment.

The adoption of the Xilinx Stacked Silicon Interconnect Technology allows a portion of the standard cell ASIC and ASSP market to be obtained and the quantification of this value as well as the increase in the growth of the FPGA market are shown in the following table.

TABLE 2

Market Perspective (New Technology)

	2009	2010	2011	2012	2013	2014	2015
Standard cell ASIC penetration of SSIT ($M)	0	0	0	111	335	617	1,132
• Growth rate (%)	NA	NA	NA	NA	200.8	84.1	83.3
• Percent standard cell ASICs (%)	0.0	0.0	0.0	1.2	3.6	6.1	10.4
Special-purpose logic penetration of SSIT ($M)	0	0	0	135	454	949	1,623
• Growth rate (%)	NA	NA	NA	NA	236.3	109.2	71.0
• Percent special-purpose logic (%)	0.0	0.0	0.0	0.2	0.7	1.3	2.0
Additional contribution to programmable logic market ($M)	0	0	0	90	148	377	677
• Growth rate (%)	NA	NA	NA	NA	64.0	155.3	79.5
• Percent programmable logic (%)	0.0	0.0	0.0	1.6	2.5	5.7	9.2
Existing programmable logic market ($M)	3,295	4,492	5,020	5,629	5,908	6,616	7,357
• Growth rate (%)	NA	36.3	11.8	12.1	5.0	12.0	11.2
• Percentage new programmable logic market (%)	100.0	100.0	100.0	94.4	86.3	77.3	68.2
∆ Potential ($M)	0	0	0	336	937	1,943	3,432
• Growth rate (%)	NA	NA	NA	NA	178.4	107.5	76.6
New potential programmable logic market ($M)	3,295	4,492	5,020	5,965	6,845	8,559	10,789
• Growth rate (%)	NA	36.3	11.8	18.8	14.7	25.1	26.0

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The potential increase in the FPGA market obtained from adopting the new technologies of Xilinx in 2015 is $3,432M (this is in addition to the legacy FPGA market). Consequently, in addition to the short-term impact of the rapid adoption of high-gate count FPGA products in 28nm, there are also long-term financial benefits. The long-term benefits provide a strategic perspective on the value of the new technologies.

If Xilinx decides to assemble different IC blocks in addition to the partitioned FPGA functions and provide application solutions, the upside potential is even larger than the level shown. Also, if Xilinx implements ultra high-capacity FPGA products (will need large interposer), there is additional upside potential.

5. Conclusion

The new technology concepts of Xilinx are very innovative and use technologies that have been proven in high-volume production, which gives low risks and can provide good benefits to customers as well as good financial returns to Xilinx.

The benefits include the following:

- Fast time-to-market for high-capacity FPGAs at 28nm, with the expectation that a similar pattern can occur at 20nm and smaller feature dimensions. The performance and reliability levels of the Stacked Silicon Interconnect Technology structures are comparable to integrated designs and allow a seamless interface for customers to adopt integrated products when they become cost-effective.

- There is the ability to mix hardware functionality as part of the multi-die solutions, which can provide increased system architectural content. This approach can provide major benefits to customers and allow Xilinx FPGA products to provide more system value.

The availability of proven TSV technology along with low-latency interposer structures is being used effectively by Xilinx to expand the capabilities of the FPGA products. The technologies used by Xilinx have been used in the high-volume manufacturing environment, with the expectation that the quality and reliability of the finished products will be high, where customer risks are very low.