

# Designing High-Speed Interconnects for High-Bandwidth FPGAs

Commercial EM software combines with circuit and system simulation to achieve reliable data transmission.

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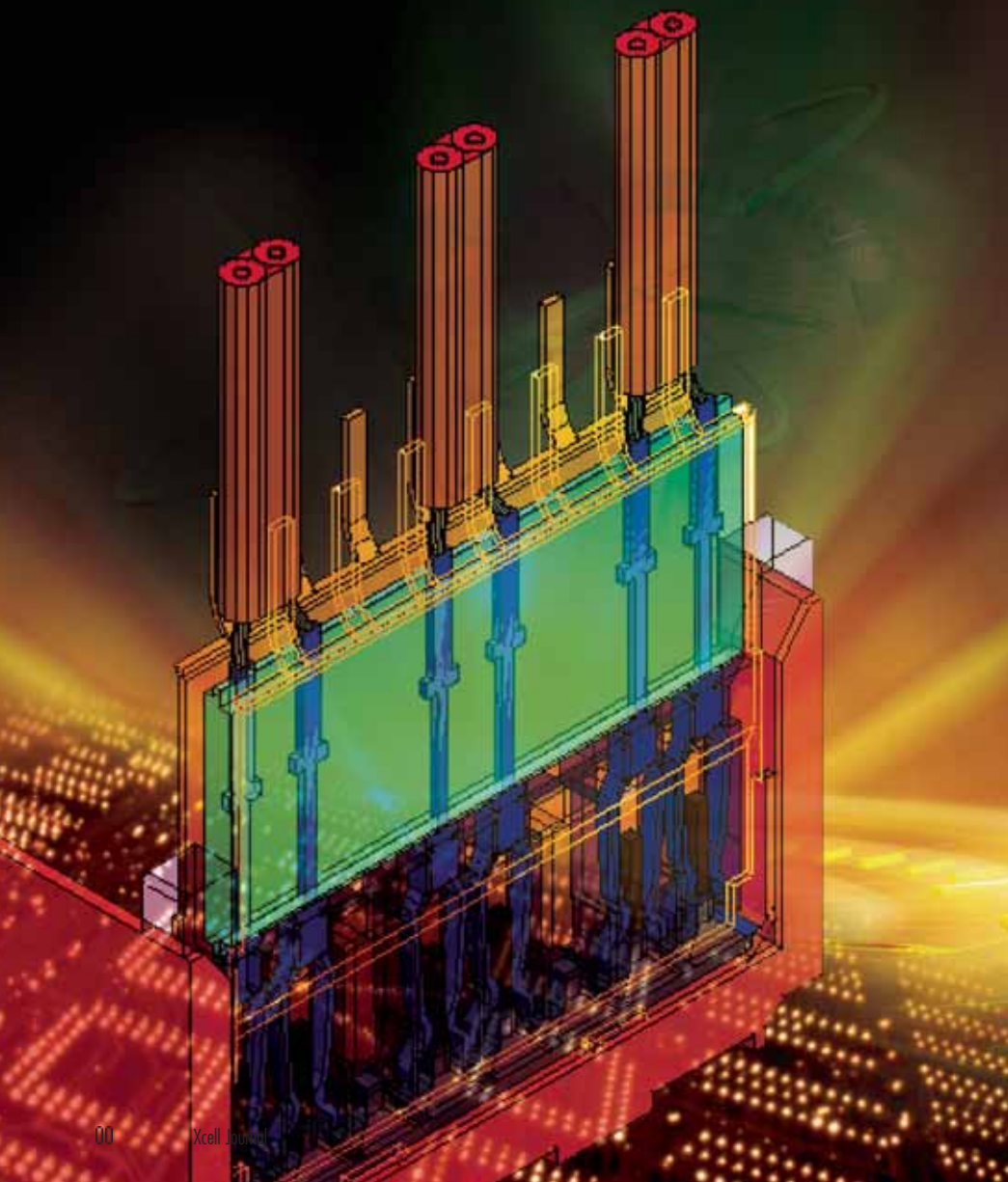
The push toward FPGA platform solutions with high-bandwidth DSP and gigahertz-speed I/O functionality has led to devices that place greater demands on PCB design. The high serial data rates of Xilinx Virtex-II Pro™ FPGAs (3.125 Gbps) and Virtex-II Pro X™ FPGAs (10 Gbps) require careful signal integrity design for proper system operation.

In this article, we'll explain how to combine commercial electromagnetic (EM) software with circuit and system simulation to characterize transmission lines, vias, and connectors for systems that incorporate high-bandwidth FPGAs [1]. We used two-dimensional EM simulation to extract quasi-static circuit models for the PCB transmission lines and three-dimensional EM simulation to extract models for vias and connectors. For end-to-end simulations, we applied a convolution simulator. Thus, it's possible to achieve reliable data transmission with proper use of modern design tools.

## High-Performance PCB Design

PCB designers aim to create interconnects that reliably transmit high-speed serial signals. Transmission lines, via structures, and connectors are the building blocks of the design – and all have their particular challenges. These structures are designed individually to meet particular metrics and are then assembled into a system-level interconnect to evaluate end-to-end performance.

The most common PCB transmission structures are the microstrip and stripline transmission line; they are easy to construct, and you can use both for signaling at gigabit speeds. Designers have also used single-ended lines successfully for lower speed designs; modern gigabit designs use differential signaling because of the advantages of noise immunity and reliable current return paths. The key parameters associated with PCB transmission lines are the characteristic impedance, delay, insertion loss, and crosstalk.



Via structures allow you to route circuit traces between layers of a multilayer board. Vias are particularly useful for transitioning from the pins of a ball grid array or connector down to stripline traces within the board. The most common and inexpensive via structure is the “through-hole” via.

Alternatives to the through-hole via are the blind via and the back-drilled via. Although these alternatives generally provide higher performance, most high-volume designs continue to use the lower cost through-hole via. Key issues in the design of through-hole via structures are unterminated via stubs and antipad radii.

Connectors provide an electrical and mechanical interface between circuit boards, or between boards and cabling. Connector performance is highly dependent on the escape-routing PCB interface. Designs can succeed or fail depending on the choice of route layer and resultant via stub length, antipad dimensions, board materials, and escape-routing layout. Additionally, transmission bends within connectors skew the transmission path and can lead to mode conversion.

### Electromagnetic Model Extraction

The most common printed circuit board material is FR4. Although inexpensive for circuit fabrication, FR4 suffers significant dielectric losses at high frequencies. Typical material properties for FR4 are  $\epsilon_r = 4.2$  and loss tangent  $\tan\delta = 0.022$ .

An alternative to FR4 is to use a lower loss Getek™ material. Getek II’s material properties are  $\epsilon_r = 3.4$  and loss tangent  $\tan\delta = 0.006$ . Figure 1 depicts a layer within a typical backplane board. The layer height is 0.272 mm (10.7 mils); trace width is 0.125 mm; trace separation is 0.250 mm. Half-ounce copper plating for the traces provides a trace thickness of 0.7 mils.

We performed simulations using the two-dimensional, quasistatic finite element simulator within the Ansoft Q3D software suite. The stripline geometries were designed to provide nominally 100 Ohms of differential impedance, and simulations confirmed that the impedance was within 4% of the nominal value.

Figure 2 depicts three methods by

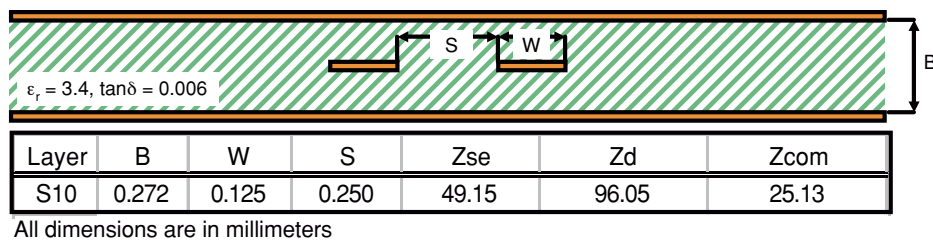


Figure 1 – Two-dimensional quasistatic simulations performed on stripline transmission structures using Ansoft Q3D. The table lists single-ended, differential, and common impedances.

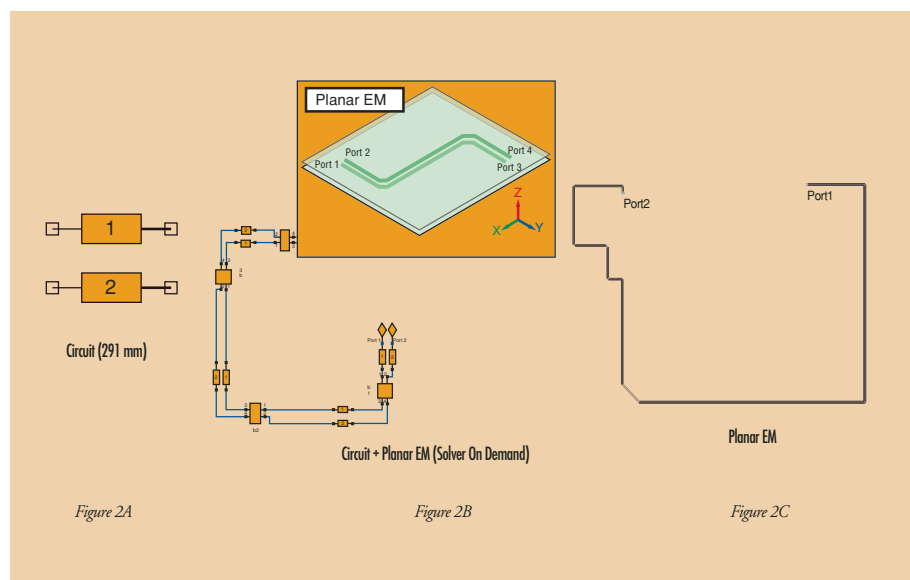


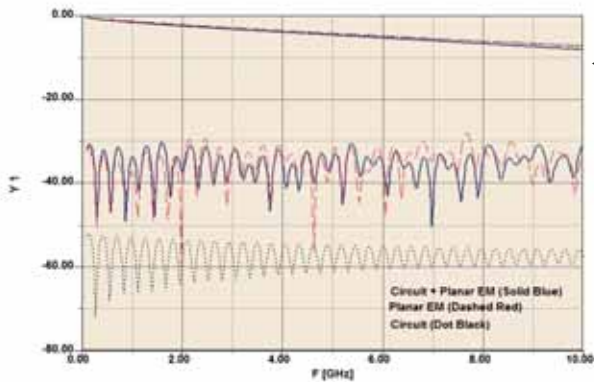
Figure 2 – You can model PCB interconnects using various methods. Circuit models (A) are the simplest and least expensive computationally; planar EM (MoM) simulations (C) are most expensive computationally but also the most accurate; a combined circuit + planar EM (B) provides accurate results with relatively low computational effort.

which you can model the PCB interconnects. The simplest is to use a coupled-line circuit model (Figure 2A), found in popular high-frequency circuit simulators like Ansoft Designer™. In this instance, the interconnect is modeled with a uniform differential coupled transmission line without any discontinuities.

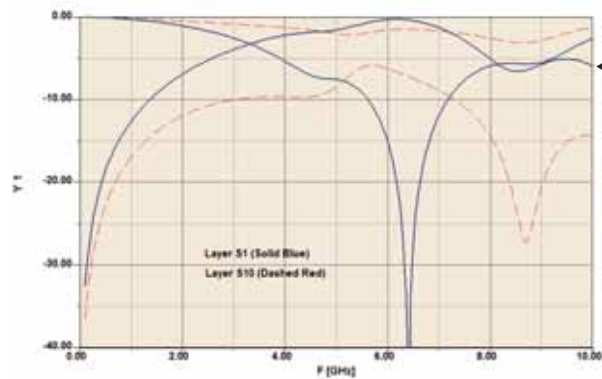
On the other end of the modeling spectrum is a full-wave planar EM field simulator based on the method of moments (MoM) (Figure 2C). The Ansoft Designer Planar EM simulator separates the traces into thousands of triangular elements. Numerical simulations compute the current flow on all triangles based on the EM coupling between them. As such, these computations completely characterize signal transmission and reflection on the interconnect.

Although accurate, MoM simulations are also the most computationally expensive. A compromise that offers the accuracy of planar EM simulations and some of the speed of circuit simulation is to use a combination of the two (Figure 2B). Ansoft Designer allows you to subdivide interconnects into a model with circuit elements and EM elements. Circuit elements are used for long, uniform sections of the coupled transmission line. EM simulation is used for all coupled line bends, as shown in Figure 2. This “solver on demand” approach automatically calls the planar EM solver whenever a bend is encountered.

Figure 3 plots the results of the three simulation methods outlined in Figure 2. All methods accurately predict the insertion loss. The circuit model cannot provide meaning-



◀ Figure 3 – PCB interconnect simulation results show that all methods outlined in Figure 2 accurately predict insertion loss. Return loss cannot be predicted with the circuit model alone.



◀ Figure 5 – “Through-hole” via performance as simulated using Ansoft HFSS. Note the sharp resonance in the insertion loss for the worst-case via routed to layer S1.

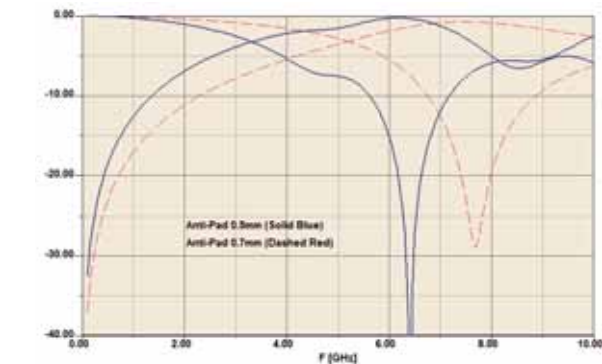
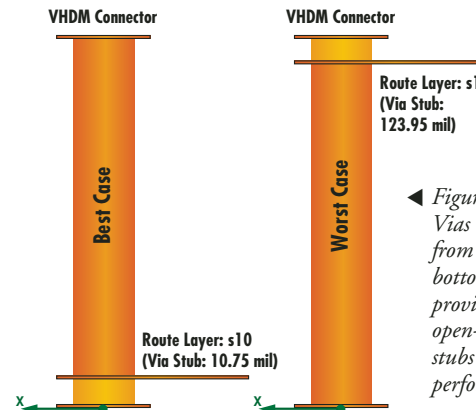


Figure 7 – Differential via performance for layer S1 (worst-case) routing for two antipad radii

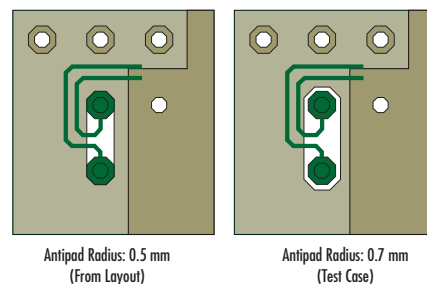
ful return loss, as it does not contain any of the coupled line bends. The circuit plus planar EM method (solver on demand) provides return loss results that are in close agreement with the planar EM results. This method provides accurate results with a greatly reduced computational expense.

### Vias

A common signal integrity design practice is to place high-speed route layers on opposite sides of the board in order to avoid open-circuit via stubs [2]. Figure 4 depicts two via structures: a best case and worst case. The best case occurs when routing from the top layer to layer S10, as this



◀ Figure 4 – Vias that transition from the top to the bottom of a board provide minimal open-circuited via stubs and “best-case” performance.



◀ Figure 6 – Antipad radii should be sufficiently large to avoid capacitive coupling to power and ground.

results in a very short (10.75 mil) via stub. The worst case occurs when routing to layer S1, leaving a very long (123.95 mil) via stub.

Figure 5 plots the insertion and return loss of an isolated differential via computed using the three-dimensional full-wave field solver Ansoft HFSS. The solid blue curve represents the via that transitions to layer S1. This is considered the worst case, as it has a very significant open-circuited via stub and an associated resonance in the insertion loss near 6.5 GHz. The dashed red curve represents the via that transitions to layer S10. This is considered the best case, as it provides a very flat insertion loss response to 10 GHz, and return loss is good to roughly 4.5 GHz.

Another consideration when designing vias are the antipads that exist on all power and ground layers. Figure 6 depicts two differential via structures with antipad radii of 0.5 mm and 0.7 mm. You can improve performance by using the larger antipad radius

[2]. We performed simulations using Ansoft HFSS to predict the performance of each.

Figure 7 shows the swept frequency results for both via antipad radii for differential vias routing to layer S1 (worst case). As you can see in the plot, a significant increase in bandwidth is possible with this simple modification. The resonance in the

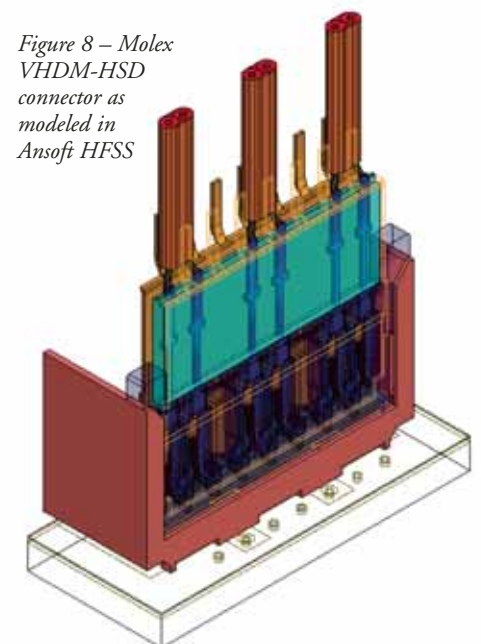


Figure 8 – Molex VHDM-HSD connector as modeled in Ansoft HFSS

insertion loss has been pushed up from 6.5 GHz to roughly 7.75 GHz. This is one of the simplest modifications that can be made to a PCB board file and should be considered for all high-performance designs.

### Connectors

A common connector used to transition between boards and differential coaxial cables is the Molex™ very high density metric-high-speed differential (VHDM-HSD). Ansoft HFSS performed simulations of such a connector (Figure 8). On one side of the connector are three twin-ax cables; on the other side is a backplane board with its associated escape routing.

Figure 9 plots the insertion and return loss versus frequency for the VHDM connector without the escape routing. This connector provides a very flat insertion loss across the band. Return loss is below 10 dB up to 3 GHz.

Results for the connector (including all escape routing) are computed by cascading S-parameters from the individual HFSS models for the connector and the backplane board, escape routing to the model has a significant effect.

Figure 10 plots the differential S-parameters for a channel containing a worst case via transition that leaves a long unterminated via stub. The performance of the VHDM connector is dominated by the sharp resonance of the via stub that manifests itself at 6.5 GHz.

### System Simulation

It is possible to cascade results generated from EM and circuit simulations to get a full system simulation. Figure 11 plots circuit simulation results displaying the insertion and return loss up to 10 GHz. As expected, the channel has a response similar to a low pass filter.

We performed time domain simulation using the system simulator in Ansoft Designer. This simulator uses a convolution algorithm to process the frequency domain channel data with user-defined input bitstreams. Insertion and return loss are included

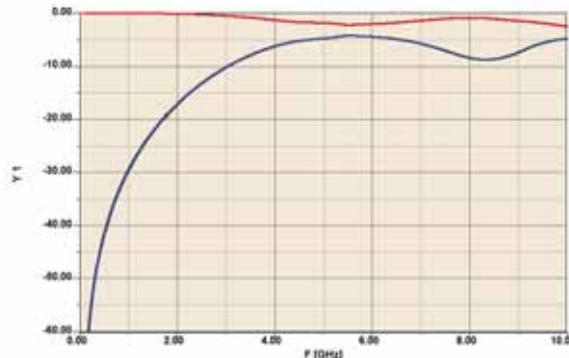


Figure 9 – Differential S-parameters for the Molex VHDM-HSD connector in isolation

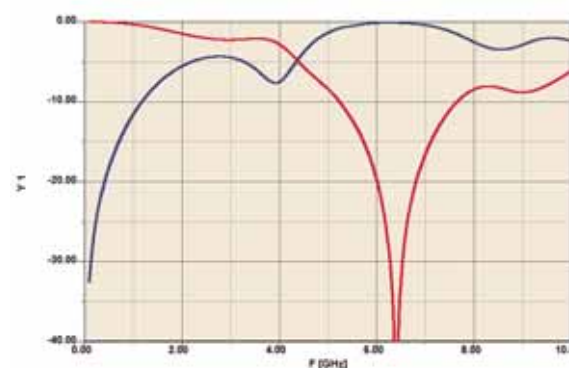


Figure 10 – Differential S-parameters for the Molex VHDM-HSD connector with backplane escape routing. This worst-case channel with large via stub shows signature resonance at 6.5 GHz.

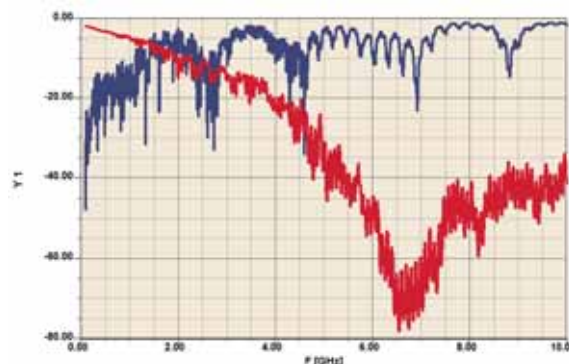


Figure 11 – Full-channel cascaded performance using the models developed from EM simulations up to 10 GHz

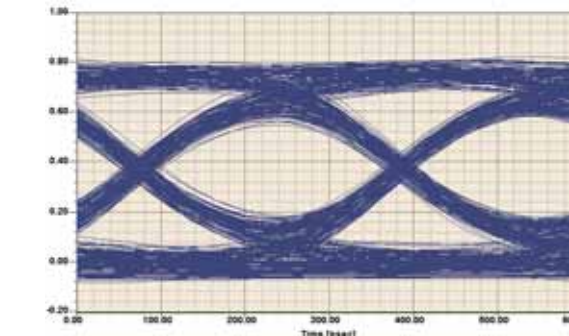


Figure 12 – Full-channel eye diagram using convolution system simulator in Ansoft Designer for the cascaded model with a 125 ps risetime

in the simulation. A 3.2 Gbps pseudo-random bit source with a 1V peak-to-peak amplitude and 125 ps risetime was applied to the channel. The channel was terminated in single-ended 50 Ohm resistors.

Figure 12 shows the resulting eye diagram as very clear and open, despite the significant channel impairments in the frequency domain results. We did not apply any pre-emphasis in the simulation. You should anticipate that some pre-emphasis would sharpen the time-domain response.

### Conclusion

Modern platform FPGA devices provide wide bandwidth processing and high-speed I/O. Serial I/O with speeds in the gigabit realm creates new challenges for PCB designers.

You can solve the high-speed I/O challenges posed by modern platform FPGA devices using EM, circuit and system simulators. Although we focused our attention on the passive interconnect in this article, it is possible to include nonlinear I/O drivers and receivers in the simulation to obtain additional insight to system performance. Indeed, you can use a new tool from Ansoft called Nexxim™ to simulate all circuit behavior for systems including EM-based models, linear, and nonlinear circuits. Visit [www.ansoft.com](http://www.ansoft.com) for more information about Ansoft Designer and Nexxim. ❧

### References

- [1] Williams, L., S. Rousselle, and B. Boots, "Cray Supercomputer 3.2 Gb/s Serial Interconnect Simulation Using Full-wave Electromagnetics," in DesignCon 2004 Conference Proceedings, Santa Clara, CA, Feb. 2-5, 2004.
- [2] Williams, L., S. Rousselle, and B. Boots, "Circuit board design for 10Gbit XFP optical modules." EDN, May 29, 2002, pp. 63-70.