Designing for Power Budgets and Effective Thermal Management

Xilinx provides the critical edge with power-optimized FPGAs, thermal-efficient packaging, and power analysis tools.

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Meeting power and thermal budgets is one of the essential criteria by which our customers measure the success of their FPGA-based system designs. Constrained both by the density (bandwidth, logic density, and functionality) of the applications they are creating and the environments in which these systems are deployed, FPGA designers need every advantage as they painstakingly balance performance, cost, reliability, and power.

Xilinx demonstrated its commitment to empower its customers' success with the introduction of the Virtex™-4 family of FPGAs. Delivering the lowest total power in any 90 nm high-performance FPGA without compromising performance (1 to 5W lower than any competing 90 nm device), Virtex-4 devices employ a variety of power-saving design techniques to provide the lowest inrush current, static power, and dynamic power. (For more details about the Virtex-4 power advantage, please see "Power vs. Performance: The 90 nm Inflection Point" in the August 2005 issue of the *Power Management Solution Guide*, *www.xilinx.com/solguides.*)

This substantial power advantage provided by Virtex-4 devices translates directly to additional measurable benefits in performance, cost, and reliability. Reducing the FPGA's contribution to total power in a given design alleviates a host of problems incurred by excessive power.

What Cost Power?

Excessive power is expensive in many ways. It creates the need for special system design and operational considerations such as electricity changes and battery back-up costs. Increased power requires more of everything, including more area on the PCB, a larger chassis, more floor space, and larger air-conditioning systems. And because dynamic power is a function of clock frequency, you may be forced to run a design at a lower performance just to keep total power consumption low.

Perhaps the most critical issue is the effect excessive power can have on reliability. Continuously operating systems with junction temperatures running from 85°C to more than 100°C increase reliability issues and decrease mean time between failures (MTBF).

Power and Thermal Budgets

Every system has a power and thermal budget driven by a standard such as NEBS, ETSI, or other requirements (see sidebar, "NEBS"). A look at various types of electronic equipment can provide valuable insight into the importance of power budgets and demonstrate how a seemingly small power savings for each FPGA can translate into enormous value within overall system operation.

Infrastructure Equipment

Metro aggregation systems (such as enterprise Ethernet/layer 2 switches and multi-service provisioning platforms) are typically deployed in temperature-controlled rooms to ensure acceptable transistor junction temperatures. A typical multi-service provisioning platform (MSPP) is populated with multiple line cards supporting a range of data and voice transmission standards. Each line card usually contains numerous ASSPs, ASICs, and FPGAs.

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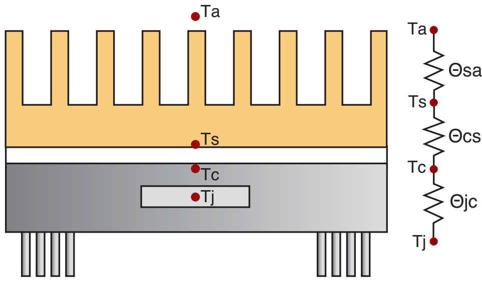

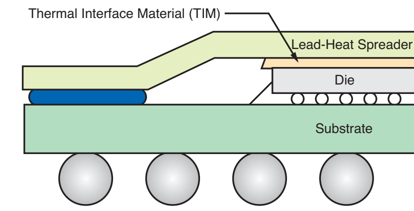

Figure 1 – Heat transfer in devices and how Virtex-4 FPGAs address them

For an FPGA that performs connectivity and traffic management functions, reducing power is critical to system reliability and operational costs. Using a power-optimized FPGA that saves 1-5W per device will dramatically impact the MSPP's total power, potentially allowing the use of smaller power supplies and reducing the size and number of heat sinks.

Now consider wireless base stations that are deployed outdoors in harsh environmental conditions with ambient temperatures exceeding 80°C and transistor junction temperatures in excess of 100°C. A typical wireless network may comprise as many as 35,000 base stations, with each base station utilizing 16 or more line cards.

Wireless base station power budgets are 1.2-2.5 KW; each line card (excluding backplane, fans, and system control) is about 20W. Using an FPGA for connectivity and signal processing, which saves as much as a third of the typical 6W power budget, can in turn save as much as $1 million in operational expenditures.

System Reliability Case Study

As stated previously, many applications are restricted in power by standards. Consider the networking OEMs who sell their equipment to operators and service providers. In the U.S., the operators require OEMs to meet NEBS (National Equipment Building Systems) standards. In particular, the GR-63-CORE and GR-1089-CORE standards specify equipment reliability criteria, on which the power, signal integrity, and thermal management of the equipment (and hence the components used) have a direct impact.

For example, consider an RPR (Resilient Packet Ring) MSPP. Such a system is limited to 4 KW/rack and must remain operational for 99.999% of the time, which equates to no more than five minutes of downtime per year.

Because FPGAs are used extensively in these systems within the various line cards, it is critical to keep the FPGA static and dynamic power consumption to an absolute minimum to help OEMs meet the GR-63-CORE standard.

The typical line card power budgets and FPGA power consumption illustrate the value Virtex-4 FPGAs offer by saving a just couple of watts per FPGA:

- 12-port DS3 card: 30W; FPGA = 4-5W
- 4-port OC-12 card: 28W; FPGA = 4-5W
- 12-port 10/100 Base-T card: 50W; FPGA = 4-5W
- 32-port T1/E1: 9W; FPGA = 2-3W

Thermal Management

Given the increasing criticality with which system vendors are scrutinizing their power and thermal budgets, Xilinx continues to strive to improve upon the edge it already provides with the Virtex-4 family.

Figure 1 shows heat transfer at various locations on a device with definitions of temperature and thermal resistance at each point. In addition to the effective thermal management Virtex-4 FPGAs provide at the silicon level, Xilinx also offers thermally enhanced flip-chip packages with built-in heat spreaders.

The new Xilinx flip-chip BGA packages are the latest package offering for Xilinx high-performance FPGA products. Unlike traditional packaging in which the die is attached to the substrate face-up and the connection is made by using wire, the solder bumped die in the flip-chip BGA is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

The flip-chip package accommodates more I/O pins than traditional wire-bond packages by using the internal chip area for package connections. Furthermore, the cavity-up nature of flip-chip packages allows for superior thermal dissipation through the top of the package.

Virtex-4 pinout provides abundant power and ground pins (Figure 2) – one adjacent to every user pin, providing even distribution for better thermal dissipation when compared to the clustered power and ground pins found in typical flip-chip packages.

To facilitate user design, Xilinx provides

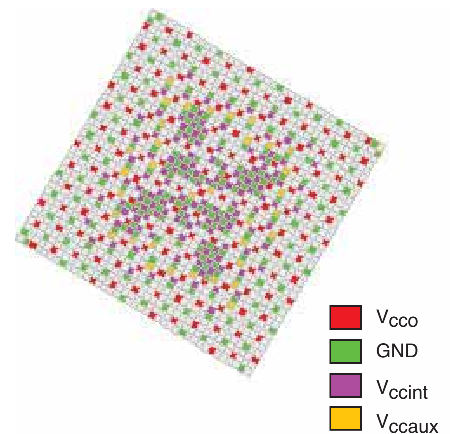

Figure 2 – Virtex-4 packaging, with uniform distribution of power and ground pins, enables better thermal dissipation.

Figure 3a – The Web Power tool allows you to set the operating voltage for the design; when feasible, this enables you to lower the voltage to save power.

Figure 3b – You select the particular utilization of slices, flip-flops, shift register and LUT RAMs, their toggle rates, and routing density to calculate the power used by the configurable logic blocks (CLBs).

JEDEC JESD-51 thermal characteristics (*http://direct.xilinx.com/bvdocs/userguides/ug075.pdf*) for a four-layer board. Although a four-layer board is quite conservative for most applications, it does provide a uniform standard-based comparison. For simulating your unique board setup, Xilinx can provide compact resistor models for the Virtex-4 device package combination.

Power Analysis Tools

Another edge Xilinx offers its customers is the ability to calculate power estimates both before and after design implementation. Xilinx Web Power tools provide pre-implementation estimates of a design's power consumption based on the expected utilization of device resources, operating frequencies, and toggle rates.

Post-implementation, XPower enables you to obtain more precise power-consumption estimates. Of course, the actual power consumption must ultimately be determined in circuit under the appropriate operating conditions.

Web Power

Xilinx Web Power tools help you estimate total power consumption accurately before design implementation. System architects can estimate power using high-level design details and make intelligent design choices on clock frequencies, implementing a function using hard IP or logic, type of I/O standard, and other factors. The Web Power tool relies exclusively on your estimates of FPGA design parameters such as utilization, toggle rates, and operating conditions (Figure 3a/3b).

To calculate a power estimate for a given design, simply enter the estimated design parameters for resource utilization, operating environment, clock rates, and toggle rates, push a button to calculate power, and save the settings. A brief look reveals the intuitively simple nature of this process:

1. Set the operating voltage of the design.
2. Enter the settings for the part and package, typical or worst case process, and thermal information (ambient temperature and airflow).
3. Select the particular utilization of slices, flip-flops, shift register and RAM LUTs, their toggle rates and routing density, to calculate the power used by the configurable logic blocks (CLBs).
4. Specify the number of DSP48s, their architectural usage level, and toggle rates.
5. Select the digital clock manager (DCM) settings.
6. Specify input/output settings.
7. Press the "calculate" button to generate the pre-implementation power estimate with totals at every level.
8. Press the "save settings" button to save the settings for future analysis and modifications.

XPower

Xilinx XPower is a post-implementation power analysis and power estimation software. Included in all configurations of the Xilinx Integrated Software Environment (ISE™ software), XPower enables you to analyze total device power.

Figure 4 – You can run XPower after map, place and route, or timing simulation.

XPower can read HDL simulation data to estimate toggle rates. XPower uses proprietary algorithms to estimate toggle rates even if the simulation vectors are missing, which is useful for iterative design. Figure 4 shows XPower in the design flow.

XPower includes a design wizard that provides a step-by-step dialog box format to help you import design and simulation data and set loading and default data. The design wizard also helps you get accurate power estimates quickly and easily.

The step-by-step process for using XPower is straightforward and intuitive:

1. Invoke XPower in ISE software.
2. Open design.
3. Load design (NCD).
4. Load optional PCF and simulation data files.
5. Launch the new design wizard.
6. Set voltage, ambient temperature, and airflow.
7. Set frequencies and activity rates.
8. Set capacitive loads for outputs.
9. Set/verify DC loads for outputs.
10. Set/verify enable rates for bi-directional I/Os if simulation data is not loaded.
11. Set global default activity to estimated value.
12. Set estimated activity for any single or groups of signals.

Corroborative Results

Given the value of these power estimation and analysis tools and the essential need for accuracy both before and after the design has been implemented, you might wonder just how much of an advantage these tools provide.

Of course, a great deal hinges on the accuracy of the settings relative to actual design parameters and operating conditions. Nonetheless, Xilinx offers the results of this simple, yet revealing test example as evidence of the veracity of these power tools.

Using a Virtex-4 4VLX60 device, we tested for a correlation of logic, register, and interconnect power across a large design. We ran the design through ISE 7.1i software and compared the power data to estimates developed by the Web Power tool and measurements in a lab. The results in Figure 5 speak for themselves.

Virtex-4 4VLX60 FF1148
Design Parameters
100 MHz, 200 MHz
21,849 LUTs, 25421 FFs; 36% toggle rate

Power Data Comparison – Dynamic			
Frequency (MHz)	Web Power (mW)	XPower (mW)	Measured (mW)
0	0	0	0
100	1,864	1,750	1,742
200	3,727	3,429	3,482

Figure 5 – When compared with actual measured results, the close approximation of the pre- and post-implementation power estimation tools demonstrates the value these tools provide to system architects and FPGA designers.

Conclusion

Designing high-performance FPGA-based systems constrained by exacting power and thermal budgets will never cease to present a daunting challenge to the design engineers and architects who must regularly build them.

As Xilinx customers continue to place their trust in our ability to provide them with the essential edge in power-optimized FPGAs, tools, and package technology, we have and will continue to strive to reduce the challenge of effective power and thermal management. For more information, visit *www.xilinx.com/virtex4/lowpower*.

NEBS

The National Equipment Building Systems (NEBS) standards prevent the target system from interfering with other equipment, while ensuring scalability and safety. The two major standards, GR-63-CORE and GR-1089-CORE, were originally developed by Bellcore/Telcordia in the 1970s and deployed in 1985.

These standards establish physical requirements such as space planning, temperature, and humidity environmental specifications. They also specify acceptable preventative measures to guard against potential hazards such as fire, earthquake, vibration, transportation, acoustics, poor air quality, and illumination.

The standards also specify the electrical requirements that safeguard the equipment against electrostatic discharge (ESD) and electromagnetic impulse (EMI), as well as establishing resilience to lightning and AC power faults.

Other preventative measures established by the standards address issues such as steady state power induction, corrosion, DC potential differential, electrical safety, bonding, and grounding.