

High-Performance Image Processing on FPGAs

You can develop and implement sophisticated imaging modules on low-cost devices.



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The rapid evolution of digital imaging technology, accompanied by huge market demand for cameras and displays in both consumer and industrial segments, presents a significant challenge to device developers who want to create high-quality products. To extract the best possible images from capture and display hardware, sophisticated image processing algorithms are available. But their implementation is limited by several factors: the intrinsic complexity of the algorithms; the pressure to reduce bill of materials costs; the need to support a wide variety of developing formats; and the frequent requirement to customize particular device environments.

The development and licensing of image-processing IP is central to Apical's business. Addressing the factors I have described in the preceding paragraph is therefore key to our company's success. If the design of a new IP core is hindered by difficulties in coding and verifying RTL, or if a customer has no straightforward way to evaluate and implement the IP in their products, then the initial enthusiasm of an exciting research result rapidly evaporates.

FPGAs have proven to be highly effective in enabling our company to shorten time to market for our IP, especially in video applications. By using FPGAs extensively in IP development, time to market is reduced, IP quality increases, and a ready route to commercialization is possible. In this article, I'll explore these benefits in the context of image enhancement technology for display applications.

Image Processing for Flat-Panel Displays

The image quality of a display is driven by its dynamic range and color gamut. Dynamic range is essentially the difference in brightness between the darkest and brightest image content that can be rendered under particular ambient lighting conditions. Color gamut represents the range of color space that can be accurately

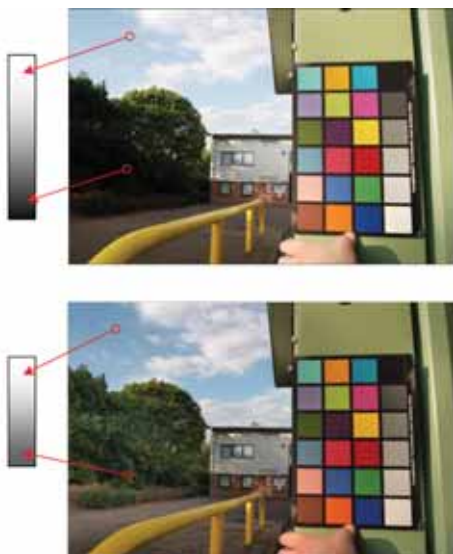


Figure 1 – Effect of space-variant dynamic range compression

reproduced. In comparison to traditional cathode ray tubes (CRTs), flat panels have certain limitations in both of these key characteristics. In particular, they have a lower dynamic range and particular problems in dark regions where true blacks are difficult to produce.

The standard technology for adjusting input video imagery to the dynamic range of the display is gamma correction, or some modification where the image processing pipeline incorporates a finely tuned non-

linear gain curve. However, a significant dynamic range adjustment leads to a degradation of image quality, with a loss of contrast and distortion of color.

A much better approach is to use an adaptive, space-variant approach. This applies different dynamic ranges and color correction in unique regions of the frame. Regions well within the display's capabilities are unaltered, but those outside can be drawn in. With Apical's iridix technology, a different non-linear correction is applied to each individual pixel based on a statistical analysis of the input frame. The effect of this algorithm on an image with a wide dynamic range is shown in Figure 1. Effectively, the algorithm is applying a different, optimized gamma curve to every pixel in every frame of the video signal.

Such an algorithm is much more demanding than the traditional technique. It is a two-pass process, mathematically complex, requiring high-precision operations (at least 12 bits) and high-speed calculations to transform streaming video data and handle large frames (HDTV) in real time.

In addition to algorithmic complexity, other development challenges are incorporating a continuous flow of new results from R&D, supporting many different video formats, and addressing customization requirements.

FPGAs as a Platform for Image Processing

Traditionally, the route to implementing image-processing functions in consumer devices is through an ASSP or a DSP. Both of these routes remain valid, and in some cases are still optimal. But their limitations are

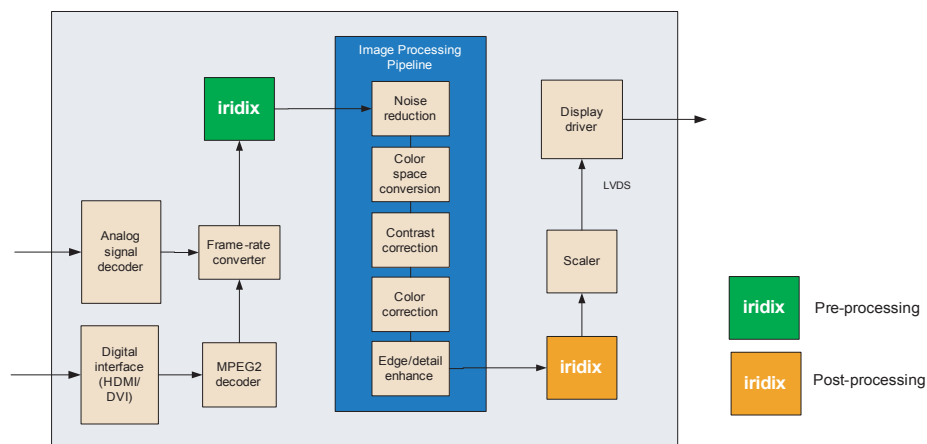


Figure 2 – Typical display pipeline showing options for pre- or post-processing through an FPGA.

Incorporating such an algorithm into a display image-processing pipeline, as shown in Figure 2, can dramatically improve the final image quality. A display equipped with such processing can render images well even under very bright ambient lighting, while retaining perfect colors and contrast under ideal viewing conditions.

In fact, you can perform this processing at any stage, on source YUV data or processed RGB. It is often most convenient to include it either before (pre-processing) or after (post-processing) the standard display pipeline. In practice, you can achieve the best results at post-processing.

well-known: ASSPs are inflexible, expensive, and time-consuming to develop; powerful DSPs are costly and their corresponding software applications may not match the performance of hardware. The attractiveness of FPGAs derives from the combination of the virtues of the alternatives.

The flexibility of the FPGA is of particular importance to Apical, as both the image processing algorithms and their target display applications are evolving rapidly. Time to market is a crucial factor in all consumer applications; this must be shortened as much as possible without compromising the quality of the product.

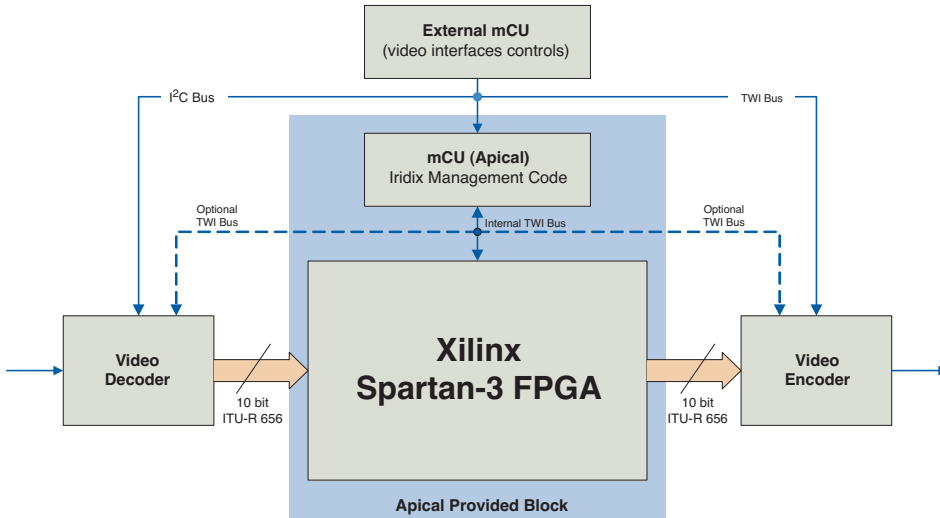


Figure 3 – Example Spartan3-based architecture for stand-alone video processing

IP Requirement	FPGA Requirement
Logical Complexity	Around 5,000 Slices or More
Real-Time Pixel-by-Pixel Transformations	Embedded Hardware Multipliers
Storage of Look-Up Tables and Statistics	Embedded Memory
Time to Market	Good Development Environment

Table 1 – FPGA characteristics required by Apical's IP

Property	Spartan X3S1500-4
Slices	4,379
Logic	28% of Logic 40% of Multipliers
Memory	17% of Memory
Clock Frequency	75 MHz

Table 2 – Statistics of Apical's "iridix" core on Spartan-3 FPGAs

Given the complexity of the algorithms, it is simply not possible to test a behavioral model exhaustively over hundreds of hours of video footage, which is necessary to analyze image quality and detect artifacts. A single frame may take several minutes to process. Therefore, the importance of implementing the design in hardware as soon as possible begins conflicting with the traditional approach of full simulation before implementation.

In addition, flexibility is critical because the IP may require customization as part of a display optimization process. Although there are standards that govern many aspects of video formatting in display applications, it is neither possible nor commercially attractive to attempt to standardize image quality. The value of the IP therefore increases with flexibility and customizability.

To make practical use of the flexibility of FPGA architectures, the device must meet the performance requirements of the application. For Apical's primary algorithms, these are listed in Table 1. Apical's principal dynamic range compression IP is significantly more complex than most image pipeline IP, but nevertheless a device such as a Xilinx® Spartan™-3 FPGA has all of the necessary resources. Even HDTV video can be processed at 60 Hz on a relatively inexpensive Spartan-3500E FPGA.

In achieving Apical's time-to-market objectives, the availability of a good development environment is crucial. Xilinx ISE™ software provides such an environment, and the recently announced Spartan-3 Display Solutions Board pro-

vides a convenient development and demonstration platform for Apical's IP.

FPGAs in Display Products

Until relatively recently programmable logic devices would not have been considered for the implementation of complex video IP in a device such as a flat-panel display, leaving ASSP the only option. However, FPGA technology has developed rapidly; low-cost devices such as Spartan-3 FPGAs are now well suited to such applications.

The performance/cost ratio of Spartan-3 FPGAs is such that they present an alternative to ASICs in numerous applications, including flat-panel displays. They provide a ready solution to a device developer's dilemma that "we need to include this new IP, but we don't want to increase our design risk or time to market." You can update the FPGA bitstream as easily as embedded software and in addition customize it to fit optimally with the panel characteristics and the rest of the display imaging pipeline.

You can conveniently control algorithm parameters through an I2C-compatible (two-wire) interface using a simple 8-bit microcontroller, as shown in Figure 3.

Given enough logic, the FPGA can deliver multiple, tailored image enhancements alongside a standard ASSP, handling additional functions such as decoding, deinterlacing, and scaling.

Conclusion

Dramatic progress has been made in image processing R&D over the last five years, with the potential for displays to deliver unprecedented visual quality even within a climate of strong price pressure. In a device build, the imaging pipeline has by far the highest contribution to the final appearance in comparison to its modular cost.

Spartan-3 devices present a new alternative to ASICs for imaging device makers to augment their products using image-enhancement IP such as that provided by Apical.

For more information about the IP and its implementation in FPGAs, visit www.apical-imaging.com.