



Reliably Boost Memory Throughput with PLL-Based QDR II SRAM

NEC Electronics' QDR II SRAM with PLL simplifies high-performance Virtex-5 memory interfaces by improving the data valid window.

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To maximize performance in systems that include Xilinx® Virtex™-5 devices and QDR II SRAM, you need good signal integrity and the widest possible data valid window. Getting a stable data valid window for QDR SRAM read data has become increasingly challenging as QDR frequencies increase. Fortunately, the extensive I/O resources of Virtex-5 devices allow you to accommodate whatever characteristics SRAM offers. The more reliable the data valid window, the less work you have to do to tune the interface.

QDR II SRAM from NEC Electronics dramatically improves the data valid window by using a phase-locked loop (PLL) rather than the conventional delay-locked loop (DLL). PLL-based QDR II SRAM thus makes it easier to realize the full potential of both QDR II SRAM and Virtex-5 devices in high-performance networking systems. In this article, I'll explain how to calculate the data valid window for such an SRAM and show how the PLL minimizes jitter that would otherwise constrain the data valid window.

Data Valid Window Calculation for QDR SRAM

When using the QDR II SRAM's CQ and CQ# clocks, you can make the following calculation:

$$\text{Data valid window} = \min. (\text{CQHCQ\#H}) - t\text{CQHQV} + t\text{CQHGX}$$

SRAM data sheets do not specify CQHCQ#H, but the parameter can be expressed as KHK#H – beta. For the ideal case, the beta is zero. With beta included:

$$\text{Data valid window} = (\min. \text{KHK\#H} - \text{beta}) - t\text{CQHQV} + t\text{CQHGX}$$

You also have to consider how jitter affects the echo clock and therefore the data valid

window. The echo clock is edge-aligned with read data Q, so the receiver must delay the echo clock to fetch read data (Figure 1). QDR SRAM is a single-ended I/O clock interface, so the worst-case timing occurs at the controller's hold time, when CQ has positive jitter (+a) and the following CQ# has negative jitter (-a).

The reference clock for the controller's hold time is then CQ with positive jitter (+a), and the read data hold time depends on the following CQ# rising edge, which exhibits worst-case timing when CQ# has negative jitter (-a). The controller sees the hold time reduced by the magnitude of positive CQ jitter (+a), as shown in

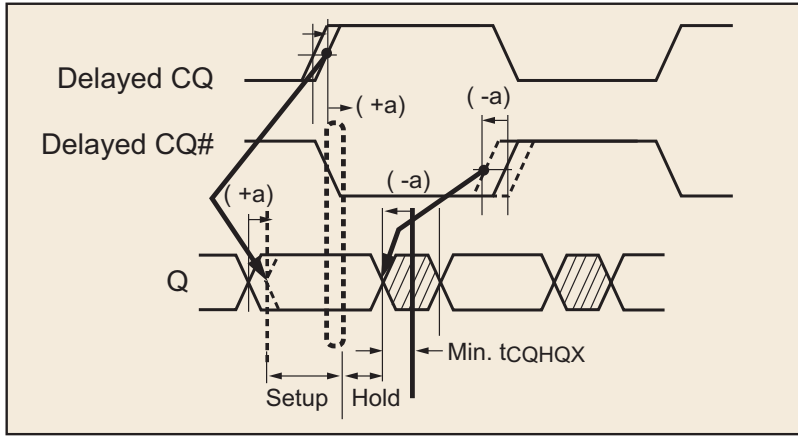


Figure 1 – Half of total echo clock jitter affects total data valid window.

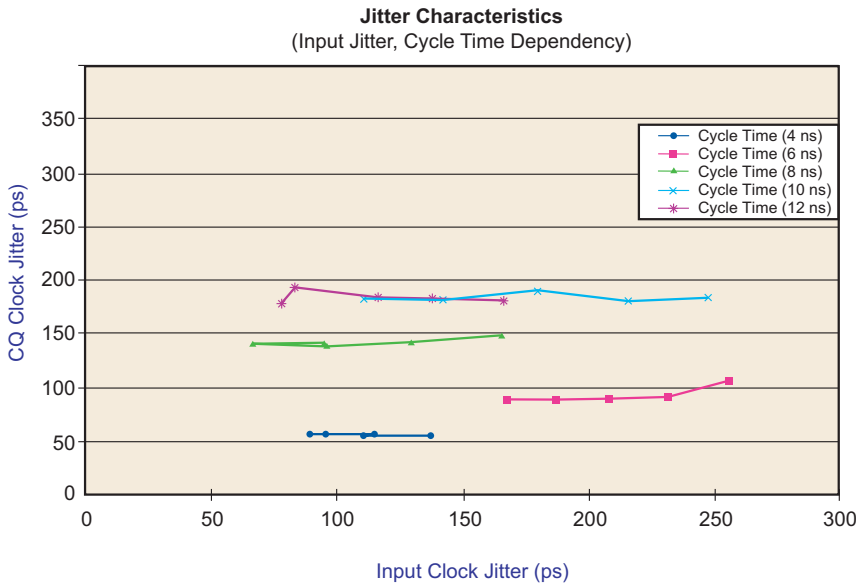


Figure 2 – Jitter characteristics for QDR II SRAM with PLL

Figure 1. The entire magnitude of the echo clock jitter, which affects the data valid window, is 0.5 * total jitter.

With these considerations, you have:

$$\text{Data valid window} = (\min. \text{KHK\#H} - \text{beta}) - 0.5 * \text{echo clock jitter} - t\text{CQHQV} + t\text{CQHGX}$$

To calculate the data valid data window for QDR SRAM, two factors must be clarified: beta and the magnitude of the echo clock jitter.

For all of the jitter measurements described in this article, I used a Wavecrest SIA 3000 signal integrity analyzer to measure total jitter (TJ) as deterministic jitter (DJ) plus 14 * random jitter (RJ) at room temperature.

Data Valid Window for Traditional QDR SRAM with DLL

When using a DLL for QDR II, you actually need two DLL circuits: one for CQ, referenced to the K clock, and another DLL for CQ#, referenced to the K# clock. Minimum KHK#H is specified as half cycle time – 10% of half cycle time. Thus, KHK#H is 1.8 ns when the cycle time is 4.0 ns.

Minimum CQHCQ#H is therefore less than minimum KHK#H (KHK#H – beta). The beta value is closely related to jitter, and the jitter value must be characterized to define the beta value.

As shown in Figure 2, however, the output jitter value fluctuates relative to the operating frequency and is proportional to the input jitter value when using DLLs. That is why QDR SRAM suppliers have been unable to define the echo clock jitter value and tCQHCQ#H on their data sheets.

Another parameter, tCQHQV/tCQHGX, represents individual I/O skew and read data jitter. By design, the devices have a 0.1 ns variation for tCQHQV/tCQHGX. Because of jitter, however, the QDR Consortium officially specifies this parameter as 0.3 ns at 250 MHz.

QDR SRAM with DLL has two uncertain parameters: beta and echo clock jitter. You must measure them to calculate the valid data window, even though you have no guarantees that process variation or device-to-device deviation will not occur.

Data Valid Window for Revolutionary QDR SRAM with PLL

NEC Electronics QDR II SRAM devices with PLL have demonstrated dramatic improvements in the width of the data valid window and high signal integrity with less output jitter, together with simplicity of design.

Minimizing Output Jitter

As shown in Figure 3, NEC Electronics QDR SRAM with PLL sometimes exhibits

output jitter smaller than input jitter. The device is stable regardless of input jitter variation; the magnitude of the jitter gets smaller as cycle times get shorter.

Maximizing CQHCQ#H

To improve the CQHCQ#H (or KHK#H – beta) parameter value, NEC Electronics has implemented a single PLL circuit for 36- and 18-Mb QDRII/DDR II shrink-die devices. These devices with one PLL reference the K clock rising edge only for both

CQ and CQ#. With this design, both CQ and CQ# are unaffected by KHK#H variation (half-cycle time – 10% of half-cycle time). This design also corrects the input-clock duty variation, so these clocks have close to a 50/50 duty-cycle ratio, regardless of K and K# input duty-cycle variation.

Therefore, CQHCQ#H references cycle time (T) rather than KHK#H (half cycle – 10% * half cycle), which enables a wider, more reliable data valid window. The beta value is closely dependent on output jitter characteristics.

With the help of smaller and more stable output jitter characteristics for NEC Electronics QDR SRAM with PLL, you can minimize the magnitude of the echo clock jitter. Thus, (min. KHK#H – beta) – 0.5 * echo clock jitter can be expressed this way:

$$(\text{min. KHK\#H} - \beta) - 0.5 * \text{echo clock jitter} = \text{TCQH\#CQ\#H} = 0.47 * T$$

where T is minimum cycle time.

Minimizing CQH\#V/CQH\#X Time

QDR SRAM with PLL minimizes the jitter impact on the tCQH\#V/tCQH\#X parameter. By correctly accounting for the read data Q jitter and echo clock jitter, the tCQH\#V/tCQH\#X parameter can improve from 300 ps to 200 ps at 250 MHz.

Including all of the considerations discussed so far, the data valid window for NEC Electronics QDR SRAM with PLL can be expressed in a simple way:

$$\text{Data Valid Window} = 0.47 * T - \text{tCQH\#V} + \text{tCQH\#X}$$

Figure 4 compares the data valid windows for QDR SRAM with DLL and QDR SRAM with PLL.

Conclusion

NEC Electronics QDR SRAM with PLL dramatically improves the data valid window, providing comprehensive, reliable solutions together with design simplicity. Using Virtex-5 ChipSync™ I/O technology, you can easily interface to QDR memory devices to take advantage of aggregate throughput as high as 43.2 Gbps for each 36-bit memory interface. ●●

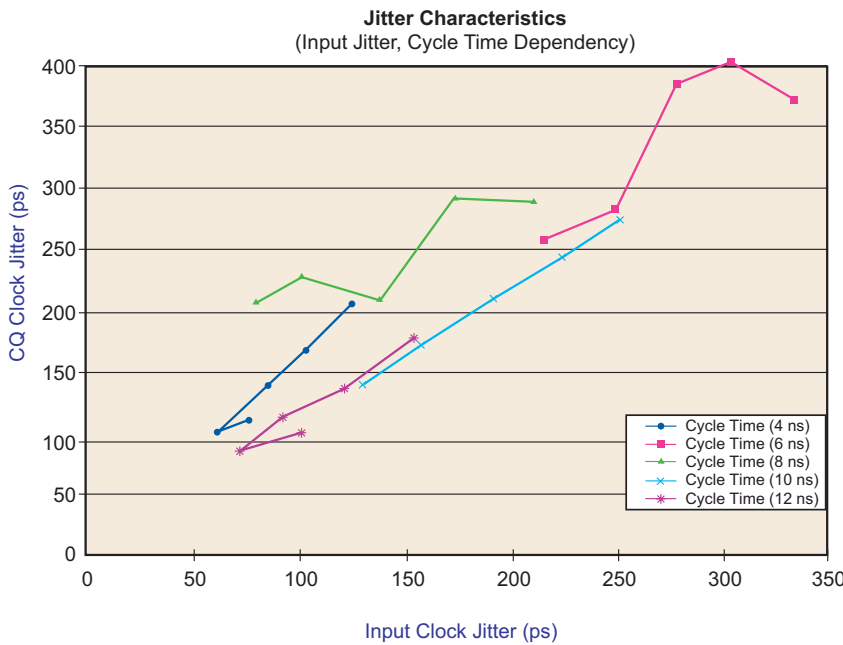


Figure 3 – Jitter characteristics for QDR II SRAM with DLL

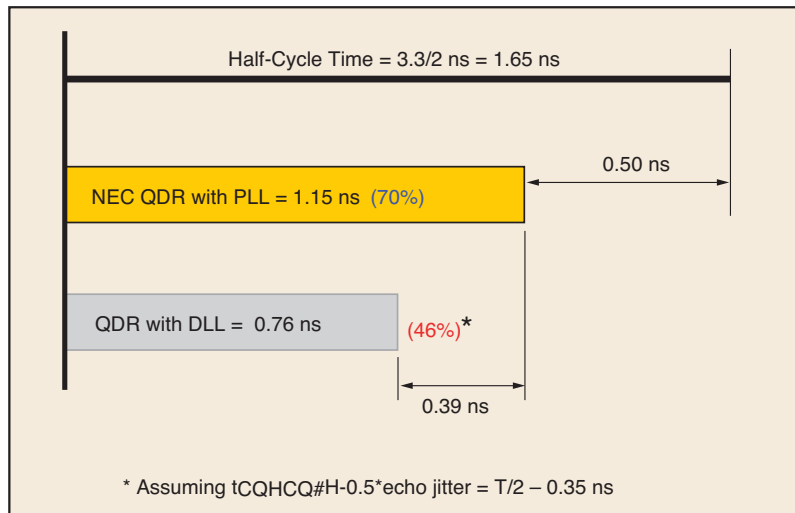


Figure 4 – Effective data valid window comparison at 300 MHz