

# Designing with Virtex-5 Embedded Tri-Mode Ethernet MACs

You can implement flexible Ethernet systems using the Virtex-5 10/100/1000 Ethernet MAC.

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Ethernet is the dominant wired connectivity standard. The Xilinx® Virtex™-5 Ethernet media access controller (Ethernet MAC) block provides dedicated Ethernet functionality, which together with Virtex-5 RocketIO™ GTP transceivers and SelectIO™ technology enables you to connect to a wide variety of network devices. The Ethernet MAC block is integrated into the FPGA as a hard block in Virtex-5 devices.

The Ethernet MAC is available in the Xilinx design environment as a library primitive, named TEMAC. The primitive contains a pair of 10/100/1000 Mbps Ethernet MACs. Each Virtex-5 LXT device contains four Ethernet MAC blocks; thus, a Virtex-5 LXT design can incorporate two TEMAC primitives. Using standard Xilinx products, you can create a range of customized packet processing and network end-point products. Xilinx has also provided an overclocking

mode to enable backplane connectivity at speeds as fast as 2,000 Mbps.

Xilinx developed the Virtex-5 Ethernet MAC from the Virtex-4 FX Ethernet MAC, making improvements in the areas of global clock usage, serial interface flexibility, and software control complexity.

In this article, we'll review the feature set of Ethernet MAC blocks in Virtex-5 devices. We'll also describe the differences between Virtex-5 and Virtex-4 FX Ethernet MACs, illustrate some potential applications, and describe how to use standard Xilinx tools to integrate an Ethernet MAC into your design.

## Supported Interfaces

The Virtex-5 Ethernet MAC is fully compliant to the IEEE802.3 specification. Figure 1 shows a block diagram of the Ethernet MAC.

## Physical Interfaces

You can independently configure the physical interface of each Ethernet MAC to operate as one of five different Ethernet interfaces.

The Media Independent Interface (MII), Gigabit Media Independent Interface (GMII), and Reduced GMII (RGMII) are parallel interfaces. These are typically connected to an external physical layer (PHY) chip to provide BASE-T functionality at 10/100/1000 Mbps. Half-duplex operation is supported at

10/100 Mbps; full-duplex operation is supported at all speeds.

Serial GMII (SGMII) and 1000 BASE-X are serial interfaces that use the physical coding sublayer (PCS) and physical medium attachment (PMA) sections of the Ethernet MAC. These interface to the Virtex-5 RocketIO GTP serial transceivers. SGMII, as with the parallel interfaces, provides 10/100/1000 Mbps full-duplex BASE-T functionality. The serial interface significantly reduces the number of pins required to connect to the external PHY chip.

When the Ethernet MAC is configured in 1000 BASE-X mode, the PCS/PMA block, along with the RocketIO transceiver, provides all of the functionality required to connect directly to a gigabit interface converter (GBIC) or small form-factor pluggable (SFP) optical transceiver. This removes the need for an external PHY chip for 1000 BASE-X network applications.

## Control Interfaces

The host interface provides access to the configuration registers of the Ethernet MAC block. Examples of configuration options include jumbo frame enable, pause and unicast address settings, and frame check sequence generation.

The host interface is accessible through either a generic host bus or a device control register (DCR) bus (when connecting to a processor). In addition, each Ethernet MAC has an optional management data

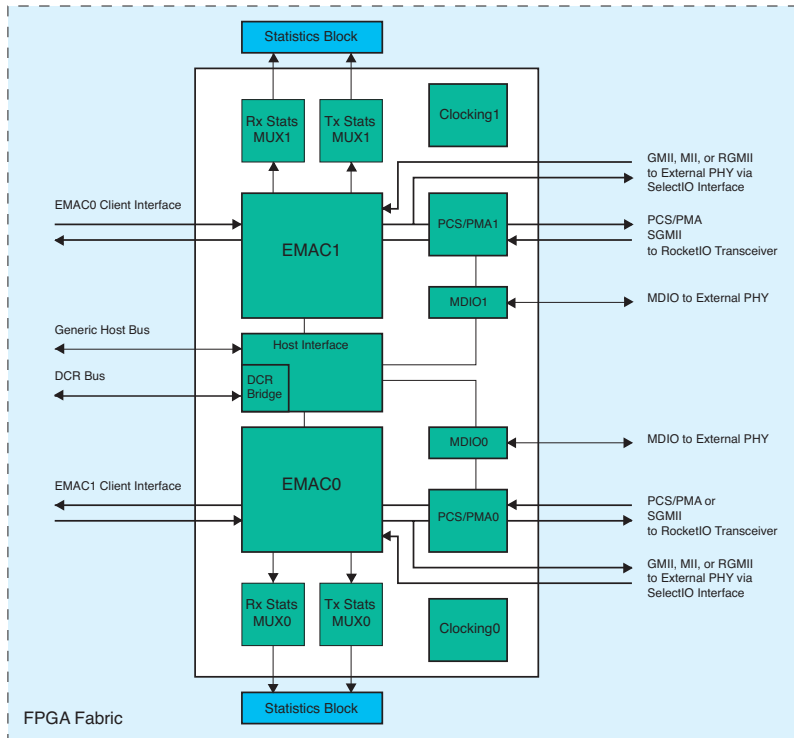


Figure 1 – Block diagram of the Virtex-5 Ethernet MAC

I/O (MDIO) interface. This allows access to the management registers of an external PHY and to the physical interface management registers within the PCS/PMA section of the Ethernet MAC.

**Client Interface**

Frames are passed to the Ethernet MAC across the transmitter client interface. The transmitter pads the incoming data when it is less than the minimum Ethernet frame length and maintains the minimum inter-frame gap between frames; however, you can increase the size of the gap. You can also configure the transmitter to add a frame-check sequence to the frame. A separate flow control interface allows you to generate pause frames. In half-duplex mode, the transmitter signals collisions and requests retransmissions for valid collisions.

The receiver interface verifies incoming frames and signals frame errors. Good and bad frame signals are provided. You can also configure the Ethernet MAC to pause and restart frame transmission upon the detection of valid pause frames.

The data on the client interface is 8 or 16 bits wide. The 8-bit interface is used for stan-

dard Ethernet applications, giving a 1,000 Mbps data rate with a 125 MHz clock. Using the 16-bit mode, you can increase the data rate to 2,000 Mbps without any increase in clock speed at the client interface.

Each Ethernet MAC outputs statistics vectors containing information about the Ethernet frames seen on its transmit and receive datapaths. An external statistics module is freely available in Xilinx CORE Generator™ software. The statistics module accumulates all of the Tx and Rx datapath statistics of each Ethernet MAC.

**New Features in the Virtex-5 Ethernet MAC**

In Virtex-4 FPGAs, implementing just the datapath consumes as many as four global clock buffers: one each for the Tx and Rx client interface logic, and one each for the Tx and Rx physical interface logic. For Virtex-5 FPGAs, Xilinx added a clock-enable feature. You can use the clocks derived for the physical interface for all of your client logic. The internally generated clock enable provides a way to maintain the correct data throughput on each of the interfaces. This reduces the number of necessary clock buffers by 50%.

**DCR Bus Addressing**

The Virtex-5 DCR interface now features an individual base address for each of the Ethernet MACs. This makes the shared DCR bus interface transparent to software drivers. The software no longer needs to know the bit locations for individual Ethernet MACs; the hardware automatically multiplexes in the correct bits depending on the base addresses.

**Serial Interface Changes**

Xilinx made several changes to the operation of the serial interfaces. Auto-negotiation is now more flexible with the inclusion of a programmable link timer. You can alter the timing of the auto-negotiation process and reduce simulation time.

A newly added unidirectional mode performs the unidirectional enable function from the IEEE802.3ah-2004 specification. When enabled, the Ethernet MAC transmits regardless of whether valid input is present at the receiver.

Finally, loopback can now take place in the Ethernet MAC as well as in the transceiver. This enables the transmission of idles to the link partner while in loopback, ensuring that the link remains active.

**Virtex-5 Ethernet MAC Use Models**

The versatility of the Virtex-5 Ethernet MAC enables its use in a wide variety of applications. For example, you can:

- Attach the Ethernet MAC to a processor running a protocol stack in network processing or remote monitoring systems, as shown in Figure 2.
- Interface the Ethernet MAC to a packet processing system implemented in the FPGA, such as a checksum offload engine or remote direct memory access design.
- Connect multiple Ethernet MACs to dedicated packet FIFOs and external memory for packet storage, bridging, or switching applications.

**Tools and IP Support**

Xilinx provides support for the Ethernet MAC through CORE Generator software, LogiCORE™ IP, and reference designs.

**Virtex-5 Ethernet MAC Wrappers**

Figure 3 shows a block diagram of the HDL wrappers available from the Xilinx CORE Generator tool.

The Ethernet MAC is a complex component with 162 ports and 79 parameters. Wrapper files enable you to easily set the parameters and interface only to those ports required for your application. They also offer benefits in simplifying the use of clocking and physical I/O resources.

The different levels of hierarchy enable you to extract the correct wrapper for your application.

- Ethernet MAC Wrapper. In the lowest level, a single or dual Ethernet MAC is instantiated and its attributes are set to your preferred selection in the CORE Generator GUI. All of the unused input ports are tied to ground and the output ports are left open.

- Block Level Wrapper. In the next level of hierarchy, the physical interfaces and the required clock resources are instantiated. This includes the RocketIO GTP transceivers for the serial interfaces. Clocking is also optimized for your configuration, and you can clock the output to your design.
- LocalLink Level Wrapper. In this level, FIFOs are added to the client transmitter and receiver interfaces. The FIFOs handle the dropping of bad frames on reception and retransmission of frames in half-duplex mode. LocalLink is used as the back-end interface.
- Example Design Wrapper. The top level features a demonstration design where the received data is looped back and sent to the transmitter. You can download this design to a board and stimulate the receiver from a network device to demonstrate the operation of the Ethernet MAC in hardware. Testbenches that stimulate receiver input and monitor the transmitter output of the design are also included in the CORE Generator software.

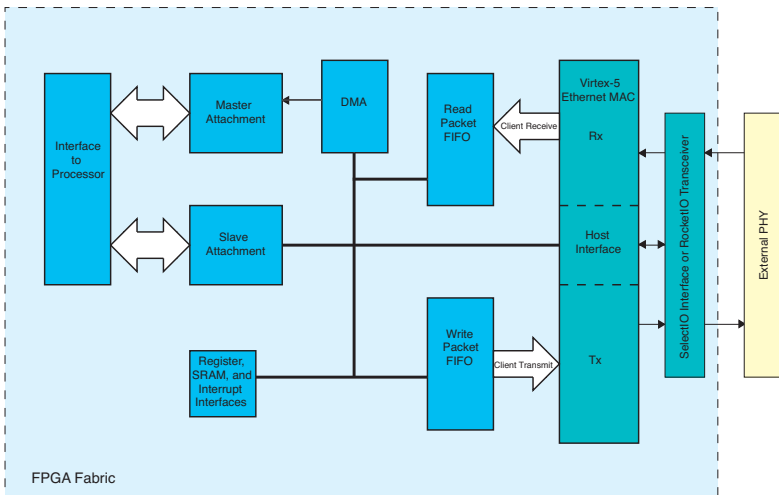


Figure 2 – MAC connected to a processor on the Virtex-5 FPGA

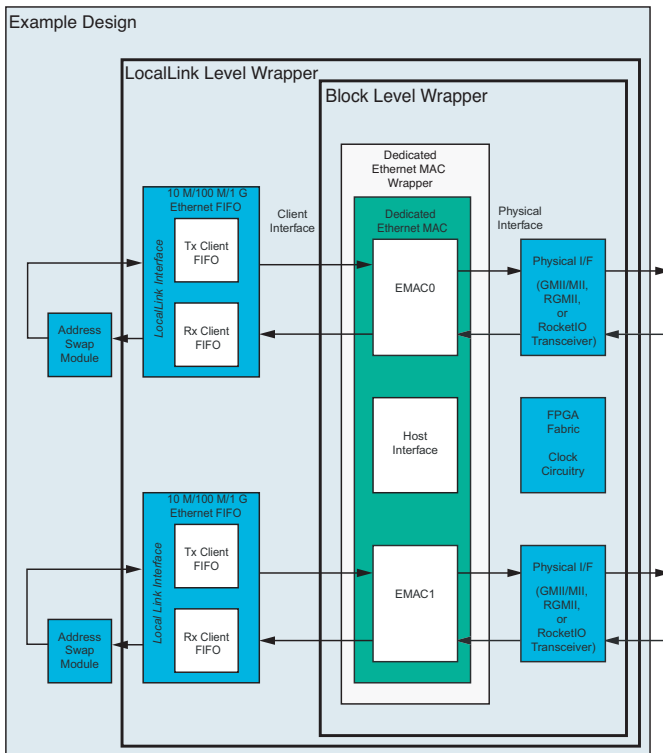


Figure 3 – Block diagram of the Virtex-5 Ethernet MAC wrappers

**LogiCORE IP and Reference Designs**

Most of the existing Virtex-4 Ethernet MAC documentation is reusable with the Virtex-5 Ethernet MAC. For example, a version of the “Ethernet Cores Hardware Demonstration Platform” (XAPP443, [www.xilinx.com/bvdocs/appnotes/xapp443.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp443.pdf)) will be available for the Virtex-5 Ethernet MAC. LogiCORE IP, such as Ethernet statistics, already supports the new architecture.

**Conclusion**

The Virtex-5 Ethernet MAC provides a cost-effective solution for a wide range of network interfaces, enabling you to connect to BASE-X and BASE-T networks at 10/100/1000 Mbps. Xilinx software tools and IP also allow you to take advantage of the improved feature set of the Ethernet MAC.

For more information, visit the Virtex-5 links on the Xilinx website, [www.xilinx.com/virtex5/](http://www.xilinx.com/virtex5/).