

# Implementing Integrated Video Connectivity Solutions with Virtex-5 LXT Devices

Xilinx Virtex-5 FPGAs provide the perfect platform for integrating broadcast video solutions inside a single chip.

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At Xilinx, we understand the challenges that broadcast system designers are facing. The number of emerging new standards for video connectivity creates difficult design challenges and schedules for broadcast products.

With the ever-changing video connectivity landscape prevalent throughout the broadcast chain, our goal is to offer help in the form of free reference designs, forming drop-in building blocks that can solve many system-level video connectivity issues. By providing you with cost-effective and highly integrated solutions compared to ASSP chips, Xilinx hopes to get you to market faster, lower costs, and differentiate your product from the competition.

Our video connectivity IP and reference design book, "Audio/Video Connectivity Solutions for the Broadcast Industry" ([www.xilinx.com/bvdocs/appnotes/xapp514.pdf](http://www.xilinx.com/bvdocs/appnotes/xapp514.pdf)), includes chapters about SDI, HD-SDI, DVB-ASI, AES embedded audio, and audio-asynchronous sample rate conversion. Each chapter describes a specific video connectivity topic and links to free reference designs in Verilog and VHDL, providing implementation examples.

Integrating the encoders and decoders for these standards into the FPGA is simple with the clear, concise reference material found within the chapters of XAPP514. The reference design code, offered in both Verilog and VHDL, is clearly documented and illustrated, as shown in Figure 1.

We also offer a suite of validation platforms that can quickly and easily test your video processing algorithms or verify connectivity performance. For example, you can use our new Xilinx® Virtex™-5 ML571 Serial Digital Video (SDV) board ([www.cook-tech.com](http://www.cook-tech.com)) to demonstrate or develop video connectivity with Virtex-5 FPGAs. Figure 2 shows a block diagram; Figure 3 is a photograph of the ML571 board. Many of the free reference designs linked to XAPP514's chapters were verified on the ML571 platform using broadcast industry-standard test equipment.

“The ML571 board is yet another example of how Xilinx provides customers with detailed design assistance for real broadcast industry issues,” said Andy DeBaets, senior director, systems and application engineering at Xilinx. “This

board demonstrates how engineers can easily implement advanced video networking protocols while greatly increasing system integration, reducing system costs, lowering power, and shortening design schedules.”

Talk to your Xilinx sales channel about seeing the demonstrations or obtaining one of these boards so that you can test your new algorithms long before your proprietary board is produced. We hope you find this article and the audio/video connectivity book valuable, but it represents just a small sample of the information available about designing with Xilinx programmable logic devices. To access the latest information on these subjects and more, visit [www.xilinx.com/esp/broadcast](http://www.xilinx.com/esp/broadcast).

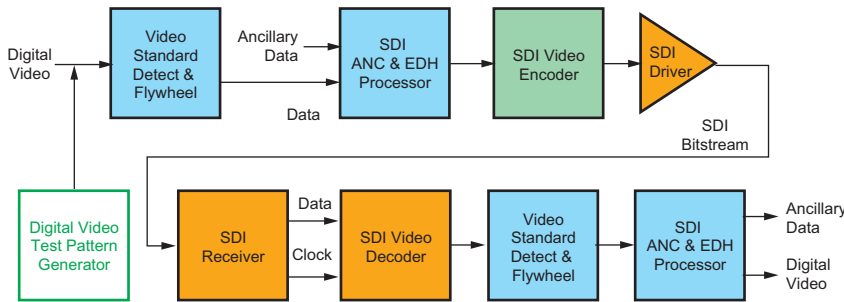


Figure 1 – Example block diagram of free modular Verilog and VHDL reference designs

**Virtex-5 Features Support Broadcast Designs**

The Virtex-5 feature set supports many aspects of broadcast solutions by providing high performance, flexibility, and scalability with unique, cost-optimized family members built on the following features:

- High-density, high-speed, reprogrammable ExpressFabric™ technology
- 550-MHz, 36-Kb, dual-port block RAM/FIFO
- 550-MHz, 25 x 18 DSP48E slice
- 550-MHz clock management tile (CMT)
- SelectIO™ technology
- Reduced power consumption
- Sparse chevron package

These features are described throughout the articles in this issue of *Xcell Journal*, with detailed descriptions of the features and performance at [www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/index.htm](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/index.htm).

**Overview of the Xilinx ML571**

The new serial digital video (SDV) board for demonstrating and testing high-bandwidth video communications channels based on Xilinx Virtex-5 platform FPGAs shows you how to easily implement high-speed serial interfaces to popular industry standards like HD-SDI.

**Standards and Functionality Supported**

The diffused silicon integration of high-performance and low-power multi-gigabit serial I/O, tri-mode Ethernet MACs, PowerPC™ processor, and PCI Express Endpoint block

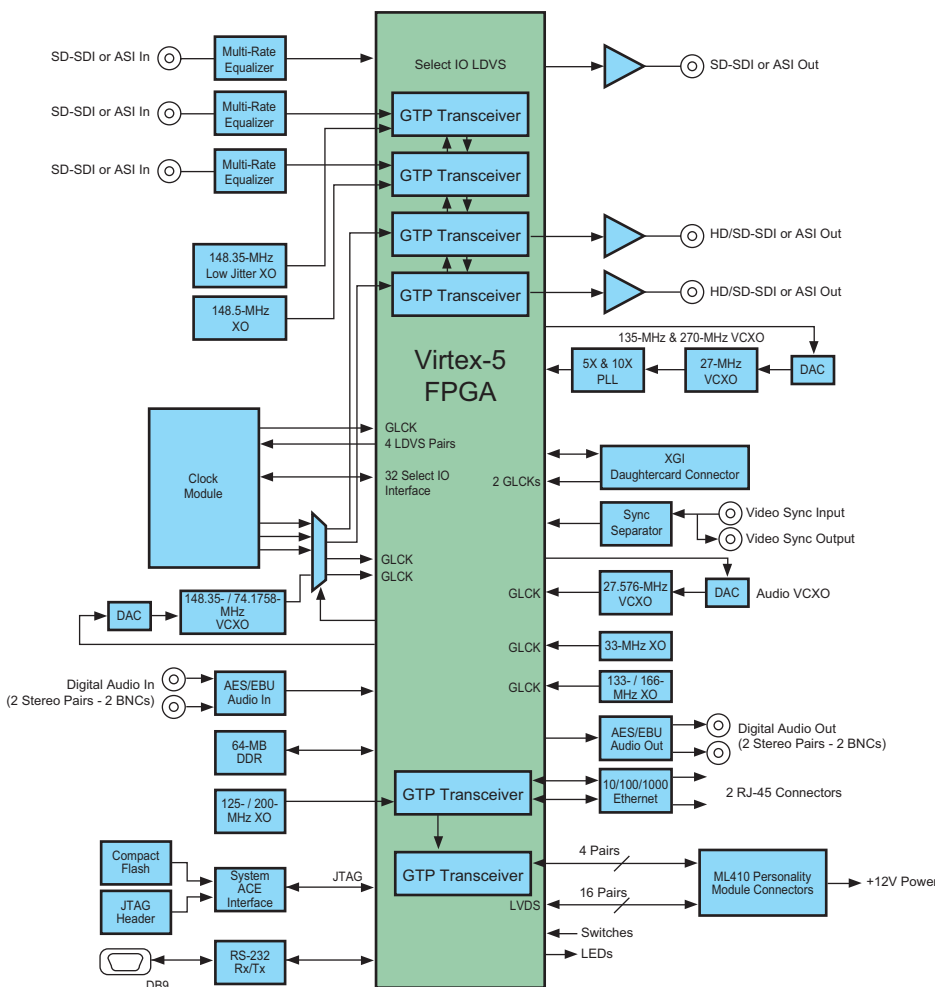


Figure 2 – Xilinx ML571 SDV video connectivity board block diagram

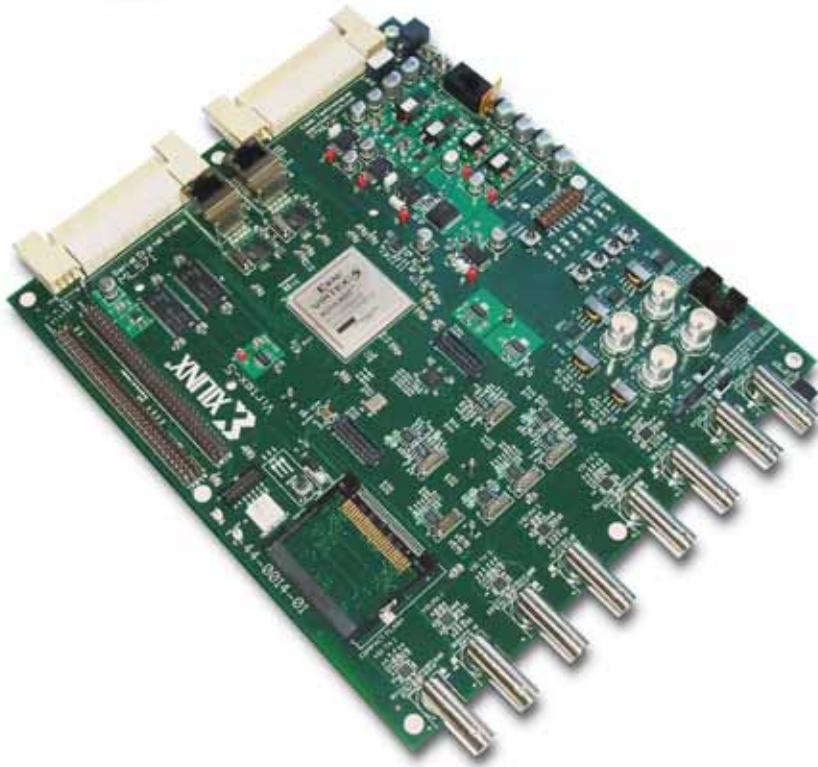


Figure 3 – Xilinx ML571 SDV video connectivity board

into Virtex-5 platforms has enabled the support of many more networking standards than previously possible.

The ML571 board now supports:

- Virtex-5 XC5VLX50T-FF1136 FPGAs (LX110T offered in a pin-compatible package)
- Two RocketIO™ GTP HD/SD-SDI receivers and two RocketIO GTP transmitters. The transmitters have Gennum tri-mode, 3 Gbps-capable cable drivers and the receivers have Gennum tri-mode, 3 Gbps-capable receiver equalizers. The standards supported are:
  - 3 Gbps HD-SDI (SMPTE424M), 2.97 Gbps
  - HD-SDI dual link (SMPTE372M) 1.485 Gbps, 1.4835 Gbps
  - HD-SDI (SMPTE292M) 1.485 Gbps, 1.4835 Gbps
  - SD-SDI (SMPTE 259M), 270 Mbps

- DVB-ASI (CENELEC EN 50083-9 Annex B), 270 Mbps
- A SelectIO video input and video output providing differential LVDS I/O. This demonstrates the ability of the Virtex-5 SelectIO interface to transmit and receive video bitstreams supporting the following video standards:
  - SD-SDI (SMPTE 259M), 270 Mbps
  - DVB-ASI, 270 Mbps
- Select IO technology, LVDS, AES3 digital audio (AES3id) I/O. Two BNC input connectors provide two stereo pairs of AES3id digital audio in. Two BNC output connectors provide two stereo pairs of AES3id digital audio out. These inputs meet the SMPTE 276M 75-Ohm unbalanced AES3 audio input electrical specifications.
- SDI AES digital audio, embed and de-embed (SMPTE272M-2004)
- AES digital audio, high-performance, asynchronous sample-rate conversion (ASRC)

- DVB-ASI to/from Ethernet for video over IP
- Frame synchronization using external DDR DRAM
- Sync separator and genlock capability. A sync separator can accept a variety of video sync sources including bi-level and tri-level video sync (HD and SD). The separated sync signals from the sync separator go to the FPGA, where they can be used to build genlock PLLs using any of the VCXO clock sources available to the FPGA.
- An XGI-compatible expansion connector set is provided to allow video I/O daughtercards
- Two 10/100/1000 Ethernet interfaces
- Debug RS-232 serial port
- Configuration six-pin JTAG header for connection to a Xilinx download cable
- Xilinx System ACE™ configuration controller with a CompactFlash Type II socket

**Conclusion**

The need to support new AVB designs and assist you, our customers, with implementations in Xilinx FPGAs is a tremendous challenge. However, at Xilinx, we pride ourselves in striving to keep up with the demand for excellence. With varying protocols and a variety of different system interfaces, it is easy to see how these designs require high-performance, cost-effective flexibility that ASSPs and ASICs cannot offer. These challenges open up opportunities for Virtex-5 devices, for these devices can enable you to provide solutions to the ever-evolving AVB equipment landscape.

The ML571 board is designed and sold by Cook Technologies. The Cook Technologies part number for the ML571 is CTXIL406. There are many clock and connectivity option daughtercards that also plug into the ML571 SDV board. For more information, e-mail [colin@cook-tech.com](mailto:colin@cook-tech.com) or visit their website at [www.cook-tech.com](http://www.cook-tech.com).