

Micron Memory Interface

RLDRAM offers a complete low-latency memory interface for networking and communication solutions.

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The increased bandwidth requirements of high-speed networking systems are pushing DRAM to perform at SRAM speeds and latencies. Micron's reduced-latency DRAM (RLDRAM) II memory addresses this need with additional densities not available in SRAM memories. Combining this memory technology with the Xilinx® Virtex™-5 device provides an excellent high-density, high-speed, low-latency solution for the networking and packet buffer applications of current and future platforms.

RLDRAM II Memory Features

RLDRAM II memory uses an eight-bank architecture optimized for high-speed operation and a double-data-rate (DDR) I/O for increased bandwidth. The eight-bank architecture enables RLDRAM II memory devices to achieve peak bandwidth by decreasing the probability of random access conflicts. Although bank management remains important with RLDRAM II memory architectures, one bank is always available for use even in the worst case (burst of two at 533-MHz operation).

One of the key features added in the RLD RAM II memory architecture is reduced row cycle latency time. Row cycle latency (tRC) is the amount of time that must elapse before a recently accessed bank can be accessed again. Table 1 shows a direct comparison between RLD RAM II memory, DDR2, and DDR at device densities of 576 Mb, 512 Mb, and 512 Mb, respectively.

Latency	RLDRAM II Memory	DDR2	DDR1	Units
tRC	15	55	55	ns

Table 1 – Row cycle time DRAM comparison

I/O Options

RLDRAM II memory offers separate I/O (SIO) and common I/O (CIO) options. The SIO devices have separate read and write ports to eliminate bus turnaround cycles and contention. CIO devices have a shared read/write port that requires one additional cycle to turn the bus around. RLD RAM II memory CIO architecture is optimized for data streaming, where the near-term bus operation is either 100% read or 100% write, independent of the long-term balance.

Figure 1 illustrates the performance variations between the versions at different read-to-write ratios. The reduced latency and eight-bank architecture achievable with RLD RAM II memory allow faster random access from the memory array, increasing sustainable bus utilization.

SRAM-Style Interface

The command bus protocol used in RLD RAM memory is a bit simpler than other DRAM devices. RLD RAM II memory incorporates an SRAM-style interface with read and write commands, replacing the activate and precharge commands used in DDR2 and other similar computer-based memory technologies. This reduction of commands frees up the command bus, helping reduce dead cycles during short burst lengths.

Additional Features

for RLD RAM II Memory

RLDRAM II memory also deviates from the refresh requirements of current DRAM technologies. Because ordinary DRAM devices refresh a row in all banks, they require dead clock cycles on the bus after a refresh command. This requires a period of inactivity on the DQ bus, typically 66 ns.

RLDRAM II memory devices have incorporated a bank-based refresh scheme to hide the refresh recovery periods required by other DRAM technologies. The refresh process for RLD RAM memory requires the bank address of the bank that needs to be refreshed, still allowing bus activity during

error-correcting schemes used to eliminate soft errors in the memory channel. RLD RAM II memory is the first DRAM-based technology to add the ECC DQ pins to the devices. RLD RAM II memory is offered in x9, x18, and x36 configurations to provide a single-chip ECC solution without adding unwanted components, reducing board layout space.

Manufacturability in large-component-count systems is a major problem, but it has been ignored in the DRAM industry, largely because the applications that use commodity DRAM devices do not need continuity testing. The module-based business uses so few components that the extra

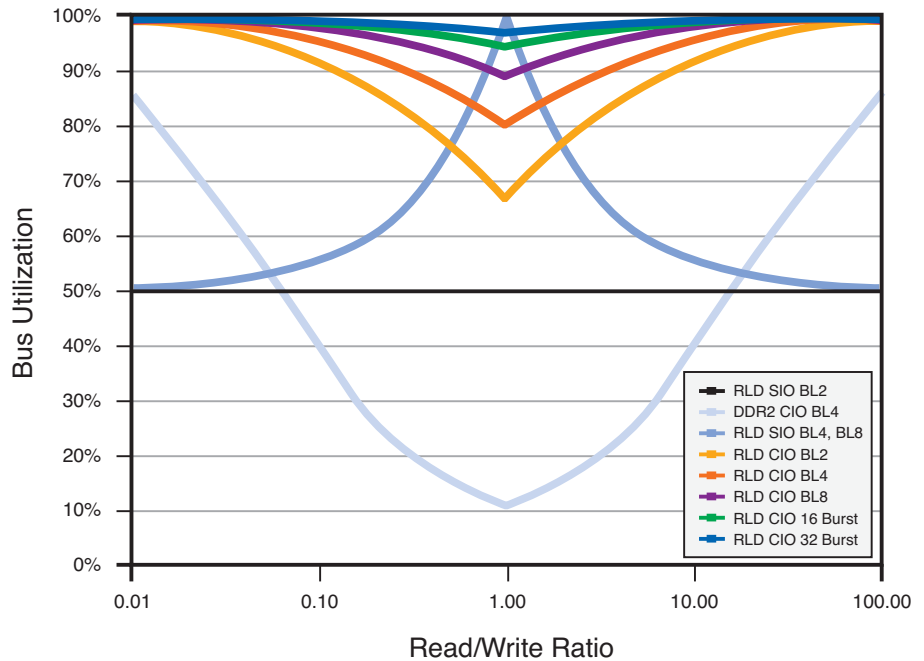


Figure 1 – Peak bandwidth comparison with different DRAM technologies

the refresh process and eliminating the dead time seen in other DRAM technologies. Bank-dependent refresh helps increase the percentage of bus utilization, increasing the overall bandwidth of the system using the Virtex-5 device.

Computer-based memory technologies such as DDR2 have relied on modules to support error-correcting code (ECC) technologies to remedy soft errors in the transition of data from the processor to the DRAM. Multiple parts are placed on the DIMM, adding extra data lines for the

pins are not desirable for JTAG support. Also, discarding manufacturing errors is less expensive than repairing them in small component-based systems.

The target market for RLD RAM memory is an entirely different scenario. Systems based on RLD RAM memory are typically point-to-point applications, where the DRAM is soldered directly to the main board alongside countless other components. Placing all of these components can be a manufacturing challenge. To address this issue, RLD RAM II memory

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incorporates JTAG continuity technology, which helps with manufacturing issues in the large system-based boards used in the networking and communication industry.

The density requirements of today's applications have presented a challenge for SRAM systems. The memory cell for SRAM memory devices is approximately five times larger than a DRAM memory cell. Figure 2 shows a comparison of the two memory technologies. The DRAM memory cell is substantially smaller, allowing for significantly higher density memory subsystems that still approach SRAM latency speeds.

In the first quarter of 2007, Micron is introducing a 576-Mb RLD RAM II memory device compatible with the high-volume 288-Mb RLD RAM memory device. The 576-Mb device will be offered in multiple configurations that are pin-for-pin compatible, but will have additional address pins to accommodate the higher density. RLD RAM II memory offers one of the highest density, lowest latency DRAM-based solutions available on the market today.

Additional I/O Interface Options

The RLD RAM II memory I/O interface provides other features and options, including support for both 1.5V and 1.8V I/O levels and a programmable output impedance driver that enables compatibility with both HSTL and SSTL I/O schemes.

RLDRAM II memory requires an external one-percent precision resistor (RQ) tied to VSS in order to calibrate the driver to a known value and eliminate the process variation that can be introduced during manufacturing. The calibration process requires the external resistor to operate at five times the desired driver impedance. The programmable impedance control (PIC) circuit calibrates the output impedance to the desired value, eliminating vari-

ation introduced during the manufacturing process. Updates are made continuously during device operation without interrupting data transfer, ensuring consistent operation of the RLD RAM memory system independent of temperature and voltage.

Micron's RLD RAM II memory is also equipped with on-die termination (ODT) to enable more stable operation at high speeds without the use of an external ter-

mination resistor. ODT provides simplicity and flexibility for high-speed designs by bringing termination resistors on-die, eliminating some of the on-board termination.

Conclusion

RLDRAM II memory combines several performance-critical features to provide flexibility and simplicity for a wide range of high-speed applications. The speed and latency requirements for high-speed appli-

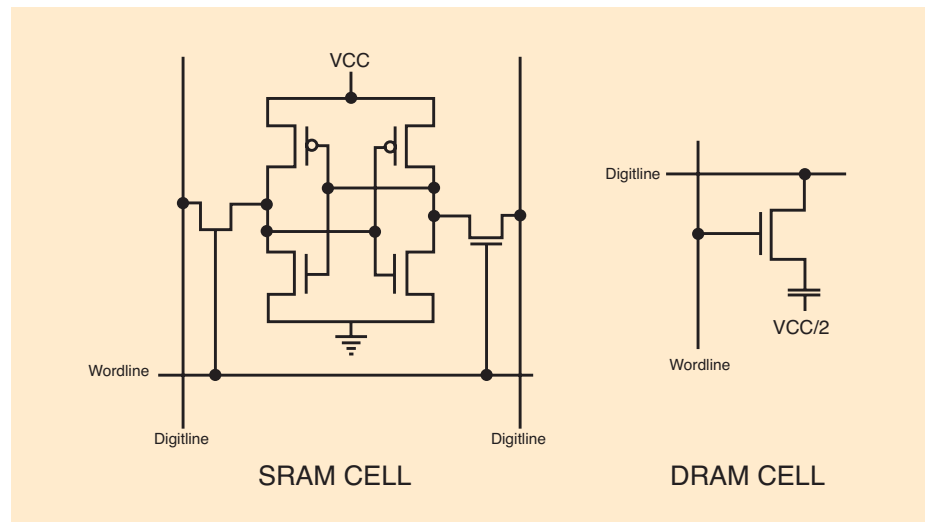


Figure 2 – SRAM cell compared to a DRAM cell

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At high-frequency operation, however, it is important you analyze the signal driver, receiver, printed circuit board network, and terminations to obtain good signal integrity and the best possible voltage and timing margins. Without proper terminations, the system can suffer from excessive signal attenuation, leading to reduced voltage and timing margins. This, in turn, can lead to marginal designs and cause random soft errors that are difficult to debug. Micron's RLD RAM II memory

cations continue to grow, demanding new and more innovative solutions to meet market requirements. As RLD RAM II memory helps address current market requirements, the demand continues for increased performance. Micron will address this demand with future low-latency devices such as RLD RAM III memory.

Micron continues to innovate and deliver solutions to meet the needs of today's and tomorrow's markets. The joint efforts of Micron and Xilinx help enable our customers to quickly deliver next-generation networking, video, and imaging systems.

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