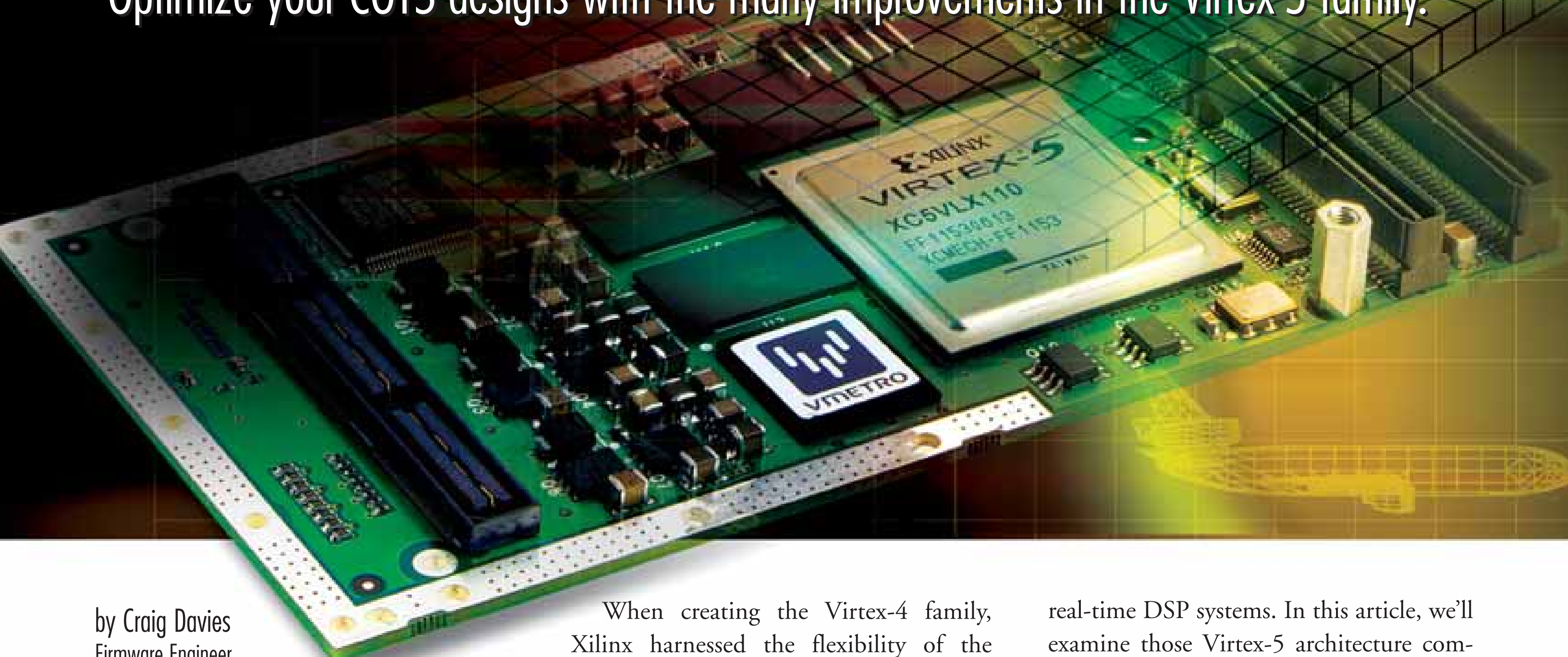
Using Virtex-5 FPGAs in COTS Board-Level Products

Optimize your COTS designs with the many improvements in the Virtex-5 family.



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In the fast-paced world of FPGA development, Xilinx has struck again with its second-generation ASMBL™ architecture devices, the Virtex™-5 family. This device family has many upgrades from its predecessor, the Virtex-4 family, and likewise continues the evolution of the ASMBL architecture, with scalable FPGAs catering to the application-specific marketplace. For commercial off-the-shelf (COTS) developers, this means a platform that is low cost, light on power consumption, and optimized for high performance.

When creating the Virtex-4 family, Xilinx harnessed the flexibility of the ASMBL architecture to build the first multi-platform FPGA family. Xilinx continues this approach with the Virtex-5 family. The initial offering is the Virtex-5 LX platform, optimized for high-performance logic.

Seasoned FPGA users expect new FPGA generations to deliver more and the Virtex-5 family certainly delivers, all while consuming less power. Compared to Virtex-4 LX devices, Virtex-5 LX FPGAs offer:

- 65% higher logic capacity with as many as 330,000 logic cells
- 70% more block RAM
- 100% more DSP slices
- 25% more SelectIO™ pins

For COTS board vendors, these features enable powerful products capable of handling the very high data rates and processing complexity required of modern real-time DSP systems. In this article, we'll examine those Virtex-5 architecture components that enable COTS designers to deliver more bang for the buck.

COTS FPGA Backgrounder

Freed from the need to design hardware and IP from scratch, COTS board-level users can focus their energies on implementing their specialist algorithms. COTS products incorporating user-programmable FPGAs target a variety of applications, from simple customizable digital I/O to RADAR, video, and signals intelligence (SigInt).

Typically, the FPGA requires hardware connections to a real-world data source or destination, plus a standardized interface to a host processor. COTS products must usually follow an industry-standard form factor (such as PMC, VME, VXS, and CompactPCI), enabling end users to integrate products from a range of vendors.

With its parallel architecture and high-speed I/O capabilities, the Virtex-5 FPGA is capable of streaming and processing data at the gigabyte-per-second rates typically required for today's applications. It is well suited to algorithms where a core "inner loop" can be parallelized to speed up operation, employing the resources available in modern devices. Many DSP algorithms dovetail with this architecture. Conversely, even the fastest CPUs cannot easily process data at gigabyte-per-second rates; they are, however, well suited to decision making and user interaction tasks.

Given these trade-offs, FPGA-based DSP systems often employ a hybrid approach, as illustrated in Figure 1. Here, a wide-bandwidth RADAR or video source is digitized at gigasample-per-second rates and fed to an FPGA. The FPGA performs some heavy-duty number crunching to eliminate unwanted data, focusing in on the key area of interest. Pre-processed data is fed at a more manageable rate to a general-purpose CPU for post-processing control and display.

Key COTS FPGA board requirements are:

- Large, reconfigurable FPGAs with ample room for customer-programmable application logic
- Regular air-cooled and rugged conduction-cooled options
- High-speed interface for efficient transfers to and from a host processor
- Flexible, fast I/O to and from a variety of real-world interfaces
- Local memory interfaced directly to the FPGA for I/O buffering as well as temporary storage during algorithm operation
- Wide range of I/O and signal-processing IP cores to speed end-user development cycle times
- Flexible FPGA development tools covering both budget-conscious and extreme-performance users
- Debugging interface capable of in-FPGA logic analysis
- Comprehensive board support firmware and software

With a proven track record in the high-end FPGA DSP arena and comprehensive tool and IP support from a variety of sources, the Virtex-5 FPGA family is a natural choice for COTS board-level vendors.

Optimization of Soft Components

A great addition to the Virtex-5 architecture is the replacement of traditional four-input look-up tables (LUTs) with new six-input LUTs (6-LUTs) for more efficient mapping of wider functions. Because 6-LUTs are also configurable as dual five-input LUTs, design software tools can achieve greater efficiency in logic mapping when six-input functions are not required.

Most FPGA devices these days base their soft fabric components – those components configured to implement logic equations – on LUTs. Previously, the common choice was the four-input LUT, as this was a nice binary base and was relatively easy to work with for optimizing a logic function. A given equation can be optimized to contain a sum of products of four inputs. For many of today's applications, especially those in DSP, this optimization reduces significantly as system-level algorithms increase in complexity.

Configurable logic block storage density improvements increase the shift register LUT (SRL) length from 16 bits to 32 bits (SRL32), while retaining a dual SRL16 option. Distributed RAM now offers a 64-bit option, up from 16 bits. With improved reduced-hop routing and more logic per slice (four LUTs/four flip-flops versus two LUTs/two flip-flops), speed improvements of as much as 45% are possible.

Improved FIR Efficiency

Let's consider a finite impulse response filter implemented in distributed logic. Distributed arithmetic filters are often selected because their operating frequency is not tied to the length of the tap vector. This characteristic is highly desirable because increasing the tap vector length is fundamental to improving the overall filter response. However, these types of filters are

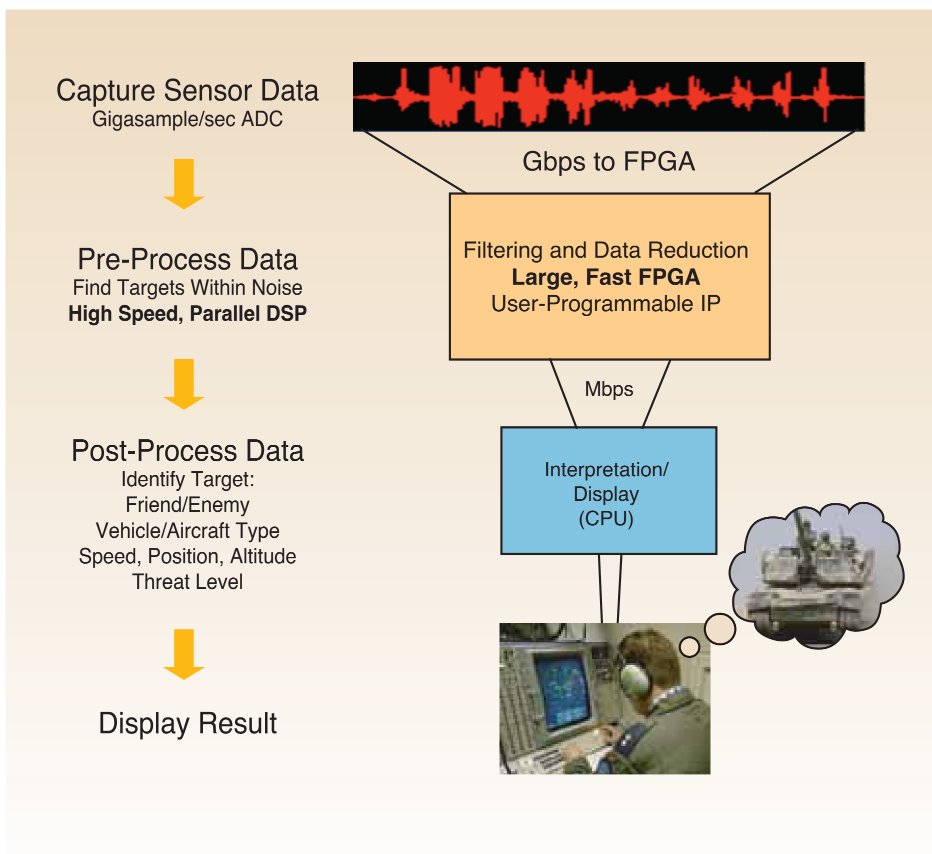

Figure 1 – Processing chain

serial in nature; most applications need valid output at a marginally decimated rate with respect to the sampling frequency. Thus, a fully parallel architecture is required.

Parallel Distributed Arithmetic FIR filters (DAFIRs) utilize significantly more logic versus other FIR implementations to perform the many partial products on a clock-to-clock basis (even when decimating the sampling rate). In the distributed arithmetic architecture, a corresponding output product y(n) is produced by summing the products of a time-delayed series of input x(n) and coefficients a(m), where m, an integer between 1 and N, is the filter length.

For the sake of simplicity, let's say that each tap or filter coefficient is two bits wide and that the input vector is six bits. In total, our filter is 96 taps in length. If we calculate this product using the partial products method, we need 6 x 2 partial products using four-input LUTs. Each LUT is capable of a 2 x 2 multiplication, which means using three 4-input LUTs. Using 6-LUTs, we can reduce this to just two LUTs. For 96 taps, we have saved 96 LUTs of a possible total of 288. This is just the savings when producing the partial product.

LUTs and SRLs are also used for shift registers in the input delay pipe and for the scaling accumulator responsible for summation and normalization of the output. Expanding our example input and tap widths to a more applicable precision of 16 bits increases the depth of our partial product multiplication tree, requiring even more LUTs. Using 6-LUTs as opposed to four-input LUTs results in a LUT logic reduction of more than 33%.

Wider LUTs Improve Efficiency and Speed

Switched fabric developers will also benefit from the 6-LUTs, as these are often used to implement multiplexers. 6-LUTs mean a reduction in the overall depth of a logic equation. For implementing multiplexers, this means an effective increase in speed for an equivalent multiplexer implemented using 6-LUTs, as opposed to four-input LUTs.

Depending on the application, changing to 6-LUTs can make as much as a 1.6x improvement in logic utilization over previous generations of the Virtex device family.

Multiplying Computational Power

Not to be outdone by the soft-logic components, the hard-logic dedicated multipliers have also been optimized for the Virtex-5 FPGA. The 18 x 18-bit multipliers present in the Virtex-II and Virtex-4 families have been upgraded to 25 x 18-bit multipliers in the new family. Application developers who implement beam-forming arrays or other advanced computations will benefit from this enhancement.

Large multiplication arrays that require a high degree of precision traditionally required a large tree structure of multipliers. As output is carried between intermediary stages of a large multiplication, the maximum allowable output value increases with each subsequent stage. To handle this bit-width increase, typical solutions involve a precision reduction by truncation or some other intelligent scheme such as convergent rounding or (less often) by breaking down the multiplication into smaller stages and then rebuilding the final product by summation. Utilizing 25 x 18-bit multipliers, more precision is carried through intermediary stages of a multiplication and thus reduces the impact of intermediary truncation/rounding errors while improving on overall speed and minimizing pipeline latency.

Suppose convergent rounding is employed to reduce the precision at each stage of multiplication within an FFT. If we implement an 8K FFT using a mixed-radix base of radix-4 and radix-2, that gives us six radix-4 butterfly stages and one radix-2 butterfly stage. In an FFT, at each subsequent stage we perform calculations that produce partial products. These outputs are fed into the multipliers of the next stage until the time-domain data is transformed completely to the frequency domain. However, each stage must employ a scheme to reduce the precision of the output so that subsequent stages can accept them as inputs. After each stage of multiplication, scaling is employed to reduce the precision. Each stage of scaling introduces quantization errors.

But what if more precision is carried into the input side of each butterfly stage? Using 25 x 18-bit multipliers, we can carry more precision from our partial products when multiplying them to new sample data and in turn introduce less rounding errors into our results.

Improved Source-Synchronous Memory Access

Much to the delight of many designers using Virtex-4 FPGAs, Xilinx introduced a primitive called IDELAY capable of synchronizing data and strobes to a source clock off the FPGA. This feature meant that high-speed DDR and DDR2 SDRAM and QDR and QDR II SRAM memories could be accessed through controllers inside the Virtex-4 device at high data rates.

COTS developers are increasingly finding applications that require fast and deep onboard memory. For example, data recording applications benefit greatly from fast onboard memory to implement the sizeable buffers needed to sustain high-speed data transfers over PCI/PCI-X buses. Video processing applications also require large, fast external memories to store the very-high-resolution, high-frame-rate images produced by today's leading camera equipment.

The introduction of the IDELAY primitive also benefits ruggedized application developers, as the IDELAY taps can be constantly monitored by logic to perform runtime resynchronization to the source clock; this technique is known as dynamic clock-to-data centering.

Now, with the Virtex-5 family, Xilinx has expanded the primitive to add ODELAY, enabling delay control on both input and output signals. The key component of the IDELAY primitive is to delay the input data relative to the clock such that the internal FPGA version of the source clock edge is centered with the input data. The ODELAY enables variable delays per output data line to better match trace-length differences.

Improving High-Speed I/O Communication

As the COTS marketplace moves more and more into high-speed serial implementations, clock and data recovery techniques become more in demand. When implementing general-purpose high-speed serial links, transmission errors and data loss become a reality, especially when targeting data rates beyond 1 Gbps.

For developers using previous generations of Virtex devices, the choices for clock and data recovery (CDR) implementation to de-serialize incoming streams without using multi-gigabit transceivers (MGTs) were limited. Although the delay-locked loops (DLLs) used for clock generation in previous families are very stable in nature because of their first-order loop architecture and digital implementation, they are not able to filter input jitter or handle phase alignment beyond their discrete range.

With the phase-locked loop (PLL) blocks introduced with Virtex-5 family, jitter reduction is an intrinsic feature, resulting in large improvements in higher data-rate sustainability. Filtering input jitter to produce stable internal versions of source clocks is critically important to correctly sample and store incoming data at the FPGA I/O boundary. Using these new blocks, implementing SERDES components using regular SelectIO pins becomes practical even at 1 Gbps and above.

Together with SelectIO performance of as much as 800 Mbps per pin single-ended and 1.25 Gbps differential, the Virtex-5 device is able to input, process, and output the high data rates generated by current real-world interfaces. For example, interfacing directly with ADCs and DACs running in the gigasample-per-second range is now perfectly feasible.

Looking to the future, new high-speed serial fabric interfaces will be a natural fit for interfacing between FPGAs, external devices, and host systems.

65-nm Copper CMOS

COTS developers will greatly benefit from the move into the 65-nm copper CMOS process. One of the consequences of process shrinks is that density and performance increase with the next generation. This is true in the case of the Virtex-5 LX platform, which has increased the amount of CLBs by 65% over the Virtex-4 LX platform, block RAM by 70%, DSP slices by 100%, and SelectIO pins by 25%.

Figure 2 – VMETRO PMC-FPGA05

Figure 3 – Standard PCI option

With increased logic density in the overall package, power consumption has been reduced significantly. While the Virtex-4 FPGA operates at 1.2V core voltage, the Virtex-5 FPGA improves power efficiency with a core voltage of 1.0V. You can achieve further power savings by optimizing the soft and hard components, such as the 6-LUTs and 25 x 18-bit multipliers.

When implementing large designs – such as in software-defined radio (SDR) applications where multi-channel digital filters consume significant CLB space – the dynamic power dissipation is quite high because of the large amount of switching activity that occurs. This is in part caused by the extensive signal routing required to implement these designs. With the new components in the Virtex-5 family, existing designs implement in a smaller number of primitives, reducing the overall switching activity. In addition, the Virtex-5 architecture includes the enhancement of diagonally symmetric routing for more efficient design implementation.

COTS developers often complain about violating power specifications when developing mezzanine cards in existing designs. With the Virtex-5 device, their mezzanine cards will be less power-hungry and more desirable to end users. In other words: less power required, simplified cooling, and greater reliability.

COTS products are often employed in environments where power consumption is a significant challenge – for example, high ambient temperatures may limit a cooling system's effectiveness, so reducing heat output is an important motivation. Other applications such as unmanned airborne vehicles (UAVs) have limited electrical power availability, so using every Watt available effectively is of paramount importance.

The VMETRO PMC-FPGA05

A good example of a current COTS product implementing the advanced Virtex-5 65-nm technology is the VMETRO PMC-FPGA05, a general-purpose high-end FPGA PCI mezzanine card (PMC) pictured in Figures 2 and 3 and illustrated in the block diagram shown in Figure 4.

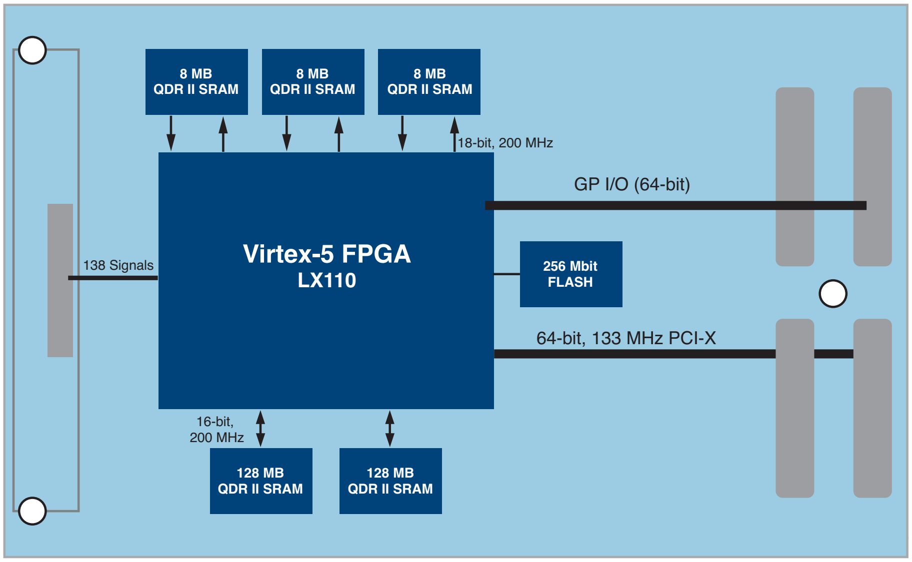

Figure 4 – PMC-FPGA05 block diagram

A Virtex-5 FPGA at the heart of a PMC-FPGA05 means that it is a highly integrated design. There is no need for external bridges and controllers because the Virtex-5 device is more than capable of handling these functions directly (see Figure 5) while using only a small amount of resources. This leaves plenty of space in the PMC-FPGA05 to include IP such as digital receivers, FFTs, or other DSP functions.

Implementing Flash and PCI-X interfaces inside the FPGA introduces some design challenges. How is the FPGA configured and debugged without these interfaces already in place – especially if the IP is complex? This is where the ChipScope™ Pro Analyzer (version 8.2) comes in – it embeds a logic analyzer inside the FPGA and connects the user interface to the FPGA through JTAG. It provides a debugging portal into the FPGA that can be inserted through HDL entry.

Once built, a ChipScope Pro ILA (integrated logic analyzer) port assignment can be changed in FPGA Editor. Therefore, changes to the ILA do not require another full run through the ISE™ flow when debugging, as shown in Figure 6. Instead, you can make changes at the map stage of the design flow, reducing the time between generating bitstreams and improving efficiency during the debugging cycle. The ChipScope Pro Analyzer consumes a limited amount of the FPGA's resources, though this is largely a function of the depth of the analyzer sample memory. Features such as the analyzer memory depth and triggering functions are parameterizable through the ChipScope Pro inserter tool, eliminating unnecessary resource waste.

The ChipScope Pro Analyzer is a valuable asset when debugging designs such as the VMETRO PMC-FPGA05. The PCI-X interface in particular represents a challenge. In simple terms, this might be to power up the PCI bus, configure the IP onto the FPGA, and re-initialize the PCI bus to detect the FPGA's PCI controller. This low-level development requires a tool like the ChipScope Pro Analyzer to reduce the number of bus initialization cycles. Without the ChipScope Pro tool, debugging would require a sophisticated bus analyzer – and even then the internal FPGA functionality would be inaccessible. Utilizing the ChipScope Pro Analyzer saves the design team considerable time by reducing the number of iterations required to debug the PCI-X interface.

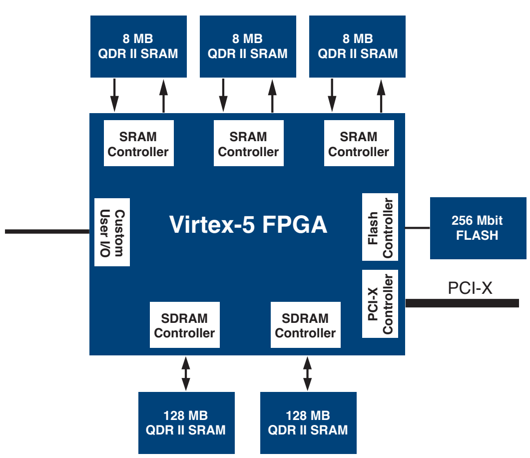

Figure 5 – PMC-FPGA05 controller IP components

The ChipScope Pro tool is not only useful for VMETRO board development, but also for customers integrating their IP and external interfaces. We designed the PMC-FPGA05 with a high-density parallel interface that you can use with a range of I/O modules including analog I/O, RS485, LVDS, FPDP, and Camera Link. Using the ChipScope Pro Analyzer makes these interesting projects manageable.

The PMC-FPGA05 also offers application developers a platform that can sustain high-bandwidth data transfers and implement sophisticated DSP and processing algorithms at a fraction of the power of previous generations.

FPGA Resources

More than any other FPGA family, the Virtex series leads the way in IP availability. Through the Xilinx® Alliance Program, IP is available from both Xilinx directly as well as third-party IP suppliers. With a strong worldwide network of IP vendors accessible directly from *www.xilinx.com*, COTS FPGA board users can choose IP cores from suppliers experienced with as many as five generations of the Virtex family. This is key to success when developing projects to aggressive timescales, and therefore is a high-priority reason for selecting the Virtex-5 family.

FPGA Firmware Development Process

With the Xilinx ISE tool chain offering an easy-to-use GUI development environment and an included VHDL/Verilog synthesis tool (XST), many end users need only purchase ISE software for a complete cost-

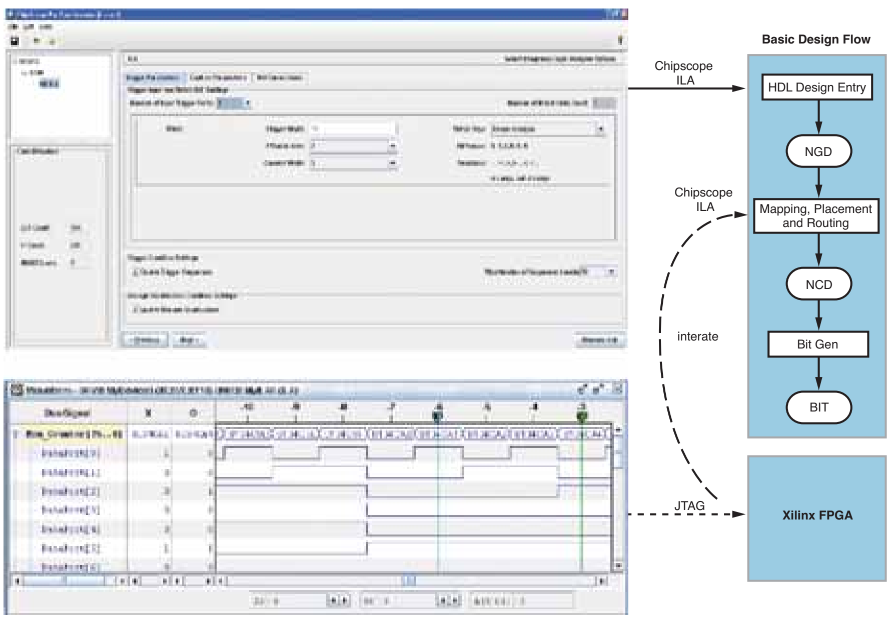

Figure 6 – ChipScope debugging cycle

effective development solution. Those implementing the most complex algorithms may benefit from high-end synthesis tools from third-party vendors. These integrate directly with ISE software to maintain a simple project management process.

Simulation may not reveal all errors in the design, particularly for complex projects. When an implementation does not function as expected, you must connect up to the actual hardware to see what is going on. But with dense packaging covering many thousands of pins, there's no practical way to connect a traditional logic analyzer.

VMETRO engineers have many years of experience developing firmware for Xilinx FPGAs. Using ISE software as the primary synthesis/place and route tool, Model Technology's ModelSim PE for simulation, and the ChipScope Pro tool for in-circuit debugging, VMETRO developed the IP necessary for interfacing with the board hardware. This includes interfaces for the SRAM and SDRAM memory devices, to which users simply connect their address and data signals, and a high-performance bus mastering PCI-X interface core supporting customizable registers and simple FIFO-based DMA transfers for streaming data.

Another good reason to choose the Virtex-5 family is a commitment to education and support: from introductory courses in VHDL to DSP logic design courses to development laboratories equipped with the latest gear for testing high-speed serial interfaces, Xilinx offers the resources necessary for successful FPGA deployment.

As the Virtex-5 device is brand new, the PMC-FPGA05 is still in development. Stay tuned for an update on the challenges, solutions, and lessons learned as VMETRO works hard to bring you the world's first Virtex-5 COTS product.

Conclusion

To meet the growing demands being placed on the COTS marketplace, you must adapt and implement platforms with the right tools for the application. Today, this means integrating high-speed serial communication, fast access memory, and plenty of optimized logic space for advanced algorithm development. Equally important are efficient development and debug tools, IP resources, and a commitment to high-speed DSP development.

The highest logic density available, the lowest power consumption, and the best performance are what COTS developers need to meet the needs of their customers. Virtex-5 FPGAs, with their ASMBL architecture and 65-nm process, deliver on these demands.