

Virtex-5 Configuration Options Offer Designers a Choice

Xilinx provides a host of flexible choices in configuration memory to help you make the best decision for your design.

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System designers are always making trade-offs between alternative requirements. Considerations include time to market, ease of use, total ownership cost, and system speed.

Every alternative offers different total-cost-of-ownership (TCO) considerations that you should examine when designing a configuration system, including design time, prototyping, manufacturing and test costs, and the per-bit costs of the configuration device. The trade-offs of all these factors should enter into your decision of which configuration method to use.

Designers using Xilinx® Virtex™-5 devices have many additional choices for configuring the new FPGA family, including new configuration modes built right into the chips; support for 32-bit-wide high-performance parallel SelectMAP, which offers the ultimate in speed; and both BPI (byte parallel interface) and SPI (serial peripheral interface) using industry-standard SPI and parallel flash memory devices (see Figure 1). The easy-to-use, full-featured, configuration-engineered Platform Flash PROMs offer a pre-engineered way to flexibly configure Virtex-5 devices and manage multiple bitstreams.

Platform Flash PROMs

Dropping a Platform Flash PROM into a design provides a seamless solution with a low TCO, including minimum board space, high configuration speed, a guaranteed source of supply, and value-added features like bitstream de-compression, design revision management, JTAG Boundary Scan for



Figure 1 – Virtex-5 configuration modes

test and configuration, and additional storage for boot and scratch-pad memory.

Platform Flash features on-board decompression that can result in as much as 50% more configuration data into the same overall memory space. Design revisioning allows you to switch between memory blocks for various configurations: for instance, using the board and system in different geographical regions or loading a diagnostic followed by a mission load of configuration. In addition, unused Platform Flash memory can be allocated to boot code or scratch-pad memory. Both of these features work without any additional glue logic or special software. The Boundary Scan JTAG port enables configuration and includes the Platform Flash in overall board tests.

SPI Flash PROMs

Virtex-5 FPGAs support direct connection to SPI PROMs using the industry-standard four-wire SPI interface. Many systems currently use SPI PROMs; you can now easily take advantage of the on-board SPI PROM without any additional circuitry or software. Designers should think about design trade-offs, including different features offered by SPI PROM manufacturers and the slower configuration speed compared to parallel SelectMAP, Platform Flash, and BPI.

BPI Flash PROMs

Virtex-5 devices include on-board circuitry to directly connect – without any additional glue logic or software – to industry-standard parallel flash devices. The parallel flash interface can be directly connected to the FPGA and the memory shared by the system bus.

Conclusion

Virtex-5 FPGAs offer you the widest variety of configuration alternatives in the industry, including Platform Flash, 32-bit SelectMAP, and interfaces that directly connect to SPI and BPI PROM devices. You should understand these alternatives and make an informed decision on which one meets your needs based on the trade-offs between speed, complexity, and features.

For more information, please see Xilinx Application Note 483, “Multiple-Boot with Platform Flash PROMs,” at www.xilinx.com/bvdocs/appnotes/xapp483.pdf.