

# Introducing Virtex-5 EasyPath FPGAs

The world's first 65-nm FPGA cost-reduction solution.

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With increasing competition in many different market segments, many companies must drive down their product development costs while at the same time adding more and more complexity and features. In addition, companies must react to fast-changing market requirements and heightened time-to-market pressures.

Xilinx® FPGAs can help you face these challenges by continually innovating to provide increasingly complex functions at a lower cost per logic cell. The recently introduced Virtex™-5 FPGAs, in combination with Virtex-5 EasyPath™ FPGAs, are the latest generation of 65-nm devices that provide higher performance, lower system cost, and greater embedded functionality than ever before.

Virtex-5 EasyPath FPGAs are the industry's only 65-nm customer-specific FPGA cost-reduction solution, providing the lowest total cost of ownership (TCO) when compared to other solutions. EasyPath FPGAs are identical to standard Xilinx FPGA offerings but use patented testing techniques and customer-specific test patterns to significantly improve FPGA yields for designs that no longer require the full programmability of a standard FPGA. You can reap the benefits of these improved yields in the form of lower costs. EasyPath technology is available across multiple platforms, different product families, and 28 different devices over a range of gate and memory counts.

### Lowest TCO with Virtex-5 EasyPath FPGAs

Virtex-5 EasyPath FPGAs devices are manufactured using a 65-nm process, which intrinsically offers a cost advantage (see Table 1). In addition to a low unit price, EasyPath FPGAs provide many other cost advantages, such as:

- Low NRE
- No re-qualification required
- No engineering resources required
- Shorter lead times (12-16 weeks)

With Virtex-5 EasyPath FPGAs, you can realize a 30%-75% price reduction when moving to high volume as compared to standard FPGAs. EasyPath FPGAs are identical to their standard FPGA counterparts, effectively eliminating any conversion work. This has two important implications. The first is that you pay less yet incur very little risk, because every single feature in a standard FPGA is supported and will work in an EasyPath FPGA. Second, you do not need to re-qualify your boards or systems when you move to EasyPath FPGAs. This saves valuable engineering time and resources and provides cost savings of \$500K or more.

Unlike structured ASICs, where customers have to go through multiple reviews with the vendor and spend many months of valuable engineering resources, EasyPath FPGAs demand almost no resources from you. Once you have finalized the design and handed off the relevant files to Xilinx, you can get to full production directly in 8-12 weeks. No intermediate prototyping is required because the design has already been finalized (prototyped) in a standard FPGA. The lead time to get to production is at least three to four months less than with structured ASICs.

Alternatively, those of you in fast-moving markets can postpone the design freeze milestone by three to four months to better address dynamic market condi-

tions. Getting to market faster can have a significant impact on the market share a product can capture. Studies have indicated that just a three-month delay in time to market can reduce market share by as much as 15%, according to research from International Business Strategies, Inc.

Total Cost Driver	Structured ASICs	Xilinx EasyPath
Time to Cost Reduction	20 to 24 Weeks	Yes
NRE Costs	\$100K to \$400K	No
Cost of Requalification	\$100K to \$500K	Yes
Engineering Costs	\$250K to \$300K	Identical
Cost of Design Tools	\$100K to \$200K	Identical
Unit Costs	Lowest	Low
Cost of Respin	High	High

Table 1 – EasyPath total cost of ownership advantage

you must take care to reduce parasitic capacitance issues when signals are being transmitted simultaneously on adjoining metal lines.

Another major problem with 65-nm design is the issue of power consumption. Although Virtex-5 FPGAs take advantage of triple-oxide technology to reduce leakage power consumption significantly, each ASIC design must factor

in power consumption and use techniques such as clock gating and selective transistors to mitigate leakage current. So although Virtex-5 EasyPath FPGAs retain the simplicity they had at 130 nm and 90 nm, 65-nm ASICs offer unique challenges that could significantly reduce the chance of first-time success with a design.



### Difficulties with 65-nm ASICs

One of the industry trends in place for some time now is that ASIC design starts are decreasing every year. Part of the reason for this is that FPGAs have been able to provide lower unit costs for higher functionality. The other driver has been the rising cost of mask sets, design, and verification. By some recent estimates, the cost of developing a new 90-nm ASIC design is in excess of \$10 million (International Business Strategies, Inc). A significant portion of this cost occurs in the verification phase, which has become longer and longer with increases in chip complexity. At 65 nm, operating voltages and transistor sizes are so small that very small process variations can have a big effect on the functionality of a design.

What this means to you is that you must now factor in DFM (design for manufacturability) rules during the physical design phase – something previously assumed to have been embedded in the library itself. Furthermore, because the interconnects are very closely spaced, signal integrity becomes even more important;

### Conclusion

The Virtex-5 family is one of the most cost-effective, high-performance FPGA families in the industry. With advanced features such as a higher utilization logic fabric, more integrated block memory, higher precision DSP slices, as well as advanced connection and embedded processing blocks, you can reduce your overall system cost by fitting into a smaller FPGA or replacing external discrete devices on your boards. This complements the natural cost reduction that comes from fabricating devices on a 65-nm process.

Virtex-5 FPGAs are a faster time-to-market alternative to ASICs and other custom logic solutions, and enable a lower total system cost. In addition, Virtex-5 FPGAs are designed for the lowest overall power consumption, highest signal integrity, and highest performance. All of these attributes can lead to lower overall system cost: lower power consumption and high signal integrity can cut design and debugging costs, and high performance can save device costs by allowing the design to be done in a lower, less-expensive speed grade. ●●