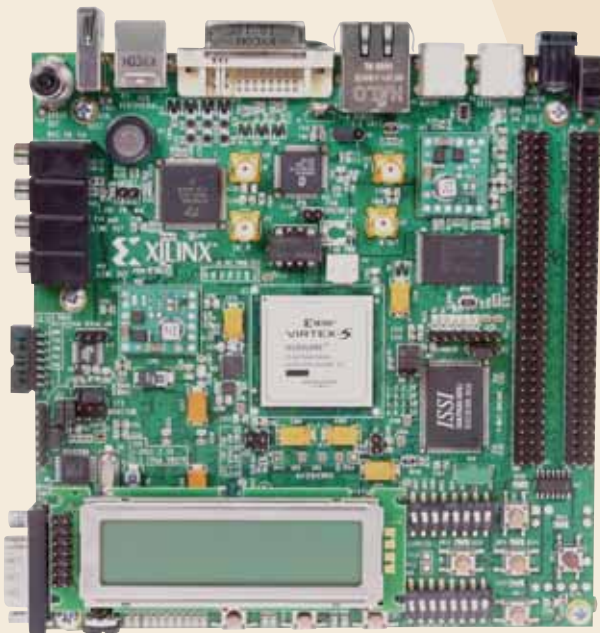


# Virtex-5 ML501 Evaluation and Development Platform



## Features

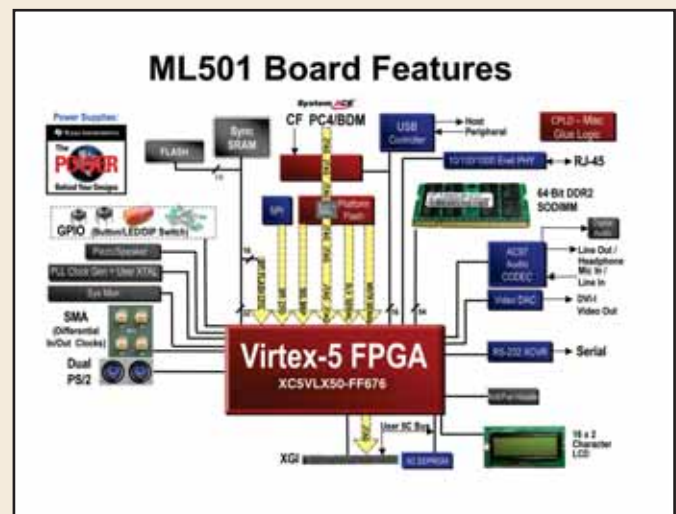
- XC5VLX50-FF676
- DDR2 SODIMM (256 MB)
- ZBT SRAM (1 MB)
- Linear flash (32 MB)
- System ACE™ CompactFlash (CF) technology
- Platform flash
- SPI flash
- JTAG programming interface
- External clocking (two differential pairs)
- USB (two) – host and peripheral
- PS/2 (two) – keyboard, mouse
- RJ-45 – 10/100 networking
- RS-232 (male) – serial port
- Audio in (two) – line, microphone
- Audio out (two) – line, amp, SPDIF, Piezo speaker
- Video (DVI/VGA) output
- Single-ended and differential I/O expansion
- GPIO DIP switch (eight)
- GPIO LEDs (eight)
- GPIO push buttons (five)

## An ideal general-purpose, low-cost development platform.

The Xilinx® Virtex™-5 ML501 evaluation platform is a feature-rich, low-cost evaluation/development platform that provides easy and practical access to the resources available in the onboard Virtex-5 LX FPGA. Supported by industry-standard interfaces and connectors, the ML501 board is a versatile development platform for multiple applications. Video, audio, and communication ports as well as generous memory resources extend the functionality and flexibility of the ML501 board beyond a typical FPGA development platform.

**Reference Designs:** Xilinx Platform Studio project with verified hardware design and stand-alone software applications

**Demonstrations:** Quick-start applications on a CF card



For additional product and ordering information, visit [www.xilinx.com/ML501](http://www.xilinx.com/ML501).

# Virtex-5 ML505 Evaluation and Development Platform



## Features

- XC5VLX50T-FF1136
- DDR2 SODIMM (256 MB)
- ZBT SRAM (1 MB)
- Linear flash (32 MB)
- System ACE™ CompactFlash (CF) technology
- Platform flash
- SPI flash
- JTAG programming interface
- External clocking (two differential pairs)
- USB (two) – host and peripheral
- PS/2 (two) – keyboard, mouse
- RJ-45 – 10/100/1000 networking
- RS-232 (male) – serial port
- Audio in (two) – line, microphone
- Audio out (two) – line, amp, SPDIF, Piezo speaker
- Rotary encoder
- Video input
- Video (DVI/VGA) output
- Single-ended and differential I/O expansion
- GPIO DIP switch (eight), LEDs (eight), and push buttons (five)
- GMII and SGMII support for Ethernet PHY
- PCI Express plug-in card form factor (x1 endpoint)
- GTP transceiver: SFP (1000-Base-X)
- GTP transceiver: Four SMA's connected to one GTP serial transceiver
- GTP transceiver: SATA (two)
- GTP transceiver clock synthesis chips
- Header for second serial port
- Second Platform Flash PROM (32 Mb) for large device
- Mictor trace port
- BDM debugging port
- Soft-touch port

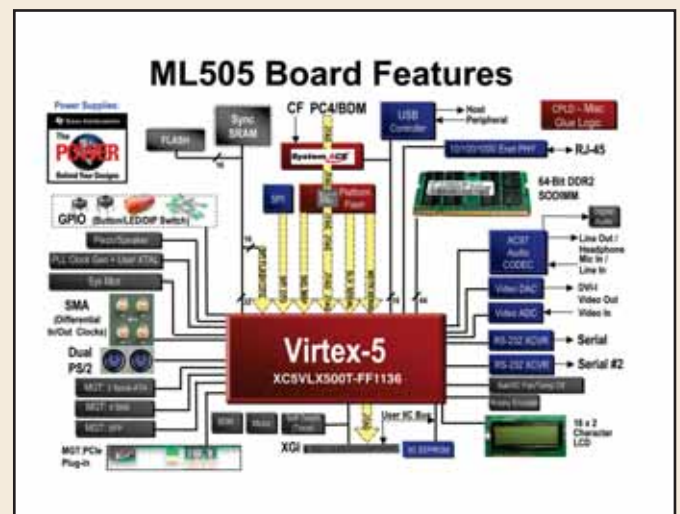
A low-cost embedded system and RocketIO GTP transceiver development platform.

The Xilinx® Virtex™-5 ML505 evaluation platform, based on RocketIO™ technology, is a feature-rich, low-cost evaluation/development platform that provides easy and practical access to the resources available in the on-board Virtex-5 LXT FPGA.

Supported by industry-standard interfaces/connectors, generous memory resources, and companion chipsets, the ML505 board is a versatile development platform for multiple applications including embedded systems.

**Reference Designs:** Xilinx Platform Studio project with verified hardware design and stand-alone software applications

**Demonstrations:** Quick-start applications on a CF card



For additional product and ordering information, visit [www.xilinx.com/ML505](http://www.xilinx.com/ML505).

# The Virtex-5 ML550 Networking Interfaces Tool Kit



## Designing networking, telecom, servers, and computing systems with Virtex-5 FPGAs.

Many of today's telecom and networking systems use high-bandwidth interfaces based on LVDS or other differential I/O standards. Differential I/O standards simplify system design by improving system performance and signal integrity.

Protocols based on source-synchronous I/Os such as SPI-4.2 and SFI-4 are central to leading-edge system design. To take advantage of these technologies, you have to work through multiple challenges to ensure device interoperability and standards compliance. Xilinx provides the Virtex™-5 network interface board, as well as standards-compliant IP cores and free reference designs, to help you tackle these high-speed, source-synchronous interface challenges. This allows you to focus on user application design and not worry about interoperability and standards compliance.

The ML550 evaluation platform supports a wide range of communications standards, including SPI-4.2 and SFI-4. Figure 1 shows the user interface of an LVDS BERT demo running on an ML550 board. The user interface includes a bit error rate tester (BERT) that measures the integrity of the data received from 16 LVDS transmitters. You can select from several pseudorandom bit sequences to simulate data; error counters on the user interface maintain a running count of all bit errors that occur during transmission. The BERT also keeps track of which channels are receiving errors to provide further troubleshooting visibility in a multichannel design.

### Features

The ML550 RoHS-compliant development board includes:

- One Virtex-5 XC5VLX50T-FFG1136 device
- Seven Clock Sources:
  - Epson EG2121CA 2.5V, 200-MHz and 250-MHz LVPECL oscillators
  - Epson EG2121CA 2.5V, 133-MHz LVDS oscillator
  - Two sets of SMA differential clock inputs
  - Two ICS8442-based programmable clock circuits (LVDS) (31.25 MHz to 700 MHz)
- Display Support:
  - 2 x 9 connector I/F for standard 3.3V LCD character displays
  - Also supports 64 x 128 LCD panel (Display Technologies Q64128E-FC-BC-3LP)
- Connectors and Interfaces:
  - One USB "B" port
  - Six LVDS Samtec connectors (a total of 53 input channels and 53 output channels)
- Memory:
  - 64 MB of 8-bit-wide DDR SDRAM memory (Micron Semiconductor MT46V64M8BN-75)
- Device Configuration:
  - A System ACE™ Compact Flash configuration controller that allows storing and downloading of as many as eight FPGA configuration image files
- Miscellaneous:
  - On-board power regulators with  $\pm 2.5\%$  and  $\pm 5\%$  margin test capabilities
  - Kit includes an LVDS loopback daughterboard and a reference/demo design CD



Figure 1 – BERT user interface

For more information on this development board and the kit, visit [www.xilinx.com/XOB](http://www.xilinx.com/XOB). To purchase the ML550, contact your local sales representative, or email [designkits@xilinx.com](mailto:designkits@xilinx.com).

# ML555 – PCI Express Development Tool Kit



## A highly configurable pre-verified development solution.

The Xilinx® ML555 RoHS-compliant PCIe/PCI-X/PCI development board provides a pre-verified solution to parallel and serial PCI interface design challenges. Using an established development environment can dramatically shorten the design cycle. By using proven Xilinx dedicated blocks, you can focus your efforts on specific application development and avoid time-consuming PCIe or PCI development.

The ML555 development board is a RoHS-compliant PCIe add-in card with both eight-lane PCIe and 64-bit PCI-X edge connectors, allowing for development of PCIe and PCI-X/PCI applications.

The Virtex™-5 ML555 PCIe tool kit includes:

- A Virtex-5 ML555 RoHS-compliant PCIe development board (XC5VLX50T-FFG1136 FPGA)
- 256 MB (32M x 64-bit) Micron single-rank DDR2 SODIMM (MT4HTF3264HY-667)
- Documentation and reference design CD-ROM

The ML555 development board (Figure 1) was designed to demonstrate the high-speed serial capability of the 12 RocketIO™ GTP serial transceivers embedded in the Virtex-5 FPGA.

### Features

#### Xilinx Devices:

- XC5VLX50T-FFG1136 FPGA, XCF32P-FSG48C (Platform Flash), and XC2C32 CoolRunner™-II CPLD

#### Clock Sources:

- Three on-board clock sources (33 MHz, 125 MHz, and 200 MHz); two differential SMA clock inputs; and two programmable ICS8442 clock synthesizers (31.25 MHz to 700 MHz) to support DDR2 memory interfaces, 10/100/1000 Mb Ethernet protocols, SATA, Fibre Channel, Aurora, and other serial GTP baud rates

#### Memory:

- 256 MB (32M x 64-bit) Micron single-rank DDR2 SODIMM
- XCF32P-FSG48C Platform Flash

#### Connectors and Interfaces:

- One set of SMA ports for off-board GTP transceiver connectivity including:
  - HW-AFX-SMA-SFP – converts SMA to SFP form factor
  - HW-AFX-SMA-SATA – converts SMA to SATA interface
  - HW-AFX-SMA-RJ45 – converts SMA to RJ45 interface
  - HW-AFX-SMA-HSSDC2 – converts SMA to HSSDC2 interface
- PCI-X/PCI 3.3V system board keyed to 64-bit PCI or PCI-X connector
- Ethernet support through an embedded Ethernet MAC (or soft IP core) and Xilinx Generic Interface (XGI) header, which supports the Xilinx HW-BERG-EPHY daughter board (sold separately), providing 10/100/1000 Mb Ethernet and MII, GMII, and RGMII connectivity
- Two Samtec connectors, each providing 24 LVDS signal pairs:
  - Support for future third-party A/D and D/A mezzanine boards
  - Pinout-compatible with Xilinx ML550 source-synchronous development board Samtec connectors
- One USB 2.0 port

#### Device Configuration:

- Support for as many as four FPGA design images in two Xilinx XCF32P-FSG48C Platform Flash configuration PROM devices
- Static or dynamic device reconfiguration support with the XC2C32 CoolRunner-II CPLD
- Device configuration through onboard Platform Flash, Xilinx PC-IV JTAG cable, or Xilinx Platform Cable USB

#### Soft Cores Evaluation Copies Included:

- Our current available release for Virtex-5 devices:
  - PCI-X/PCI V6.1
  - PCI V4.1
  - PCIe Wrapper support – x1, x2, x4, and x8 endpoint connectivity

#### Miscellaneous:

- Three user push-button switches and LEDs

Visit the Xilinx IP Center at [www.xilinx.com/ipcenter/](http://www.xilinx.com/ipcenter/) to review the status of PCIe Wrapper and PCI and PCI-X cores.

# ML561 – Advanced Memory Development System



## Features

- Memory interfaces: DDR2 SDRAM, DDR SDRAM, QDR II SRAM, RDRAM II (Table 1)
- Three Xilinx Virtex-5 XC5VLX50T-FF1136 devices
- Multiple FPGA configuration interfaces
- Debugging ports: RS-232, USB, LEDs, and DIPs
- CD-ROM with complete documentation
- Hardware-verified reference designs using the MIG tool

Parameter	DDR2 SDRAM	DDR SDRAM	QDR II SRAM	RDRAM II
Data Rate	667 Mbps	400 Mbps	1.2 Gbps	600 Mbps
Clock Rate	333 MHz	200 MHz	300 MHz	300 MHz
Data Width	32-bit Comp, 144-bit (DIMM)	32-bit	(72 + 72)-bit	36-bit
I/O Standard	SSTL18	SSTL2	HSTL	HSTL

Table 1 – Memory architectures supported by the ML561 development system

## Achieve your performance targets in the shortest development time.

Building interfaces to high-performance memory devices presents challenges such as high-speed synchronous data capture, along with implementing complex physical-layer interfaces and control logic.

Xilinx® Virtex™-5 FPGAs solve these challenges with advanced silicon capabilities, including:

- ChipSync™ source-synchronous technology, which provides 75-ps resolution for clock-to-data alignment, ensuring reliable data capture.
- XCITE digitally controlled impedance (DCI) simplifies PCB design and improves signal integrity by terminating a signal right on the die, minimizing stub reflections and dynamically adjusting on-chip impedance.
- Second-generation sparse chevron packaging reduces board layer count and simplifies board design by minimizing the number of external decoupling capacitors needed on the board.

To shorten design time, Xilinx provides expert guidance: free hardware-verified reference designs, application notes, user-friendly tools, and advanced development systems. This combination of unique silicon capabilities and comprehensive support enables you to build and verify robust memory interfaces quickly and easily.

The ML561 advanced memory development system offers an excellent platform to develop and verify high-performance memory interfaces using Virtex-5 FPGAs.

Xilinx also offers a free menu-based tool, the Memory Interface Generator (MIG), to further customize reference designs (Figure 1). MIG generates the pin placement file and a complete modular set of HDL files.



Figure 1 – Memory Interface Generator

You can download the reference design, application notes, Memory Interface Generator, and other resources for memory interface designs at [www.xilinx.com/virtex5/](http://www.xilinx.com/virtex5/). If you are interested in purchasing the ML561, contact your local sales representative, or e-mail [designkits@xilinx.com](mailto:designkits@xilinx.com).

# The Xilinx Virtex-5 LX Development Kit



## Features

- Xilinx XC5VLX50-1FF676 FPGA
- 16M x 32 DDR2 SDRAM
- 4M x 16 of flash
- 10/100/1000 PHY
- 10-bit LVDS receive and transmit interfaces
- Cypress USB 2.0 device
- RS232 serial port
- EXP expansion slot
- Programmable LVDS clock generator
- On-board 100 MHz LVTTTL oscillator
- On-board LVTTTL oscillator socket
- XCF32P Platform Flash
- JTAG programming/configuration port

- BPI configuration support
- SystemACE™ module connector
- Four user LEDs
- Four-position user DIP switch
- Four user push button switches
- LCD panel

## Applications

- General-purpose prototyping
- IP and software development
- Networking and communications
- Storage and servers
- DSP and video processing

A complete development platform for designing and verifying applications based on the Xilinx Virtex-5 LX FPGA family.

Available with the Xilinx® Virtex™-5 LX50 device (XC5VLX50-1FF676), the Virtex-5 Development Kit enables you to prototype high-performance designs with ease, while providing expandability and customization through the EXP expansion slot.

The system board includes DDR2 SDRAM, flash memory, a 10/100/1000 Ethernet PHY, and a serial port, making it an ideal platform for MicroBlaze™ development. Other board features include a USB port, programmable LVDS clock, 10-bit Tx/Rx high-speed LVDS interface, user switches and LEDs, and a 2 x 16-character LCD panel.

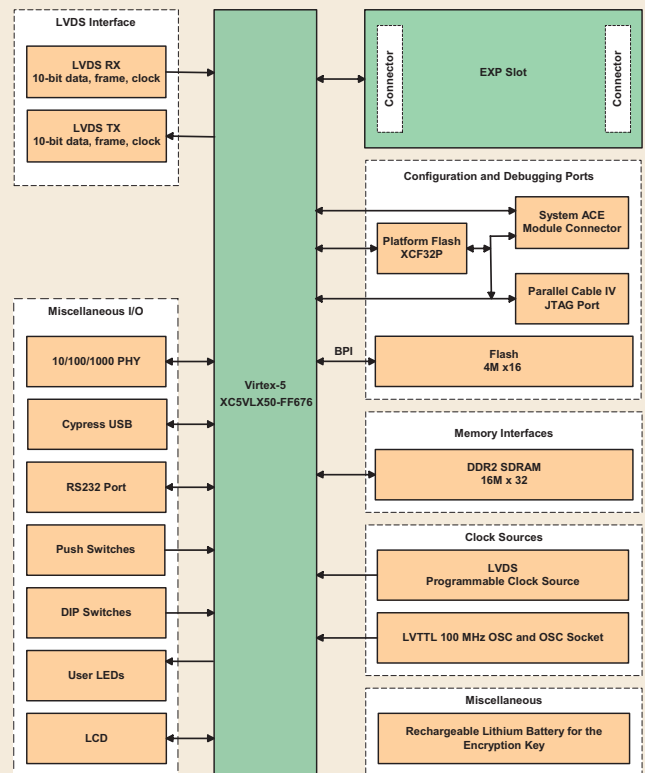
The board also provides a full EXP expansion slot, providing a total of 168 high-speed, single-ended, and differential user I/O. You can easily add EXP modules to the board for additional application-specific functions.

The Virtex-5 development kit includes:

- Development board
- Downloadable documentation and reference designs
- Wall-mount power supply

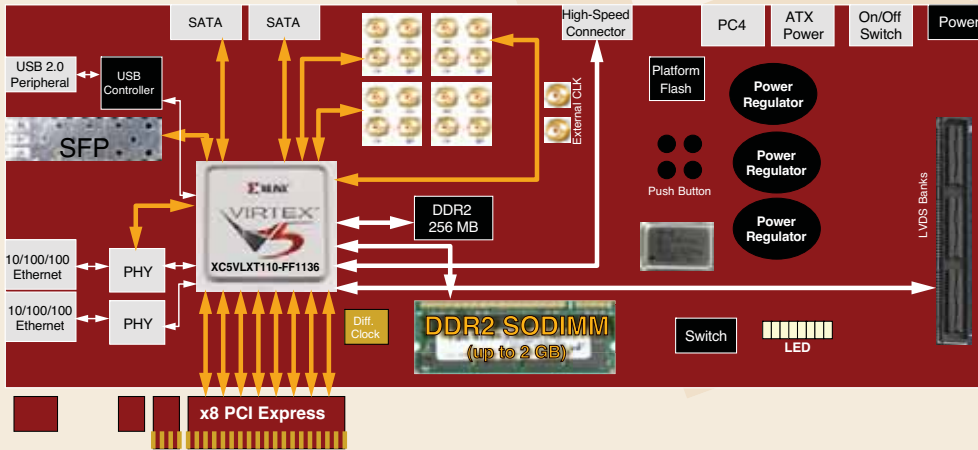
Optional EDK and ISE™ software is also available.

Part Number: AES-XLX-V5LX-EVL50-G



For more information on the Virtex-5 LX Development Kit or to purchase the kit, visit [www.em.avnet.com/virtex5lx](http://www.em.avnet.com/virtex5lx). To purchase by phone, call (800) 408-8353.

# HiTech Global Virtex-5 PCI Express Development Platform



## Features

- Xilinx XC5VLXT110-FF1136
- x8 PCI Express upstream interface
- As much as 2 GB of DDR2 SODIMM
- 256-MB discrete DDR2 SRAM
- Platform Flash for FPGA configuration
- x2 10/100/1000 Ethernet (with SGMII)
- x2 Serial ATA (SATA)
- x1 SFP
- x1 6 SMA connectors (four Virtex-5 RocketIO GTP serial transceiver channels)
- x1 high-speed connector for custom modules (DVI, USB, Camera Link)
- x1 USB 2.0 peripheral
- Multiple banks of LVDS Samtec connectors
- SMA for external clock

## Seamless serial interface connectivity enabled by the Virtex-5 LXT FPGA.

Powered by a Xilinx® Virtex™-5 LXT FPGA, supported by mainstream peripherals, and designed with excellent signal integrity performance, the HiTech Global HTG-V5PCIE is the ideal platform for serial interface/connectivity developments, including PCI Express subsystems, Serial ATA (SATA), Fibre Channel, RapidIO, and XAUI.

The hard-coded PCI Express Endpoint block of the Virtex-5 XC5VLXT110FF1136 device simplifies integration and reduces the overall design cycles. Connecting the PCIe subsystem to eight RocketIO™ GTP serial transceivers, the HTG-V5PCIE platform provides as many as eight lanes of PCI Express upstream interface.

Direct access to eight other RocketIO GTP transceivers is provided through several connectors: 16 SMA (4 per channel), 1 SFP, 2 SATA, and 1 Ethernet (SGMII). This extends the flexibility of the HTG-V5PCIE platform and enables you to use the same platform for multiple applications.

The availability of high-speed connectors with LVDS and single-ended I/Os provide direct access to the HTG-V5PCIE platform's resources for custom modules and daughtercards such as DVI and Camera Link.

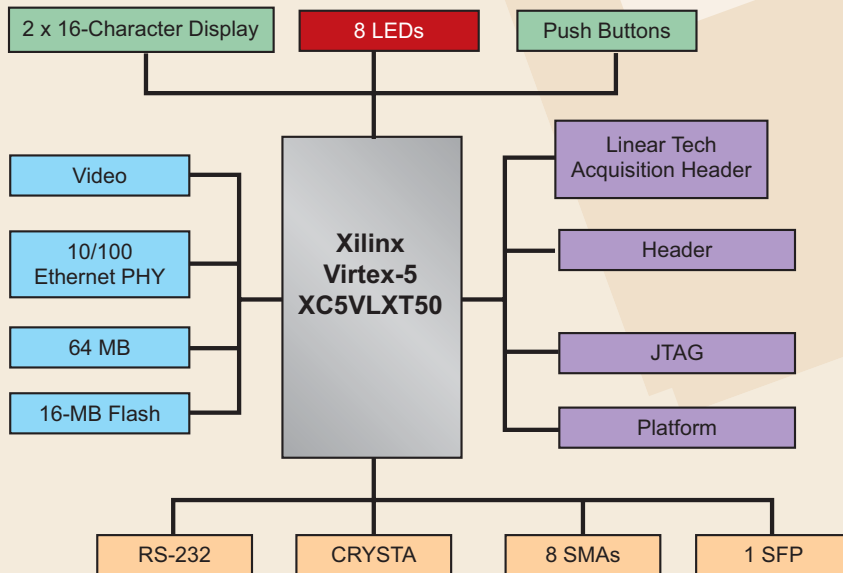
The DDR2 SODIMM, along with 256 MB of discrete memory components, provides a generous amount of memory. You can also use a Xilinx Platform Flash memory for quick configuration of the on-board Virtex-5 LXT FPGA.

The HTG-V5PCIE can be used either as an eight-lane PCI Express Endpoint block or as a stand-alone development platform.

For product and ordering information, visit [www.hitechglobal.com/V5PCIEExpress.htm](http://www.hitechglobal.com/V5PCIEExpress.htm).

# Nu Horizons Virtex-5 LXT Evaluation Kit

**NU HORIZONS**  
ELECTRONICS CORP



## Features

- Xilinx XC5VLX50T FPGA
- Linear Technology FastDAACs connector
- Linear Technology LTM4601 DC/DC uModule
- 10/100/1G Marvell Ethernet PHY
- 64 MB ISSI DRAM
- 64 MB ST Flash
- Eight SMA's for RocketIO transceivers
- One receptacle for SFP module
- 2 x 16-character display
- Part number: NH-5VLX50T-EVL

## Nu Horizons creates a low-cost evaluation kit for Virtex-5 LXT platform FPGAs.

Nu Horizons's newest evaluation kit is designed for customers interested in evaluating Xilinx® Virtex™-5 LXT FPGAs. This kit differs from other kits from Nu Horizons in that it has the added ability for high-speed serial communication.

By connecting eight SMA's to two RocketIO™ transceivers, you can transmit and receive on a signal board. For off-board communication, an SFP cage is also provided.

The additional peripherals, including memory and Ethernet, allow customers to create complete systems and implement them on the kit.

The Linear Technology FastDAACs connector can expand the capabilities of the system by connecting one of more than 50 high-speed A/D and D/A daughtercards available from Nu Horizons and Linear Technology.

The Virtex-5 LXT Evaluation Kit is the perfect way to begin designing with the latest platform FPGAs from Xilinx.

To view the user's manual, download the schematic, or order online, visit [www.nuhorizons.com/5vlxtevl](http://www.nuhorizons.com/5vlxtevl).

## Xpress Track Training Classes

In addition to providing customers with low-cost evaluation kits, Nu Horizons also offers a range of hands-on workshops designed to help you through the learning curve associated with using new products.

Xpress Track seminars and workshops are conducted in Nu Horizons training centers throughout the world. Through the use of computers and evaluation and demonstration boards, each training center replicates an ideal design environment for engineers interested in leveraging Xilinx development tools, architectures, and products. Topics covered in Xpress Track include fundamentals of FPGAs, the MicroBlaze™ processor, PowerPC™ processor design, VHDL, and signal processing. To see what topics will be covered in your area, visit [www.nuhorizons.com/seminars](http://www.nuhorizons.com/seminars).

For more information on the Nu Horizons Virtex-5 LXT Evaluation Kit, visit [www.nuhorizons.com/linecard/xilinx.asp](http://www.nuhorizons.com/linecard/xilinx.asp).