



Push the Performance of Your Complex Designs with Virtex-5 and Synplify Pro

Synplicity and Xilinx Team Up and Deliver

In May 2006, Xilinx announced Virtex-5 - the industry's first 65nm FPGA. Long before this announcement was made, however, Xilinx knew that an innovative kind of Synthesis tool would be required to enable users to take advantage of the performance and logic density of these revolutionary devices. That's why, once again, Xilinx teamed up with Synplicity.

Engineers at Xilinx and Synplicity have worked closely over the past year to ensure that Synplicity's market-leading synthesis software would provide optimal support for the new Virtex-5 devices. The resulting changes made to the synthesis algorithms allow users to take maximum advantage of these high-capacity Virtex-5 devices.

The enhanced optimizations built into the Synplify Pro software, along with its timing-driven approach to synthesis, allow designers to push the performance of their complex designs while remaining comfortably within their time-to-market goals.

Looking Beyond Today

Future generations of devices will contain even greater density points and capabilities than the current devices, further expanding the reach of advanced FPGA architectures across a wide range of application domains. That's why Synplicity and Xilinx have formed an Ultra-high Capacity Timing Closure Task Force. The purpose of this task force is to enable engineers from both companies to collaborate to define and implement new design flows that maximize the quality of results of design productivity of ultra-high density designs with next-generation 65-nanometer FPGAs.

To learn more about how Synplicity's tools can help you gain maximum performance from your complex designs, contact Synplicity at info@synplicity.com or visit our website at www.synplicity.com.



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