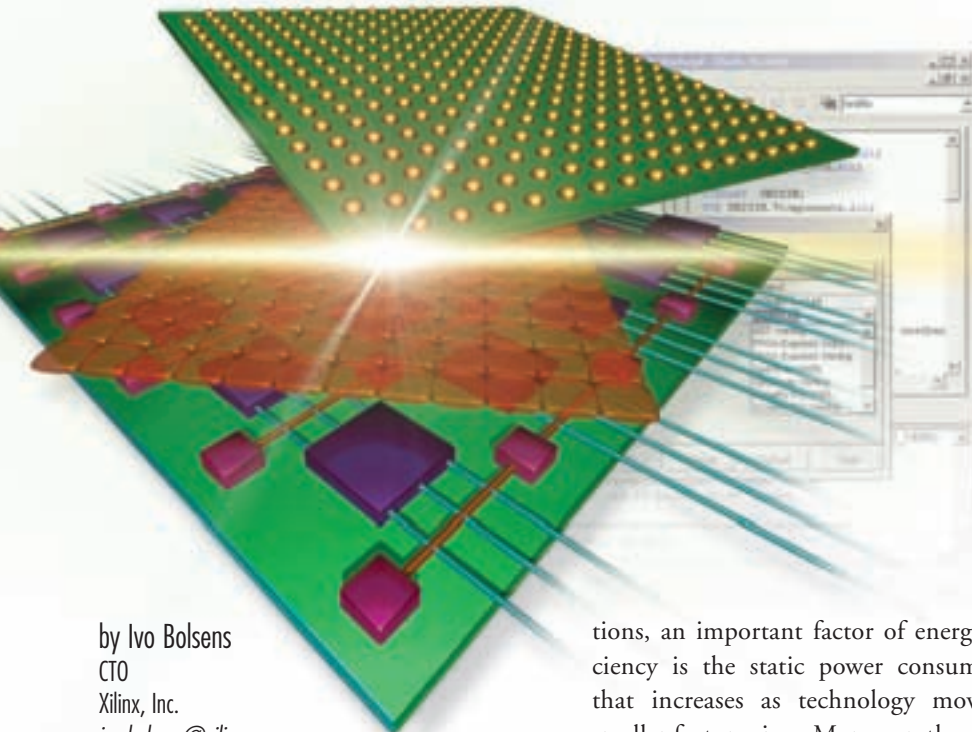


Energy-Efficient System Design

Power optimization techniques in silicon and software have become mainstream considerations in FPGA system design.



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In recent years, power consumption as a figure of merit for FPGAs has grown in importance. Because of the increasing use of FPGAs in high-volume and embedded applications, power dissipation and energy efficiency are at the forefront of the system designer's concerns. Lower power consumption simplifies thermal management and results in smaller (or no) heat sinks, cheaper packages, and lower airflow requirements, which in turn lead to lower cost and more compact system solutions. Lower current requirements simplify power supply design, resulting in fewer system components and less PCB area.

As high-volume applications are becoming more battery operated, the importance of energy efficiency (power consumed over time) is growing to allow for longer battery life. In many applica-

tions, an important factor of energy efficiency is the static power consumption that increases as technology moves to smaller feature sizes. Moreover, the cost of energy consumption plays a growing role in the total cost and OPEX (operating expenditure) of end-customer solutions.

It is well known that, in terms of giga floating-point operations per second (GFLOPS)/Watt, the FPGA programmable architecture is more power-efficient than a processor architecture. A high-end Xilinx® Virtex™-5 component (such as an XC5VLX330) can deliver 3 to 12 times more GFLOPS (GFLOPS being 64-bit multiply, multiply/add, or add) and consumes 2 to 3 times less power than a leading-edge processor architecture (such as today's dual-core x86 architectures). Therefore, depending on the application, the high-end Virtex-5 family will deliver 3 to 30 times better GFLOPS/Watt than leading-edge processors. Comparing 32-bit floating-point, fixed-point, or integer computations per Watt would even further benefit the FPGA.

For a given system application, the relentless focus on power optimization has resulted in Virtex-5 devices consuming between 30% to 80% less power than Virtex-4 devices (depending on which resources are being used). In the low-cost Spartan-3 family, the focus has been further on ease of use of the power management and on improving energy efficiency by providing different power-saving modes during periods of inactivity.

In contrast to other figures of merit, such as cost and performance, the efficiency of power consumption cannot be captured by one single comparative number. Different application characteristics and use models can result in different benefits from all of the possible power optimizations. "The Power of FPGA Architectures" in this issue of the *Xcell Journal* demonstrates the effectiveness of design techniques such as sleep modes, power and clock gating, voltage scaling, and how specialized hardware depends heavily on the system application at hand. "Optimizing FPGA Power with ISE Design Tools," also in this issue, highlights the importance of intelligent design tools and sophisticated place and route algorithms that can exploit the characteristics of an application to optimize power consumption of the final implementation on an FPGA.

Designing power-efficient systems into an FPGA encompasses a holistic optimization process that includes an understanding of all system constraints, the selection of the optimal FPGA architecture, and the optimization of the design during all steps in the design flow, from architecture to final place and route. Aggressive scaling and cost reduction will continue to move FPGAs further into higher volume and lower power products. This will result in a constant improvement of FPGA architectures and design tools to meet the requirements of lower power and energy efficiency. 🌈