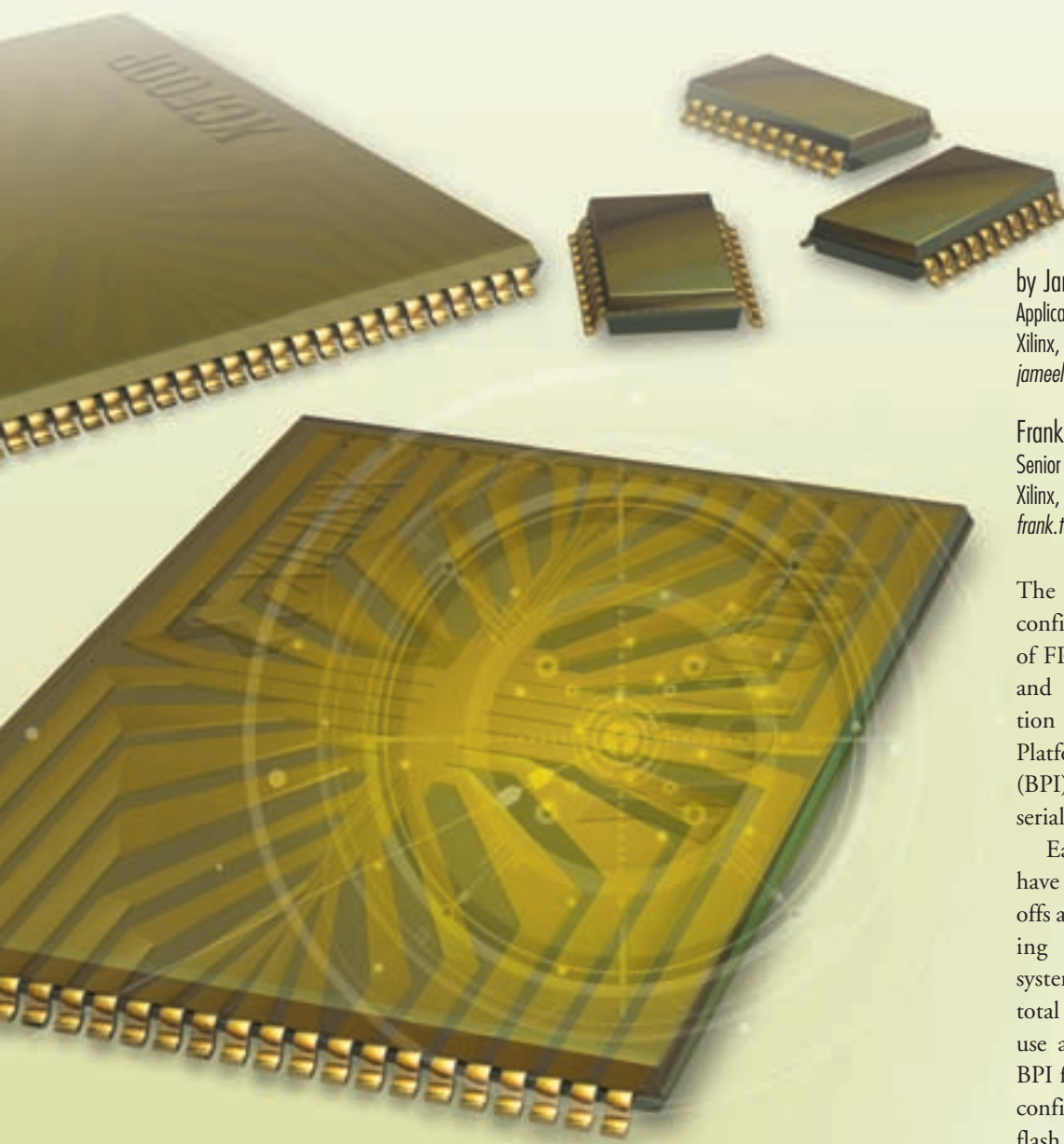


Picking the Right PROM for Your System

Platform Flash PROMs deliver at every stage in the product lifecycle.



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The flexible and fully integrated FPGA configurations from Xilinx take advantage of FPGA capabilities like remote updating and reconfiguration. Available configuration silicon options (see Figure 1) include Platform Flash, byte peripheral interface (BPI) supporting parallel NOR flash, and serial peripheral interface (SPI flash).

Each of these configuration options have different speed and complexity trade-offs and can offer you the flexibility of sharing configuration memory with other system-level tasks, thus greatly reducing total cost. For example, some applications use a microprocessor that interfaces with BPI flash on board. In these cases, you can configure the FPGA from the same BPI flash that the microprocessor uses to save cost and board space.

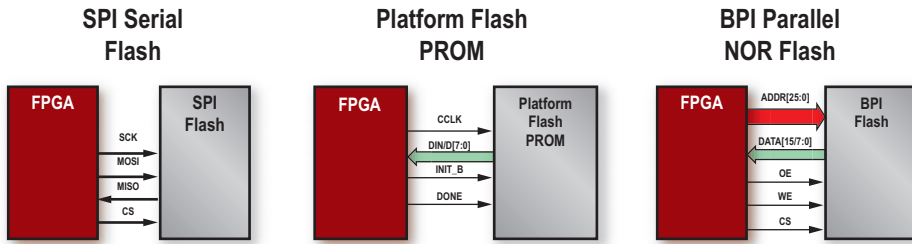


Figure 1 – Available configuration silicon options in Spartan-3E/3A/3AN and Virtex-5 devices

Other applications are more cost-sensitive; you may have to make certain sacrifices to keep the project within your budget. If you can afford a slower configuration time, SPI PROMs can provide the lowest cost solution in many cases.

Because Xilinx gives you the flexibility to use multiple memory sources for FPGA configuration, you will need to consider several factors at the start of the design: the configuration speed required to meet system specifications (for example, PCI Express); ease of use and design (such as a simple power-up configuration); and memory, with value-added features like multiple design revisioning (for product customization) and safe-update capabilities (for flawless remote configuration). Other features such as compression can also save costs.

Before the introduction of the Xilinx® Spartan™-3E, Spartan-3A, and Virtex™-5 families, designers who configured Xilinx FPGAs with commodity flash would use a three-chip configuration solution: a commodity flash PROM, a CPLD, and of course the FPGA. The newer FPGAs eliminate the need for a CPLD (or other controller) by providing a direct interface for leading commodity flash devices, thus reducing the chip count to one memory device.

Safe-Update Solutions with Platform Flash PROMs

In-system safe-update solutions, also referred to as remote-update solutions, are becoming more and more popular; in many cases they are essential to a product's success. There are several variations of a safe-update solution, but the basic idea is to update the FPGA bitstream in-system, which involves updating the image inside the PROM and reconfiguring the FPGA from that updated

image. The “safe” part of a safe-update solution comes from the ability to recover from a failed attempt at updating the FPGA, which is only possible if the FPGA always has a known-good or golden bitstream stored in the PROM, from which it can always configure in case of an error. With competing FPGAs, these solutions required a third device, typically a CPLD, to control the update process and help the FPGA recover in the event of an error.

For example, where there is a need to reconfigure multiple devices (see Figure 2) from a base station, it is important that the update be flawless. If there is any corruption of the new configuration data, there is a fail-safe fallback position.

Whereas competing solutions required a third device, Virtex-5 FPGAs have “fall-

back” logic already built into the device; only the FPGA and PROM are necessary. This fallback logic is among the key parts to a safe-update solution, which comprises:

- A file-generation flow for updated image: iMPACT + XAPP972
- An embedded in-system programmer: XAPP058 or XAPP424
- Non-volatile configuration memory: a Platform Flash XCF00P PROM
- An FPGA with a fail-safe configuration feature: Virtex-5 fallback feature

The first step is creating a file that contains the information to update the PROM with the new bitstream for the FPGA; you can do this with iMPACT software tools. The file created will contain the new bitstream as well as the instructions to interface with the PROM. For more details, see Xilinx application note XAPP972, “Using Serial Vector Format (SVF) Files to Update a Platform Flash PROM Design Revision In-System,” at www.xilinx.com/bvdocs/appnotes/xapp972.pdf.

The next step is to run or play this file (Figure 3); you can do this with an embedded in-system programmer available in Xilinx application note XAPP424,

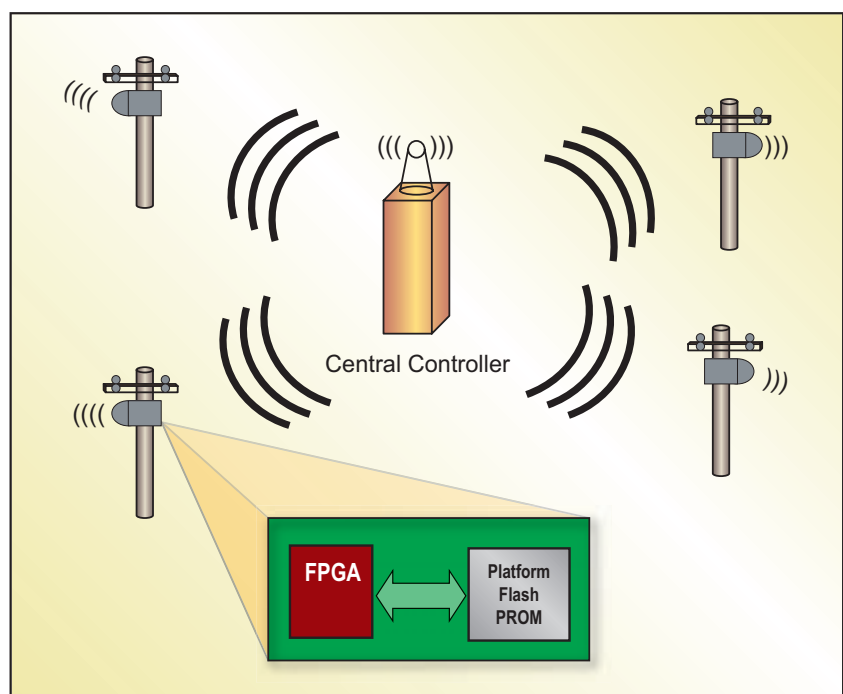


Figure 2 – Reconfiguring multiple systems from a remote base station

“Embedded JTAG ACE Player,” (www.xilinx.com/bvdocs/appnotes/xapp424.pdf) or XAPP058, “Xilinx In-System Programming Using an Embedded Microcontroller,” (www.xilinx.com/bvdocs/appnotes/xapp058.pdf). XAPP424 is the latest in-system programmer available from Xilinx and is capable of significant performance gains over previous solutions in many cases. The programmer uses JTAG to interface with the Platform Flash PROM, which is the next key step in the process.

The Platform Flash XCF00P PROM (Figure 3) is capable of storing as many as four different designs or revisions, but many safe-update solutions only use two: the known-good or golden bitstream and the updated or enhanced bitstream. The key to maintaining safety is to only erase and reprogram the enhanced bitstream and leave the golden bitstream completely unmodified from original programming. XAPP972 describes a method to ensure safety, which is made possible with Platform Flash PROMs.

The last step is the fallback logic inside Virtex-5 FPGAs. Once the Platform Flash PROM has been reprogrammed with the updated bitstream, the FPGA must be reconfigured. The danger is that if there was an error reprogramming the PROM, the FPGA will not be able to configure from the updated bitstream. Fallback logic helps to eliminate this danger. If the FPGA is triggered to reconfigure from the updated bitstream and configuration fails, the FPGA will automatically attempt to reconfigure from the golden bitstream. The golden bitstream is the known-good bitstream that was unmodified during the update process; the FPGA should regain functionality with the golden design. The functionality of the golden bitstream is at your discretion.

This safe-update solution is a two-chip solution made possible with Platform Flash PROMs and Virtex-5 FPGAs. The resources to build such a solution are available on www.xilinx.com and can significantly reduce time to market, as well as add value and flexibility to the project.

Configuration Speed

Another advantage of using Platform Flash PROMs is the configuration speed. For

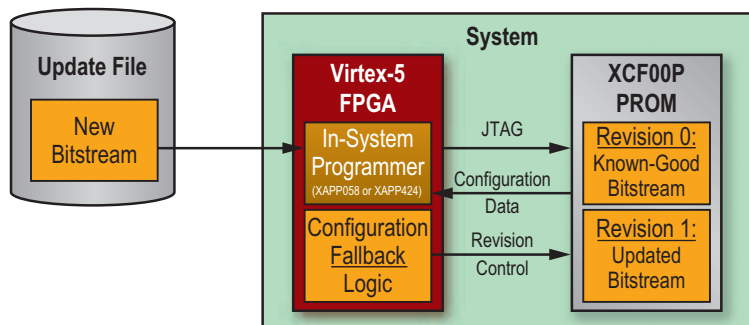


Figure 3 – Safe-update system overview with Virtex-5 FPGAs and Platform Flash XCF00P PROM

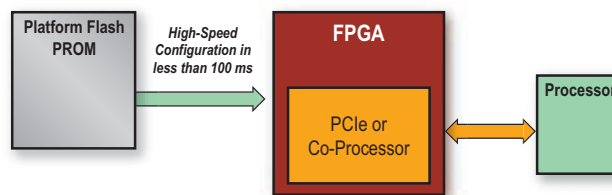


Figure 4 – High-speed configuration with Platform Flash PROMs in less than 100 ms for all Spartan-3E/3A/3AN and Virtex-5 devices up to LX85 and LX85T

most applications, configuration speed is not an issue; however, for several projects, the configuration speed is the difference between success and failure.

For example, applications using PCI Express require the FPGA to configure in less than 100 ms (Figure 4). For some SPI and BPI NOR flash devices, it can be difficult to configure larger FPGAs in that amount of time. The FPGA provides the configuration clock (CCLK) when configuring from a third-party flash device. The CCLK is generated by internal circuitry and on some FPGAs can have 50% variation, which means that if the CCLK is set to 60 MHz, the output clock could range from 30 to 90 MHz. You must set the CCLK to ensure that the maximum clock rate on the PROM is not exceeded.

Finding the correct CCLK speed is easy with a few simple formulas. The FPGA CCLK + 50% should be less than the maximum clock rating on the PROM. The same FPGA CCLK – 50% is the worst-case FPGA CCLK. The worst-case FPGA CCLK is critical when determining the maximum configuration time, which is roughly calculated by dividing the number of configuration bits for a device by the number of bits per second being delivered to the FPGA.

Platform Flash has the ability to run from an external stable clock source. When the FPGA is in slave mode, it too can run from a high-speed stable clock source to deliver the fastest and most consistent configuration times. In most cases configuration times are less than 100 ms, even for mid-sized Virtex-5 devices. (Numbers are approximate; actual numbers may vary across different devices. Refer to the appropriate data sheets for more information at www.xilinx.com/xlnx/xweb/xil_publications_index.jsp.)

Conclusion

Designers must make trade-offs in speed, complexity, functionality, and cost during configuration. Existing on-board BPI and SPI devices can be put to dual-mode use for both configuration and system-level memory. Platform Flash PROMs provide unique money-saving features, including the ability to store and select multiple bitstreams. Virtex-5 and Spartan-3E/3A devices provide you with integral support for SPI and BPI flash, in addition to Platform Flash.

For more information, please visit www.xilinx.com/products/silicon_solutions/proms/pfp/index.htm. 