

# Ultra-High-Speed Spectral Analysis in Xilinx FPGAs

A 32k-point FFT with 2-GSPS data throughput in a single FPGA establishes a new level of performance.

by Bruno Stuber

Professor

University of Applied Sciences Northwestern Switzerland,  
School of Engineering, Institute of Automation

*bruno.stuber@fhnw.ch*

Dino Zardet

Development Engineer

University of Applied Sciences Northwestern Switzerland,  
School of Engineering, Institute of Microelectronics

*dino.zardet@fhnw.ch*

A fast Fourier transform (FFT) is the ultimate way to accomplish spectral analysis in digital signal processing. Many real-time applications require seamless operation with continuous data throughput, a high-speed data rate, excellent spectral resolution, and a large dynamic range. Today, many standard solutions are offered to perform real-time FFTs, either with DSPs or FPGAs. However, to go beyond established limits, a thorough analysis of the system architecture is necessary, as is a design approach that focuses on timing.

FPGAs offer the potential for a huge amount of parallelism. For an FFT application, the number of multipliers and RAM blocks determines the overall performance, expressed in terms of data throughput and the number of spectral lines or bins.

In this article, we will discuss the implementation of a 32k-point FFT (32,768 points) with power spectrum accumulation. The 8-bit input data flows continuously at a rate of 2 gigasamples per second (GSPS), therefore providing an analog bandwidth of 1 GHz. The spectrometer is implemented in a single Xilinx® Virtex™-II Pro XC2VP70 FPGA operating at an overall clock speed of 125 MHz.

We developed the unit for spectroscopy applications in millimeter and terahertz radio astronomy. However, many other applications are possible, including low-frequency radio astronomy, atmospheric physics, physical chemistry, radio surveillance, and spectral measurements.

### High-Speed FFT Architecture in an FPGA

To achieve the enormous throughput of 2 GSPS, a strictly synchronous and pipelined architecture is necessary along the signal processing path. A “pipeline FFT” is best suited for a high-speed parallel implementation.

In typical FFT signal flow graphs, a number of  $r$  input data, where  $r$  is a power of two, are processed within the first butterfly stage. The butterfly outputs  $r$  intermediate results;  $r$  is the radix of the FFT implementation. The butterfly involves some additions and  $(r-1)$  complex multiplications with twiddle factors. This process is visualized in Figure 1.

$M$  stages are needed for an  $N$ -point FFT,  $M = \log_r(N)$ . All stages (with the exception of the last one) perform twiddle multiplication and data shuffling, which are necessary to implement the well-known “butterfly” signal flow graph of the FFT algorithm.

Therefore, a radix- $r$  FFT pipeline forwards  $r$  data streams with the pipeline’s clock frequency,  $f_c$ . The data throughput is thus  $r \times f_c$ .

The hardware resources involved in the FFT processing are adders, multipliers, memory for the twiddle factors and data shuffling, and a number of multiplexers. We recommend using dedicated multipliers, preferably in conjunction with the assigned internal registers. Twiddles are stored in Xilinx block RAM instantiated as ROM. You can also use block RAM for

most of the data shuffling stages, employing the dual-port capability, whereas some smaller memory blocks are more efficiently realized with distributed RAM.

A closer analysis of the pipeline FFT shows that there are  $(N-r)$  complex twid-

and weeks. To extract the chosen signal, the accumulation process is carried out “on source,” with the antenna directed to the object, and “off source,” with the antenna deflected. The resulting spectra are then subtracted.

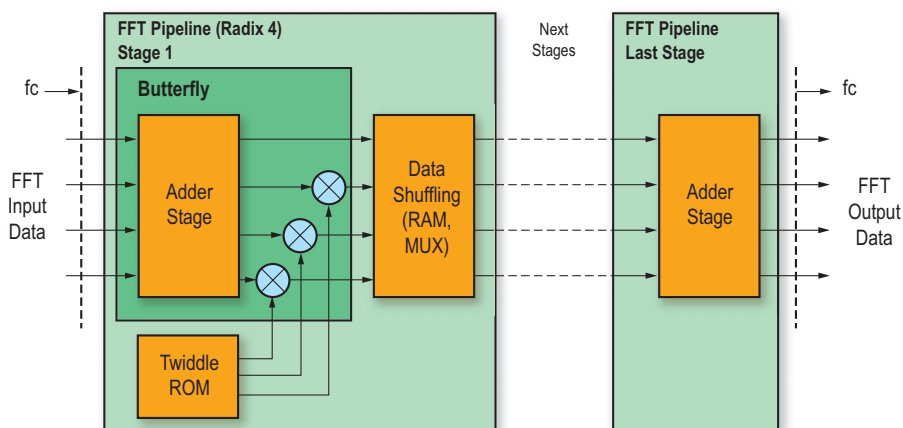


Figure 1 – Pipeline FFT structure

dle factors needed and a total number of  $N$  complex data memory for the data shuffling. The number of multipliers is  $4 \times (M-1) \times (r-1)$  for a radix-2 or radix-4 FFT pipeline.

A crucial factor with respect to the throughput is  $f_c$ . The dedicated signal processing elements, multipliers, and RAM blocks in Virtex-II FPGAs have a propagation delay of as much as 5 ns. Together with the signal path delays – assuming that such a complex circuit is spread over a large area – an overall delay of approximately 8 ns is feasible, resulting in an overall system clock of 125 MHz.

Several pipelines may operate in parallel with the aid of an extended input, buffering and scheduling to further enhance overall data throughput.

### Applying the FFT in Radio Astronomy

Spectrometers in millimeter astronomy are used to identify and explore atomic and molecular lines of cosmic sources. Because the signals are very weak, the signal-to-noise ratio may be less than  $-60$  dB; the power spectra will be accumulated over a period of milliseconds up to hours

The frequency range observed is spread from tens of kilohertz to approximately 2 terahertz. The bandwidths of the spectrometers should therefore be as large as possible while the frequency resolution is reasonably in the range of 100 kHz. Currently, broadband spectrometers are mainly based on acousto-optical devices with bandwidths as high as 3 GHz. They have, however, a resolution of about 1 MHz and pose some problems in dynamic range, stability, and cost.

New generations of FPGAs and high-speed digital-to-analog converters enable FFT-based solutions that are competitive with or even superior to acousto-optical devices, with the advantages of an all-digital, reconfigurable, and programmable system.

Radio spectroscopy based on FFT typically comprises three processes:

- Digitizing the receiver’s intermediate signal
- FFT computation
- Accumulation (averaging) of the power spectra; that is, the squared magnitude of complex FFT values

We attempted to establish a new level of performance with an FFT-based spectrometer – one with an analog bandwidth of 1 GHz subdivided in 16,384 channels.

For more information, measurement results, and the features of the spectrometer system, visit [www.astro.phys.ethz.ch/instrument/argos/argos\\_nf.html](http://www.astro.phys.ethz.ch/instrument/argos/argos_nf.html).

### Designing the Spectrometer Unit

A detailed block diagram of our spectrometer unit is shown in Figure 2. The analog input signal is fed to a pre-amplifier and analog-to-digital (A/D) converter, which digitizes the signal at a rate of 2 GSPS. The data are transferred to the FPGA through a 32 x 8-bit-wide bus. Next, the FFT frames (32k data samples) are multiplied with a programmable window function and buffered. The complex spectral values are then computed with the aid of two parallel, radix-4 32k-point FFT pipelines. The data are transported continuously in 2 x 4 streams of complex numbers with the system clock  $f_c = 125$  MHz. A 32k FFT frame is processed every 16.384  $\mu$ s.

At the input, the streams have a width of 2 x 9 bits. They are expanded to 2 x 18 bits later within the pipelines, thus maintaining an adequate level of precision and matching the FPGA's RAM and multiplier structures.

After computing the power spectrum, the resulting values are accumulated in 36-bit-wide registers. The number of accumulation cycles is programmable. Hence, a single shot is possible as well.

When an accumulation cycle is completed, the data are flushed to an output buffer. The data is transferred through interrupt or polling over the PCI interface to the host computer.

A number of control and status registers are accessible through PCI, allowing for flexible programming of the whole unit.

### FPGA Utilization

The XC2VP70 comprises 328 block RAM and as many multipliers. In the first design step, we analyzed the need for processing resources. With the guidelines presented here, you can easily determine the number of multipliers.

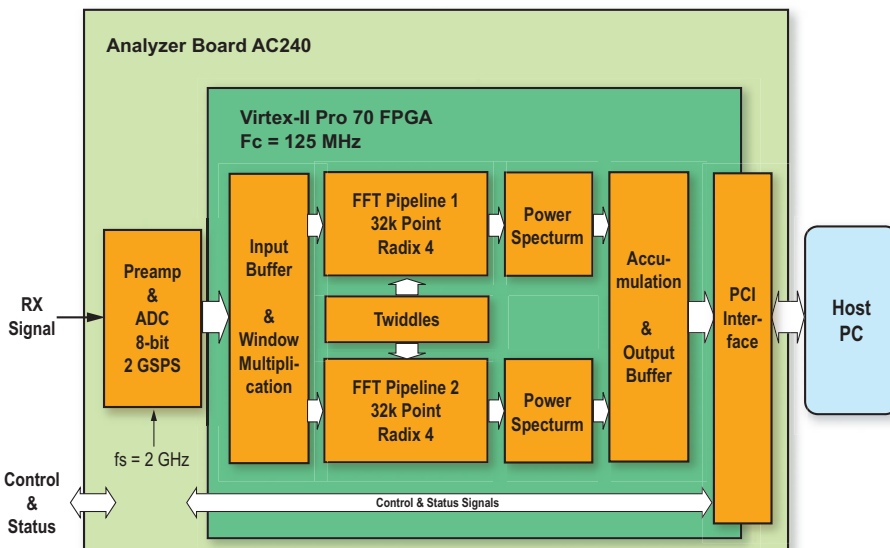


Figure 2 – Spectrometer unit block diagram

A rough estimate of memory is also possible, taking into account all buffer stages at the pipeline's input and output, the data-shuffling stages within the pipelines, and the twiddle and window ROM. However, determining the exact number of RAM blocks requires a detailed stage-by-stage analysis, taking into account the word widths involved. A crucial factor is the granularity of RAM blocks with respect to memory size, number of ports, and configuration possibilities.

Detailed analysis shows that for our spectrometer application, RAM blocks are the most limiting resource. Table 1 summarizes device utilization. All functional units, as shown in Figure 2, are included.

### Managing Timing

Such a complex and time-critical application requires a detailed inspection of every signal path with respect to propagation delay. Throughout the design process, we allocated multipliers and RAM blocks directly in VHDL. All arithmetic elements, RAM blocks, and logic stages are registered consecutively.

We developed the FFT unit in VHDL using the Mentor Graphics tool chain and Xilinx ISE™ software for place and route.

Taking precautions very early in the design stage, we did not apply any location constraints for synthesis and place and route.

Using an XC2VP70 Virtex-II Pro device with speed grade -6, we obtained a minimum clock period of 7.495 ns. Thus, a clock speed of even 133 MHz is feasible.

### Flexible Hardware Platform

Figure 3 shows the hardware platform, an Acqiris AC240 2-GSPS analyzer CompactPCI card. Two interleaved 8-bit A/D converters, with a pre-amplifier stage, provide a configurable sampling

|                            |                      |     |
|----------------------------|----------------------|-----|
| Number of Occupied Slices  | 32,379 out of 33,088 | 98% |
| Number of Slice Flip-Flops | 41,549 out of 66,176 | 63% |
| Number of Block RAMs       | 309 out of 328       | 94% |
| Number of MULT18X18s       | 196 out of 328       | 59% |

Table 1 – FPGA device utilization

rate as high as 2 GSPS. The signal processing core comprises a Virtex-II Pro FPGA. Communication to a host computer is established through the CompactPCI bus.

A firmware development kit (FDK) is included with the AC240. With this concept, you have all of the interfaces avail-

able in a uniform description at the VHDL level. Data input streams, I/O streams through PCI, and front-panel control and status signals are accessible in the VHDL environment. A number of registers are accessible through PCI with driver software. A number of trigger and interrupt mechanisms are also available.

To implement our application, we had to connect the FFT unit to the FDK's interfaces. We found embedding applications in the FDK environment both practical and convenient.

For more information about the hardware, visit [www.acqiris.com](http://www.acqiris.com).

### Conclusion

With our implementation, we established a new level of performance in the field of FFT-based spectrometers. This is possible through an architecture that is highly adapted to the high-speed requirements and signal processing resources available in FPGAs. Block RAM and multipliers are the key elements.

The spectrometer unit has been tested with complete success in the laboratory and in radio astronomy applications. Taking into account the latest developments in FPGA technology in conjunction with faster A/D converters (10 bits at 4 GHz), we may be able to further increase performance. ●●



Figure 3 – AC240 analyzer board with FPGA

**Supporting Your Future**  
**HUNT ENGINEERING**

**USB connected Programmable FPGA systems**

### V-II Pro PowerPC

- **Virtex-II Pro XC2VP7**
- **256 Mbytes DDR Memory**
- **Configurable digital I/Os**
- **PowerPC boot FLASH**
- **USB 2 or Standalone**

### Software Defined Radio

- **Virtex-II FPGA 1M gates**
- **2 ch 125Mps A/D and D/A**
- **TI C6203 DSP**
- **32Mbytes SDRAM**
- **Configurable Digital I/O**
- **USB 2 or Standalone**

### Imaging with Virtex-4FX

- **Virtex-4 FPGA FX12**
- **128Mbytes DDR Memory**
- **CameraLink connection**
- **VHDL and PowerPC Imaging Libs**
- **USB 2 or Standalone**

Programmable hardware with cables, device drivers, loading tools, examples and Power Supply. Systems can be used connected to a PC using USB, or can function standalone (without USB) using the initialisation PROMs.

sales@hunteng.co.uk  
+44 (0)1278 760188

**www.hunt-rtg.com**