

Spartan-DSP Takes Aim at Affordable DSP Performance

The latest addition to the XtremeDSP platform portfolio takes price/performance to a new level.

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The search for the best DSP solution for a given application usually leads designers into a maze of price, performance, and power consumption trade-offs, often requiring a compromise of one or more to accommodate the others. With the introduction of Spartan™-3A DSP, the latest addition to the Xilinx® XtremeDSP™ portfolio and the first Spartan FPGA to be DSP optimized, Xilinx has broken through the maze to deliver the most efficient combination of these three critical values for a host of applications, including wireless base stations, mobile defense communications systems, surveillance, automotive, video, and medical imaging technologies.

Spartan-3A DSP delivers 32 or more GMAC/s (32 billion multiply accumulate operations per second), up to 2,200 Mbps memory bandwidth, and size-reduced packaging. This represents a compelling price/performance breakthrough that hits the mark for applications such as digital front-end (DFE) and baseband solutions in a single-channel picocell wireless base station; military mobile software-defined radios (SDRs); ultrasound systems; driver assistance/media systems; high-definition video; and Smart IP cameras.

Moreover, with as much as 53,712 logic cells, 2,268 Kb of block RAM, 373 Kb of distributed RAM, 519 I/O pins, DeviceDNA for security, and newly developed hibernate/suspend power-manage-

	Spartan-DSP		Virtex-DSP					
	Spartan-3A DSP		Virtex-4 SX FPGA			Virtex-5 SXT FPGA		
	XC3SD1800A	XC3SD3400A	XC4VSX25	XC4VSX35	XC4VSX55	XC5VSX35T	XC5VSX50T	XC5VSX95T
Max DSP Performance (GMAC/s)	21	32	64	96	256	106	158	352
Max Memory Bandwidth (Mbps)	1,736	2,196	4,608	6,912	11,520	3,326	5,227	9,662
Max DSP Frequency (MHz)	250	250	500	500	500	550	550	550
XtremeDSP DSP48 Slices	84	126	128	192	512	192	288	640
Min Footprint (mm)	19 x 19	19 x 19	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27
Distributed RAM (Kb)	260	373	160	240	384	520	780	1,520
Block RAM (Kb)	1,512	2,268	2,304	3,456	5,760	3,024	4,752	8,784
Logic Cells	37,440	53,712	23,040	34,560	55,296	34,816	52,224	94,208

Table 1 – The Spartan-DSP platform fills an important performance slot – the <40 GMAC/s range – in the XtremeDSP platform portfolio.

ment features, Spartan-3A DSP offers enough integration capacity to drive price/performance/power ratios even lower. Add to this the inherent benefits afforded by FPGA-based DSP solutions – lower risk through design flexibility and faster time to market – and the value of the Spartan-DSP platform becomes increasingly apparent (see Table 1).

DSP-Optimized Spartan FPGAs

At the heart of the Spartan-3A DSP is a modified version of the XtremeDSP DSP48 slice – the DSP48A. Initially introduced with the release of Virtex™-4 FPGAs, the DSP48 slice has an Application Specific Modular Block (ASMBL™) architecture that powers the DSP functions in Virtex DSP devices.

These XtremeDSP slices enable designers to implement solutions to complex challenges, such as hundreds of IF-to-baseband down-conversion channels, 128x chip-rate processing for 3G spread spectrum systems, and high-definition H.264 and MPEG-4 encode/decode algorithms in a cost- and power-efficient manner.

The DSP48 slices support many independent functions, including multiplier, multiplier accumulator (MAC), multiplier followed by an adder, three-input adder, barrel shifter, wide bus multiplexers, magnitude comparator, or wide counter. The architecture also supports connecting multiple DSP48 slices to form wide math functions, DSP filters, and complex arithmetic functions without the use of general FPGA fabric, thereby reducing power consumption

while delivering very high performance and efficient silicon utilization.

The Spartan-DSP DSP48A slice is a simplified and cost-reduced version of the Virtex-4 DSP48 slice. To reduce cost, the rounding modes, 17-bit shifters, and 3-input adder modes were removed from the DSP48A slice; you can implement these functions in the FPGA fabric if necessary. Two additional enhancements in the DSP48A slice are a fly-independent C-port and a pre-adder. The independent C-port provides increased flexibility in implementing DSP algorithms. The pre-adder increases density for common DSP filters and FFTs. Specifically, the pre-adder can be used to reduce the number of DSP48A slices that are required by 50% for symmetric FIR filters and by 25% for FFT algorithms, respectively. In the Spartan-3A DSP platform, the optimized DSP48A slice achieves 250 MHz operation in the slowest speed grade.

Application Impact

Typical of the price/performance/power efficiency made possible by Spartan-3A DSP devices, a single XC3SD1800A device can replace two \$25 DSP processors in a Smart IP camera application, absorbing the entire video pipeline section in the process. Besides the immediate \$25 cost reduction, this enables you to place the remaining control functions in a smaller, less expensive DSP processor, thereby dropping the cost of materials by another \$10.

For high-volume consumer applications such as the Smart IP camera or high-definition video, this represents tremendous value to the manufacturer that goes directly to the bottom line. Add to this the savings in power, footprint, and bill of materials (BOM), and Spartan-DSP can have a direct positive impact on profitability, reliability, and product migration.

Similar studies in multi-stream video servers have shown that a design employ-

ing six \$25 DSP processors can be reduced to three \$25 Spartan-3A DSP devices, literally cutting device costs in half. Here again, the positive impact on power, footprint, and BOM is highly appealing.

In some cases, such as SDR for mobile defense communications, the Spartan-3A DSP can serve as a reconfigurable co-processor to a discrete DSP, providing both the aforementioned price/performance/power economies as well as eliminating the need for duplicate circuitry to support multiple waveforms.

Clearly, in every application for which Spartan-DSP is an appropriate platform, the result is greater efficiency in performance, power, and price.

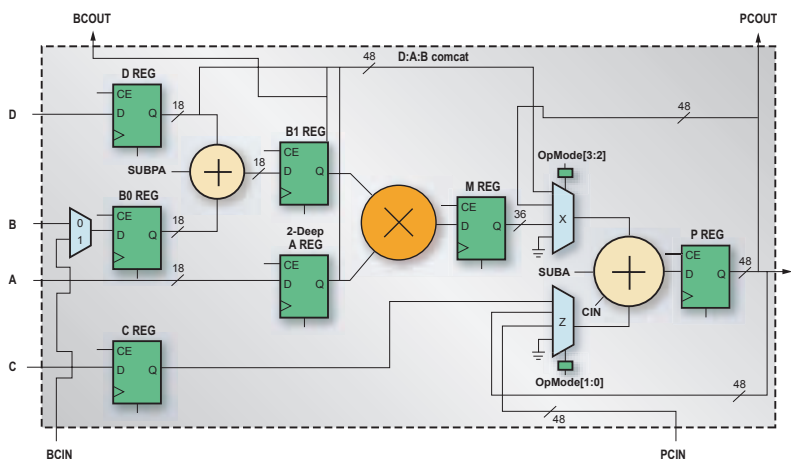


Figure 1 – The pre-adder saves nine slices for every Spartan-DSP DSP48A slice used in a FIR filter design.

XtremeDSP Solutions

The XtremeDSP Initiative, launched in November 2000, gave light to a corporate commitment shared by Xilinx and its partners to make all of the available FPGA-based DSP horsepower and flexibility accessible to three distinct designer profiles: the system designer, the DSP engineer, and the FPGA/hardware engineer. Each profile represents a unique set of responsibilities (and preferences) that dictate the requirements for their particular design environment.

System designers must quickly determine how best to partition the various functions of a system-level design across the available processing resources. Their concerns focus on the selection of processing resources that meet product performance and throughput

requirements while meeting size, cost, and power budgets.

DSP engineers are more focused on the creation and refinement of DSP algorithms. Typically unfamiliar with detailed hardware design, they rely on tools to abstract away the details of hardware design so that they can focus on higher level design exploration and validation.

Hardware engineers usually work in VHDL or Verilog to extract the maximum performance from their designs. They often require the capability to work simultaneously with higher level functional blocks and their own RTL-level design from within the same design environment, running test benches to validate function and performance.

Thus, an essential factor in the success of the XtremeDSP Initiative is the degree to which the design tools accommodate all three profiles. Since the launch of the initiative, XtremeDSP tools such as SystemGenerator and AccelDSP have evolved to provide system modeling, algorithmic development and exploration, automatic generation of test benches, design verification and debugging, and HDL generation and simulation. Whether you prefer to work with VHDL, Verilog, C/C++, MATLAB, Simulink, HDL, or any combination of these, XtremeDSP tools provide fast and efficient access to the full power of the FPGA.

Conclusion

In the DSP marketplace, it is not always the fastest, the least expensive, or the most power-efficient processor that wins: it is the platform that provides the best fit in every category. For a large and growing number of applications, Spartan-3A DSP provides the most efficient combination of price, performance, and power consumption, backed by a robust set of tools, IP, and support infrastructure. If your next DSP design needs extreme efficiency, you may need the latest XtremeDSP solution from Xilinx. 