

Educational Opportunities

Xilinx delivers training that helps you develop low-cost, efficient programmable logic designs.

Choose from a variety of flexible training options, including instructor-led classes (both in person and online) and recorded e-learning that allows you to learn at your own pace.

For tuition and registration information as well as class schedules, please contact an authorized training provider at www.xilinx.com/support/training/atp.htm. For a complete listing of all Xilinx® training opportunities, visit www.xilinx.com/support/education-home.htm.

FPGA Design Courses

- **Fundamentals of FPGA Design** – This course covers ISE™ software 9.1i features, such as the architecture wizard and floorplan editor. Other topics include design planning, implementation options, and global timing constraints. For more emphasis on improving overall design performance,

take the follow-up course, Designing for Performance, which builds on the basic principles covered in this course.

On the Web at www.xilinx.com/support/training/abstracts/fundamentals.htm

- **Design Techniques for Lower Cost** – This course will appeal to engineers who have an interest in developing low-cost products, particularly in high-volume markets. The course and exercises cover several different design techniques, which will be exciting and challenging for any digital designer regardless of the final application.

On the Web at www.xilinx.com/support/training/abstracts/low-cost.htm

CPLD Design Courses

- **Fundamentals of CPLD Design** – This comprehensive course provides

you with an introduction to designing with Xilinx CPLDs by using ISE software tools. You will learn the basics of ISE software flow and how to interpret CPLD reports for optimum performance designs.

On the Web at www.xilinx.com/support/training/abstracts/cpld.htm

- **Designing for Performance for CPLDs** – This intermediate-level course provides a comprehensive overview on CPLD software flow. By applying the techniques presented in this course, you will be able to enhance the performance of your designs and make the best possible use of Xilinx CPLD architectures.

On the Web at www.xilinx.com/support/training/abstracts/dfp_cpld.htm