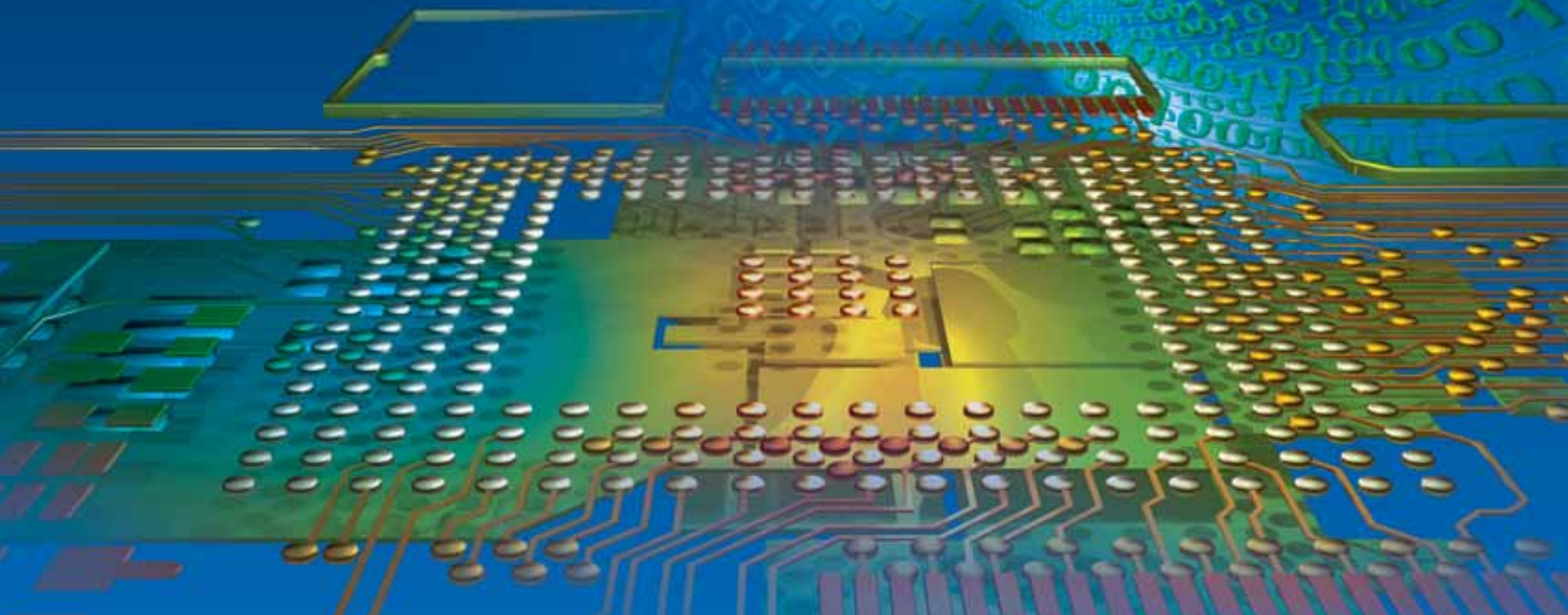




Serial RapidIO Connectivity Enhances DSP Co-Processing

The Virtex-5 LXT FPGA-based SRIO IP solution significantly enhances connectivity by providing a true bi-directional data flow.



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Today, the demand for high-speed communication and super-fast computing is spiraling. Wired and wireless communication standards are being deployed everywhere and the data-processing infrastructure is scaling everyday. The pervasive means of wired communication is Ethernet through LAN, WAN, and MAN networks. The pervasive means of wireless communication is through cell phones, enabled by infrastructures using DSP. What was primarily a means of voice connectivity – the phone – now caters to the ever-increasing demands for voice, video, and data.

System designers must create architectures that will alleviate the exorbitant demands of triple-play scenarios while meeting such requirements as:

- High performance
- Low latency
- Lower system costs (NRE included)
- Scalable, extensible architectures
- Integrating off-the-shelf (OTS) components
- Distributed processing
- Support for multiple standards and protocols

What emerges from these challenges are two primary themes: connectivity

between compute platforms/boxes in wired or wireless infrastructures and the individual computing resources in these platforms/boxes.

Connectivity Between Compute Platforms

Standards-based connectivity is common today. Parallel connectivity standards (PCI, PCI-X, EMIF) may be able to meet current demands, but will come up short when scalability and extensibility are involved. With the advent of packet-based processing, clearly the trend is toward high-speed serial connectivity (Figure 1).

The desktop and networking industries have adopted standards like PCI Express (PCIe) and Gigabit Ethernet/XAUI. Data-processing systems in wireless infra-

structures, however, have slightly different interconnect requirements:

- Low pin counts
- Backplane chip-chip connectivity
- Bandwidth and speed scalability
- DMA and message passing
- Support for complex scalable topologies
- Multicast
- High reliability
- Time-of-day synchronization
- Quality of service (QoS)

The Serial RapidIO (SRIO) protocol standard can easily meet and exceed most of these requirements. As such, SRIO has become the dominant interconnect for data-plane connectivity in wireless infrastructure equipment.

SRIO networks are built around two basic blocks – endpoints and switches (Figure 2). Endpoints source and sink packets, while switches pass packets between ports without interpreting them.

SRIO is specified in a three-layer architectural hierarchy (Figure 3):

- The physical layer specification describes device-level interface specifics such as packet transport mechanisms, flow control, electrical characteristics, and low-level error management.
- The transport layer specification provides the necessary route information for a packet to move from endpoint to endpoint. Switches operate at the transport layer by using device-based routing.
- The logical layer specification defines the overall protocol and packet formats. All packets are 256 payload bytes or less. The transactions use load/store/DMA operations targeted to a 34-/50-/66-bit address space. The transactions include:
 - NREAD – read operation (data returned is the response)
 - NWRITE – write operation, no response

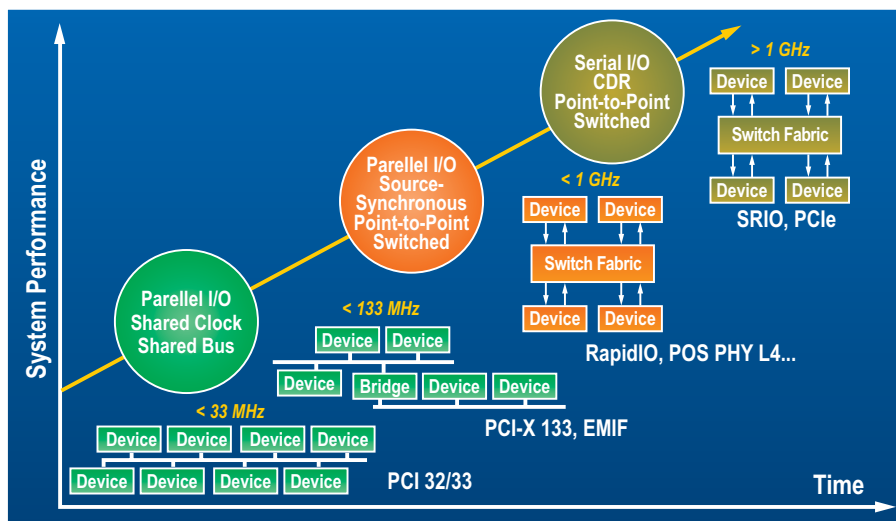
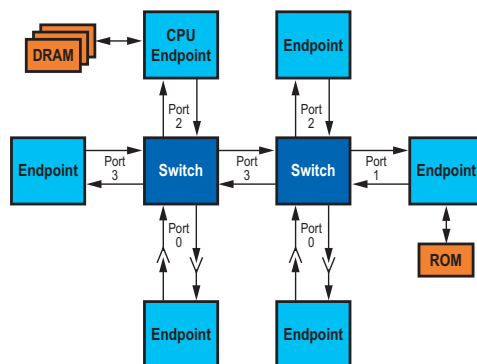


Figure 1 – Trend toward serial connectivity



- SRIO networks are built around two basic blocks:
 - Endpoints
 - Switches
- Endpoints source and sink packets
- Switches pass packets between ports without interpreting them
- All devices support maintenance transactions for access to configuration registers

Figure 2 – SRIO network building blocks

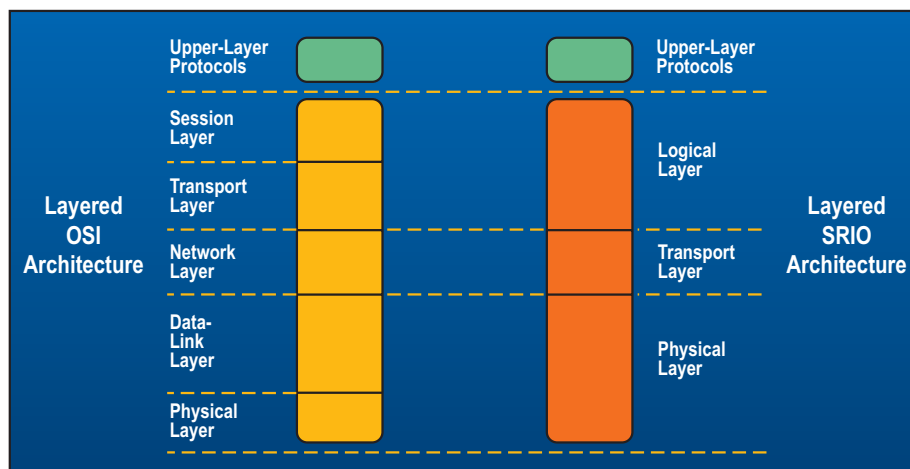


Figure 3 – Layered SRIO architecture

- NWRITE_R – robust write, with response from the target endpoint
- SWRITE – streaming write
- ATOMIC – atomic read-modify-write
- MAINTENANCE – system discovery, exploration, initialization, configuration, and maintenance operations

SRIO – An Advantage Scenario

A four-lane SRIO link running at 3.125 Gbps can deliver 10 Gbps throughput with full data integrity. Because SRIO is similar to microprocessor buses – memory and device addressing instead of the software management of LAN protocols – packet processing is implemented in hardware. This means significantly lower I/O processing overhead, lower latency, and increased system bandwidth. But unlike most bus interfaces, SRIO has low pin count interfaces and scalable bandwidth based on 3.125-Gbps links.

Computing Resources in Platforms

Today's applications demand greater processing resources. Hardware-based implementations are gaining traction. Compression/decompression algorithms, firewall applications like anti-virus and intrusion detection, and security applications requiring encryption engines like AES, Triple DES, and Skipjack have been targeted for hardware implementations after being initially implemented in software. This demands a massive parallel ecosystem of shared bandwidth and processing power. Shared or distributed processing harnessing through systems using CPUs, NPUs, FPGAs, or ASICs is required.

Considering all of these application-specific requirements for building a future-proof system, the requirements for computing resources include:

- Multiple hosts – distributed processing
- Direct peer-to-peer communications
- Multiple heterogeneous OSs
- Complex topologies:
 - Discovery mechanisms
 - Redundant paths (failover)

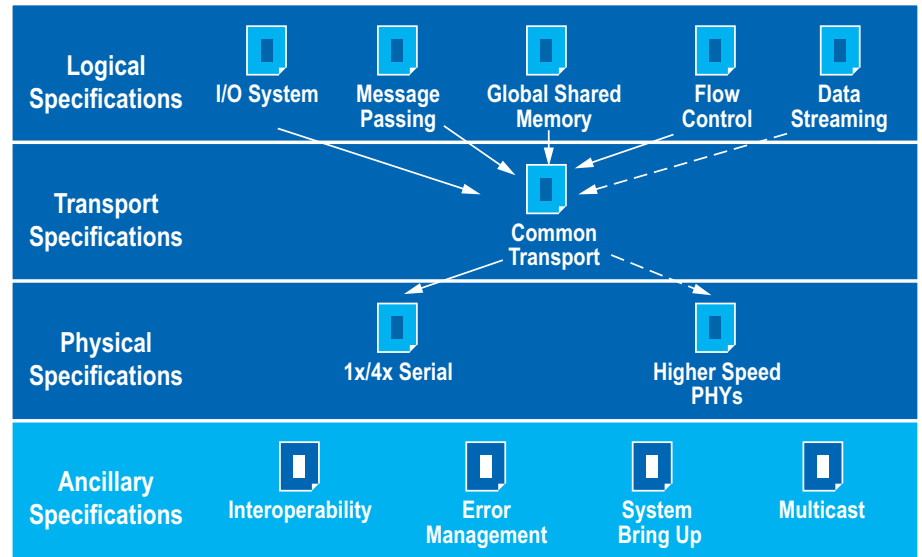


Figure 4 – SRIO specification

- Ability to support high reliability:
 - Lossless protocol
 - Automatic retraining and device synchronization
 - System-level error management
- Ability to support communications data plane:
 - Multicast
 - Traffic-managed (lossy) operation
 - Link, class, and stream-based flow control
 - Protocol interworking
 - Higher transaction concurrency
- Modular and extendable
- Broad ecosystem support

The SRIO protocol was designed to support all of the disparate requirements driven by compute devices in wireless infrastructures.

The SRIO specification (Figure 4) defines a packet-based layered architecture to support multiple domains or market segments for system architects to design next-generation computing platforms. Features like architectural independence, ability to deploy scalable systems with carrier-grade reliability, advanced traffic management, and provisioning for high performance and

throughput can easily be accomplished by adopting SRIO as the computing interconnect. Furthermore, a broad ecosystem of vendors makes the selection of OTS parts and components easy.

SRIO is a packet-based protocol that supports:

- Data movement using packet-based operations (read, write, message)
- I/O non-coherent functions and cache coherence functions
- Efficient interworking and protocol encapsulation through support for data streaming and segmentation and reassembly functions
- A traffic-management framework by enabling millions of streams, support for 256 traffic classes, and lossy operations
- Flow control to support multiple transaction request flows, provision for QoS
- Priorities support to alleviate problems like bandwidth allocation, transaction ordering, and deadlock avoidance
- Topology support for standard (trees and meshes) and arbitrary hardware (daisy-chain) topologies through system discovery, configuration, and bring-up, including support for multiple hosts
- Error management and classification (recoverable, notification, and fatal)

Xilinx IP Solutions for SRIO

Xilinx endpoint IP solutions for SRIO are designed to RapidIO specification v1.3. The complete Xilinx endpoint IP solution for SRIO comprises the following components (Figure 5):

- The Xilinx endpoint IP for SRIO is a soft LogiCORE™ solution. It supports fully compliant maximum-payload operations for both sourcing and receiving user data through target and initiator interfaces on the logical (I/O) and transport layers.
- The buffer layer reference design is provided as source code to perform automatic packet re-prioritization and queuing.
- The SRIO physical layer IP implements link training and initialization, discovery and management, and error and retry recovery mechanisms. Additionally, the high-speed transceivers are instantiated in the physical layer IP to support one- and four-lane SRIO bus links at line rates of 1.25 Gbps, 2.5 Gbps, and 3.125 Gbps.
- The register manager reference design enables the SRIO host device to configure and maintain endpoint device configuration, link status, control, and time-out mechanisms. In addition, ports are provided on the register manager for the user design to probe the status of the endpoint device.

The complete Xilinx endpoint IP LogiCORE solution for SRIO has been exhaustively tested, hardware validated, and is undergoing interoperability testing with leading SRIO device vendors. The LogiCORE IP is delivered through the Xilinx CORE Generator™ software GUI tool that enables user customization for baud rates, endpoint configuration, and support for extended features like flow control, re-transmit suppression, doorbell, and messaging. This enables you to create a flexible, scalable, and customized SRIO endpoint IP optimized for your application.

Virtex-5 FPGA Computing Resources

The Xilinx endpoint IP for SRIO ensures that high-speed connectivity is established between the link partner using the SRIO protocol. The IP consumes <20% of the available logic resources in the smallest Virtex™-5 device, thereby ensuring that the user design has access to the most logic/memory/I/Os for targeting a system application. Let's review the resources in Virtex-5 devices.

Logic Blocks

The Virtex-5 logic architecture, with six-input look-up tables (LUTs) based on the 65-nm process, offers the highest FPGA capacity. Along with improved carry logic, this provides a 30% performance benefit over previous devices. Power consumption is significantly lowered

because fewer LUTs are required, and the device has a highly optimized symmetric routing architecture.

Memory

Virtex-5 memory solutions include LUT RAMs, block RAMs, and memory controllers for interfacing to large memories. The block RAM structure includes pre-engineered FIFO logic – embedded error checking and correction (ECC) logic that can be used for external memories. In addition, Xilinx provides comprehensive design resources to instantiate memory controller blocks in a system design through the Memory Interface Generator (MIG) tool. This enables you to leverage hardware-verified solutions and focus your efforts on other crucial sections of your designs.

Parallel and Serial I/Os

SelectIO™ technology is capable of virtually any parallel source-synchronous interface the customer needs in the design. Using the SelectIO interface, you can easily create industry-standard interfaces for more than 40 different electrical standards or proprietary interfaces. The SelectIO interface offers maximum rates at 700 Mbps single-ended and 1.25 Gbps differential.

All Virtex-5 LXT FPGAs have a GTP transceiver capable of running at speeds from 100 Mbps to 3.2 Gbps. The GTP transceiver is also one of the industry's lowest power MGTs, with less than 100 mW per transceiver. The design flow process for high-speed serial design is alleviated by the introduction of proven design techniques and methodologies to simplify the design.

In addition, new design tools (RocketIO™ transceiver wizard and IBERT) and new silicon capabilities (TX and RX equalization and built-in pseudo-random bit sequence (PRBS) generator and checker) allow you to exploit the features and benefits of migrating architectures from parallel I/O standards to more than 30 serial standards and emerging serial technologies.

DSP Blocks

Each DSP48E slice can provide 550-MHz performance, enabling you to create appli-

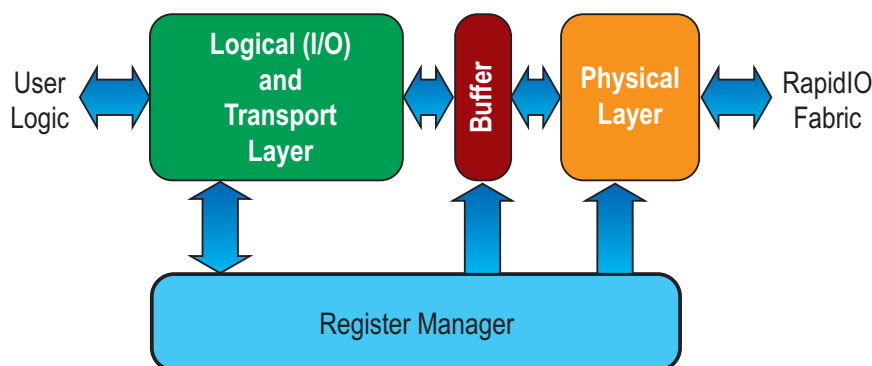


Figure 5 – Xilinx endpoint IP architecture for SRIO



cations that require single-precision floating-point capability like multimedia, video and imaging applications, and digital communications. This provides expanded functionality compared to previous devices as well as providing a power advantage by reducing dynamic power consumption by more than 40%. The number of DSP48E slices has also been increased in Virtex-5 FPGAs, which optimizes the ratio of these blocks relative to the available logic resources and memory.

Integrated I/O Blocks

All Virtex-5 LXT FPGA devices have one endpoint block for implementing a PCIe function. This hard IP endpoint block enables easy scalability from x1 to x2 and x4 or x8 painlessly with easy reconfigurability. The block has also passed stringent PCI-SIG compliance and interoperability tests for x1, x4, and x8 links, considerably easing the user adoption for PCIe.

All Virtex-5 LXT FPGA devices also have four tri-mode Ethernet media access controllers (TEMACs) capable of 10-/100-/1,000-Mbps speeds. The block provides dedicated Ethernet functionality, which together with Virtex-5 LXT RocketIO transceivers and SelectIO technology enables you to connect to a wide variety of network devices.

Using the two integrated I/O blocks for PCIe and Ethernet, you can create a range of customized packet processing and network products that provide a significant reduction in utilization and power consumption. Using these varied resources available in Xilinx FPGAs, you can easily create and deploy intelligent solutions.

Let's look at some system design examples using SRIO and DSP technologies.

SRIO Embedded System Application

Consider an embedded system built around x86 architecture-based CPUs. The CPU architecture has been highly optimized and can easily cater to applications requiring "number crunching." You can easily implement algorithms in hardware and software that use CPU resources to perform functions like e-mail, database management, and word processing that do not require extensive multiplication.

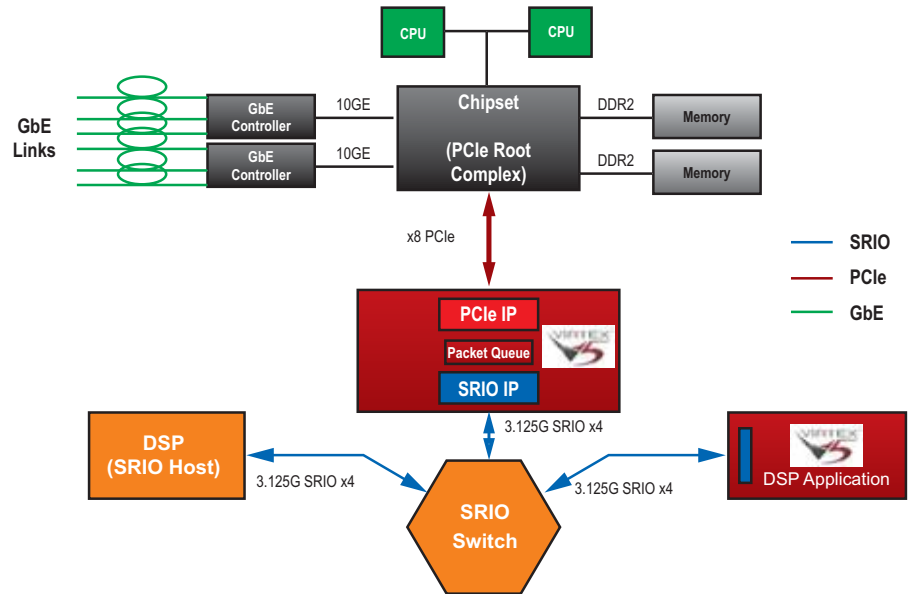


Figure 6 – CPU-based scalable, high-performance embedded system

Performance is measured in millions or billions of instructions/operations per second and efficiency is measured in terms of time/cycles required to complete a specific operation.

High-performance applications requiring a wide range of fixed- and floating-point operations take longer to process the data. Examples include signal filtering, fast Fourier transforms, vector multiplication and searching, image/video analysis and format conversion, and simple number-crunching algorithms. High-end signal processing architectures implemented in DSPs can easily perform these tasks and optimize such operations. The performance of these DSPs is measured in multiply-accumulates per second.

You can easily design embedded systems that use CPUs and DSPs to take advantage of both processing techniques. Figure 6 shows an example system using FPGAs, CPUs, and DSP architectures.

In high-end DSPs, the primary data interconnect is SRIO. In x86 CPUs, the primary data interconnect is PCIe. As shown in Figure 6, FPGAs can easily be deployed for scaling the DSP application or for bridging across disparate data interconnect standards, like PCIe and SRIO.

In the system depicted in Figure 6, the PCIe system is hosted by the root complex

chip set. The SRIO system is hosted by a DSP. The 32-/64-bit PCIe address space (base address) can be intelligently mapped to the 34-/66-bit SRIO address space (base address). The PCIe application communicates with the root complex through memory or I/O reads and writes. These transactions can be easily mapped to SRIO space through NReads/NWrites/SWrites.

Designing such bridge functions is easy in Xilinx FPGAs because the back-end interfaces for these Xilinx endpoint functional blocks, PCIe, and SRIO are similar. The "packet-queue" block can then perform the crossover from PCIe to SRIO or vice-versa to establish packet flow across either protocol domain.

SRIO DSP System Application

In applications where DSP processing is the primary architectural requirement, the system architecture can be designed as depicted in Figure 7.

Virtex-5 FPGA-based DSP processing can act as an intelligent co-processing solution with other DSP devices in the system. The complete DSP system solution can be scaled easily if SRIO is used as the data interconnect. Such solutions can be future-proofed, provide extensibility, and can be supported across multiple form factors. In DSP-intensive applications, fast number

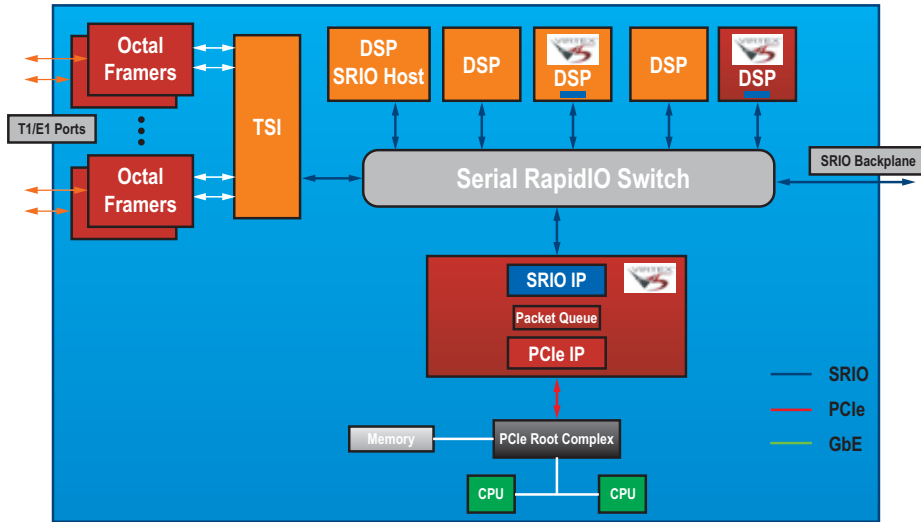


Figure 7 – DSP-intensive farms

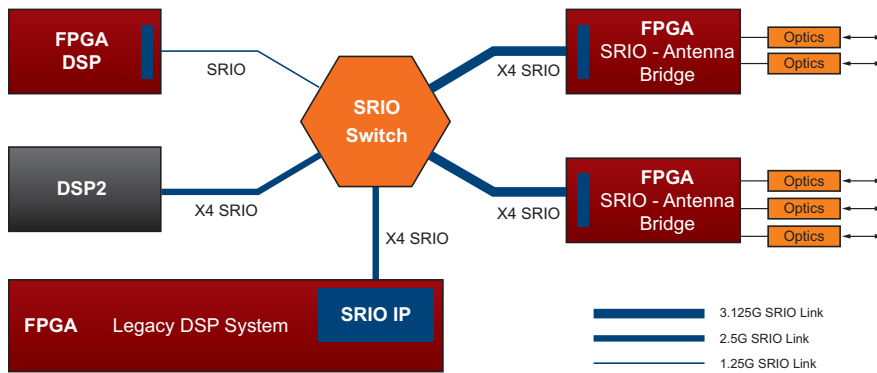


Figure 8 – Scalable baseband uplink/downlink card

crunching or data processing can be accomplished by offloading that processing to the x86 architectures. The Virtex-5 FPGA can be easily used to connect the PCIe subsystem and SRIO architecture to enable efficient function offload.

SRIO Baseband System Application

Existing 3G networks are beginning to mature at a rapid pace and OEMs are deploying new form-factors to alleviate specific capacity and coverage problems. To solve such unique challenges to assess market trends, FPGA-based DSP architectures using SRIO as the data-plane standard makes perfect sense. In addition, legacy DSP systems can be quickly provisioned and targeted to new, fast, low-power FPGA DSP

architectures to gain scalability advantages.

As shown in the system depicted in Figure 8, you can design Virtex-5 FPGAs to meet existing demands of line-rate processing of antenna traffic and also provide connectivity to other system resources through SRIO. Migrating existing legacy DSP applications, which have inherently

slow parallel connectivity, is easy because of the SRIO endpoint functions that can be targeted to Virtex-5 FPGAs.

Conclusion

SRIO is appearing in a wide array of new applications, largely centered around DSPs in wired and wireless applications. The key advantages of implementing SRIO architectures in Xilinx devices are:

- Availability of complete SRIO endpoint solution
- Flexibility and scalability to produce different classes of products with the same hardware and software architecture
- Low power with new GTP transceivers and 65-nm technologies
- Easy configurability through the CORE Generator software GUI tool
- Proven hardware interoperability with leading industry vendors supporting SRIO connectivity on their devices
- Lower overall system cost by achieving system integration through use of integrated I/O blocks like PCIe and TEMAC

In addition, Virtex-5 FPGAs have DSP resources that can meet the requirements of existing legacy DSP systems in terms of power, performance, and bandwidth. Additional benefits accrue in terms of system integration – through availability of functional blocks like Ethernet MACs, endpoint blocks for PCIe, processor IP blocks, memory elements, and controllers. Also, you can achieve significant overall system cost savings through the exhaustive list of IP cores to support multiple source aggregation in the FPGA. 🌟

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