



The NXP/PLDA Programmable PCI Express Solution

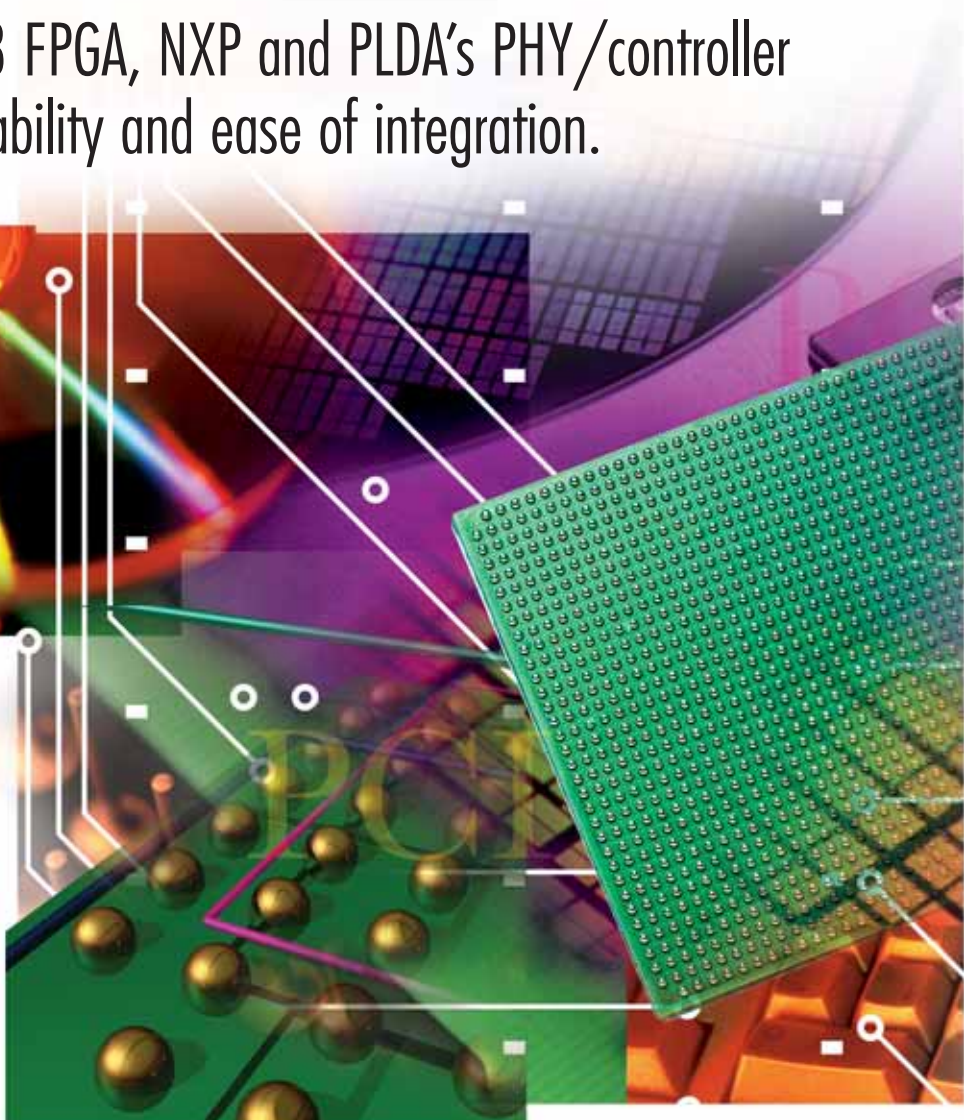
Based on the Spartan-3 FPGA, NXP and PLDA's PHY/controller solution delivers affordability and ease of integration.

by Ho Wai Wong-Lam
Marketing Manager
NXP Semiconductors
ho.wai.wong-lam@nxp.com

Martin Gallezot
Marketing and Sales Director
PLDA
mgallezot@plda.com

Developers today are increasingly squeezed between providing ever-greater throughput for data-hungry applications and shrinking product lifecycles. Take frame grabber products, for example, which are image-processing computer boards that capture, process, and store image data for a wide range of scientific, medical, and industrial applications. Advances in image sensing continue to put a greater demand on the interconnect bandwidth as the number of pixels, frame rates, and number of cameras served by a single frame grabber increases. Some applications already require throughput exceeding 1 Gbps.

To meet the demands of today's development environment, companies are adopting PCI Express, the next-generation I/O interconnect technology of choice, and increasingly relying on FPGA-based interoperable, proven solutions that reduce the integration risk and decrease a product's time to market.



PCI Express is designed to replace PCI and PCI-X interconnect technologies, providing a scalable bandwidth from x1 at 250 Mbps to x32 at 8 Gbps. The v2.0 specification further increases bandwidth by doubling the one-lane data rate from 2.5 Gbps in the v1.1 specification to 5 Gbps. Besides increased throughput, PCI Express offers a smaller connector than PCI/PCI-X, which lowers costs and eases

PCB routing. And to ease the transition from PCI/PCI-X, PCI Express is backward-compatible with PCI with regards to software performance.

Interoperable solutions such as the NXP PHY/PLDA IP controller offer the advantages of PCI Express coupled with the security of a PCI-SIG-proven solution, allowing you to concentrate on application-specific functionality.

NXP's PX1012A

NXP Semiconductors (previously Philips Semiconductors) offers the PX1012A single-lane 2.5-Gbps PCI Express PHY device, which serves as a companion chip to FPGAs or digital ASICs. The PX1012A is ideal for use with PLDA's XpressLite PCI Express IP core.

The PX1012A is optimized for use with low-cost FPGAs. It is available in a very small package, delivers superior transmit and receive performance, and is compliant to PCI Express specifications v1.0a and v1.1. The PX1012A is designed to serve PCI Express applications in all kinds of form factors, from space-constrained and low-power ExpressCard modules to desktop add-on cards to PXIe test equipment rack add-on modules. The NXP PCI Express PHY PX1012A has the following key features:

- Compliant to PCI Express base specification v1.0a and v1.1; the NXP PHY passed the first official U.S. PCI-SIG v1.1 electrical compliance tests in December 2006.
- The Xilinx® Spartan™-3 FPGA communicates with the PX1012A PHY using the source-synchronous 250-MHz PXPIPE standard, based on SSTL_2 I/O. The use of source-synchronous clocking eases PCB layout by making the data transactions between the FPGA and PHY devices more robust than the original PIPE standard, which uses only one clock for both transmit and receive data.
- A small 9 x 9-mm BGA package with two signal rings (so that only one inner-ring signal needs to escape between the balls). In fact, the NXP PHY can be laid out with just two PCB signal layers, which have been proven in actual hardware designs. Example reference schematics are available on request.
- Low power dissipation in normal L0 mode (typically <300 mW including I/O). For further reduction in power dissipation, the removal of termination resistors on the PHY/FPGA interface and optimized PCB layout can further reduce PX1012A power dissipation to <150 mW.

- Both commercial temperature grade (0 to 70°C) and industrial grade (-40 to 85°C) are available; this is a unique industrial temperature grade device for PCI Express PHY, making NXP PHY suitable for various industrial applications.

PLDA's XpressLite IP Core

PLDA's XpressLite PCI Express IP core is a complete PCIe digital controller optimized for Spartan-3 FPGAs. It includes all three layers of the PCIe specification (physical, data link, and transaction layer), plus an additional application layer called the EZ DMA interface.

PLDA's EZ DMA interface is suitable for designers who have little or no experience with the PCI Express protocol or for experienced designers looking for a robust yet simple PCI Express interface. The EZ DMA interface provides designers with a target path, which includes a simple address/data bus, and a master path, which comprises multiple DMA engines that handle the transfer of data to the host system memory. The EZ DMA interface can also be used together with the built-in PCI Express controller in Virtex™-5 LXT devices.

The XpressLite controller is an RTL-level IP core fully compliant with the PCI Express protocol. As required, the configuration space (located within the transaction layer) implements all configuration registers and associated functions. The configuration space also generates all messages (PME#, INT, error, power slot limit), MSI requests, and completion packets from configuration requests that flow in the direction of the root complex.

The XpressLite is fully configurable through a graphical wizard, making it simple to customize such parameters as maximum payload size, configuration space registers, buffer sizes, and number of DMA channels. The wizard generates a wrapper that instantiates the core top level and connects ports and assigns parameters according to specified options. Unused core features are not synthesized.

The XpressLite is PCIe specification 1.1-compliant. It has a small footprint and minimal memory utilization. Typical implementation requires about 8,000 LUTs and seven block RAMs in a Spartan-3 device. These figures include the EZ multi-DMA application layer configured with two DMA channels. PCI Express features supported by the XpressLite controller are summarized in Table 1.

Core Type	Legacy or Native Endpoint
Maximum Payload	Up to 2 KB
Backend Data Path	64 bit
Virtual Channels	One
BARs, Expansion ROM	User-defined, set by the XpressLite wizard
PCI ID	User-defined, set by the XpressLite wizard
Legacy Power Management	Minimal or full, set by the XpressLite wizard
Message Signaled Interrupt (MSI)	<ul style="list-style-type: none"> • Message count: 1 to 32, set by the the XpressLite wizard • 64-bit address: Yes • Per-vector masking: No
EZ Multi-DMA Interface	<ul style="list-style-type: none"> • DMA channels: up to eight, set by the XpressLite wizard • Number of outstanding requests: one to eight simultaneous requests, set by the XpressLite wizard • Maximum DMA transfer size: up to 4 GB

Table 1 – PCI Express features supported by the XpressLite controller



PLDA's core package also includes a complete test bench with an RTL-level PCI Express bus functional model (BFM), transactor, monitor, and checker.

Fully Compliant and Interoperable Solution

The NXP/PLDA joint solution successfully completed PCI Express compliance tests administered at the PCI-SIG Compliance Workshop #48 in December 2005 and later workshops in 2006 (see transmitter eye pattern results in Figure 1).

NXP, PLDA, and mutual customers have run extensive and successful system tests in a multitude of PC systems, including:

- ASUS A8NE (x16, two x1 slots and one x4 slot)
- ASUS P5GP motherboard (Intel 915G chipset)
- ASUS P5LD2 DELUXE (Intel i945 chipset)
- Dell Dimension 4700 x1 and x16 slots (Intel 915G chipset)
- Dell Dimension 8400 (Intel 925G chipset)
- DELL Precision 370
- Dell Precision 470 x8 and x16 slots (Intel Turnwater E7525 chipset)
- HP XW4200
- HP XW4300
- MSI (Intel i915 chipset)
- Serverworks GC-SL
- Shuttle ATI Express 200 chipset
- Supermicro X6DA8G (x16 and x4 slots)

In addition to the standard PCI-SIG compliance tests, NXP and PLDA also used a variety of system tests developed internally and from third-party test equipment vendors:

- PCI scan diagnostic utility
- Transmitter electrical compliance tests v1.0a and v1.1
- PCI-SIG PCI-ECV v1.2

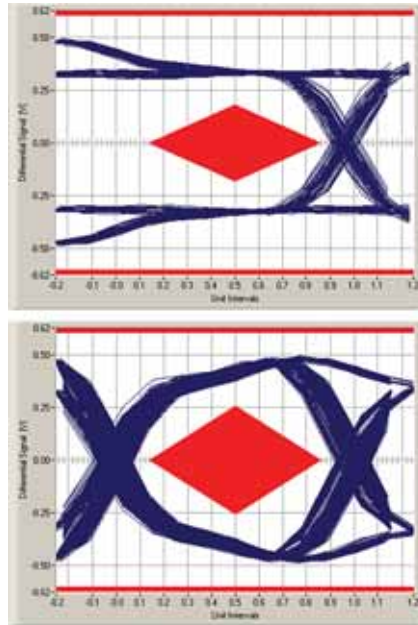


Figure 1 – PLDA XpressLite SP3 board transmitter eye pattern with v1.1 PCI Express template (top: non-transition eye; bottom: transition eye)

- Agilent protocol test card (PTC) test
- Agilent receiver bit error rate (BER) test
- NXP receiver performance test
- PLDA throughput measurement test

High Throughput

Theoretical maximum throughput is a function of payload size and PCI Express protocol overhead. Actual throughput results depend on factors such as software driver efficiency, PCI Express IP core efficiency, the user's application design, transmitter jitter, and receiver BER performance. Throughput might be further compromised by link-layer protocol overhead such as ACK/NAK packets (acknowledge/non-acknowledge), re-transmitted packets, and flow control protocol (credit reporting).

Theoretical Maximum Throughput

The line speed of one-lane PCI Express is 2.5 Gbps. However, 8B/10B encoding overhead reduces the maximum PXPIPE data throughput (2.5 Gbps divided by 10 bits per byte = 250 Mbps). Given the overhead performance cost, throughput typically increases with payload size – up to a point. For example, for a payload of 128 bytes, the theoretical efficiency is 86% (128 B(ytes) payload + 12B header + 8B framing) and the maximum theoretical throughput is 216 Mbps. Although the PCI Express specification specifies a potential maximum payload size of as much as 4 KB, most existing applications only implement a maximum payload size of 128B or 256B. Throughput measurements for the NXP/PLDA solution are listed in Table 2.

Receiver Performance

NXP and PLDA have performed extensive proprietary system tests in many PC systems to ensure that there are no recoverable receiver errors for extended periods of time (many hours). Test results yield a BER of 1×10^{-12} .

PCI Express specifications v1.0a and v1.1 require 0.6 UI (unit interval) of receiver jitter tolerance, but the specifications do not precisely indicate how the jitter components are composed. NXP performed receiver BER tests using an Agilent BER tester.

- Agilent J-BERT N4903A
- TJ = total jitter; RJ = random jitter; PJ = periodic jitter; DDJ = data-dependent jitter; UI = unit interval; ISI = inter-symbol interference; BER
- $0.60\text{UI TJ} = 0.25\text{UI RJ} + 0.25\text{UI PJ}$ (at 15 MHz) + 0.1UI DDJ

PCIe PHY	IP Core	Computer Platform	Payload	Throughput	Throughput
				DMA Read (Card->PC)	DMA Write (PC->Card)
PX1012A	PLDA	ASUS A8NE Supermicro X6DA8G	128 bytes	200 Mbps	175 Mbps

Table 2 – Throughput measurement results



Figure 2 – The PLDA XpressLite SP3 is based on a Xilinx Spartan-3 FPGA and includes NXP's PCIe PX1012A PHY and PLDA's XpressLite IP controller.

- 0.1 UI DDJ = ISI module, which stimulates 9 inches of PCB trace, equivalent to about 0.1-UI jitter and significant amplitude degradation.

NXP obtained excellent receiver performance results with the Agilent bit error tester.

- PX1012A achieved $< 1 \times 10^{-12}$ BER with a 800-mV_{diff. p-p} input signal, which is the minimum transmit output level allowed by the PCI Express specification. The 800-mV_{diff. p-p} signal goes from the pattern generator to the BERT ISI module before feeding into the PHY receiver.
- Without the ISI module, the PX1012A can achieve $< 1 \times 10^{-12}$ BER with a 400-mV_{diff. p-p} input signal.

PLDA XpressLite SP3 Design Kit

The PLDA XpressLite SP3 Design Kit (see Figure 2) is based on a Spartan-3 FPGA (XC3S2000 device) and integrates the NXP PX1012A. The design kit includes a Protocore (board-only) license of the PLDA XpressLite IP core.

The Protocore license is a full-featured RTL-level license that is valid for an unlimited duration when used with the design kit. It also includes a software development kit, with a library of C source code func-

tions and a driver. With the Protocore license, you can freely simulate and synthesize your own design connected to the XpressLite IP core and re-program the FPGA device accordingly.

The complete design has gone through extensive validation testing, is hardware-proven, and readily available for customer prototyping.

The XpressLite SP3 design kit provides a low-cost solution to prototype your design with PCI Express. It can also be used as part of your final product if you want to save the effort of designing your own PCIe board. A 400-hole matrix (2.54-mm step) for prototyping and probing purposes is also provided.

Conclusion

A prototyping board like PLDA's XpressLite SP3 Design Kit, which combines the power of the Xilinx Spartan-3 FPGA with a proven PCI Express NXP PHY/PLDA IP controller solution, responds to today's development challenges to produce applications that support ever greater data throughput in an ever-shrinking product lifecycle. For more information, visit www.standardics.nxp.com/products/pci/phys/ and www.plda.com/products/board_pcie_sp3.php.

NXP also provides a joint solution with the Xilinx PCI Express PIPE core for Spartan-3 FPGAs. You can buy this solution from Xilinx, which includes an x1 PCI Express add-in card and an evaluation version of the PIPE core.

GET PUBLISHED



WOULD YOU LIKE TO BE PUBLISHED IN XCELL PUBLICATIONS?

It's easier than you think!

Submit an article draft for our Web-based or printed Xcell Publications and we will assign an editor and a graphic artist to work with you to make your work look as good as possible.

For more information on this exciting and highly rewarding program, please contact:

Forrest Couch
 Publisher, Xcell Publications
xcell@xilinx.com

