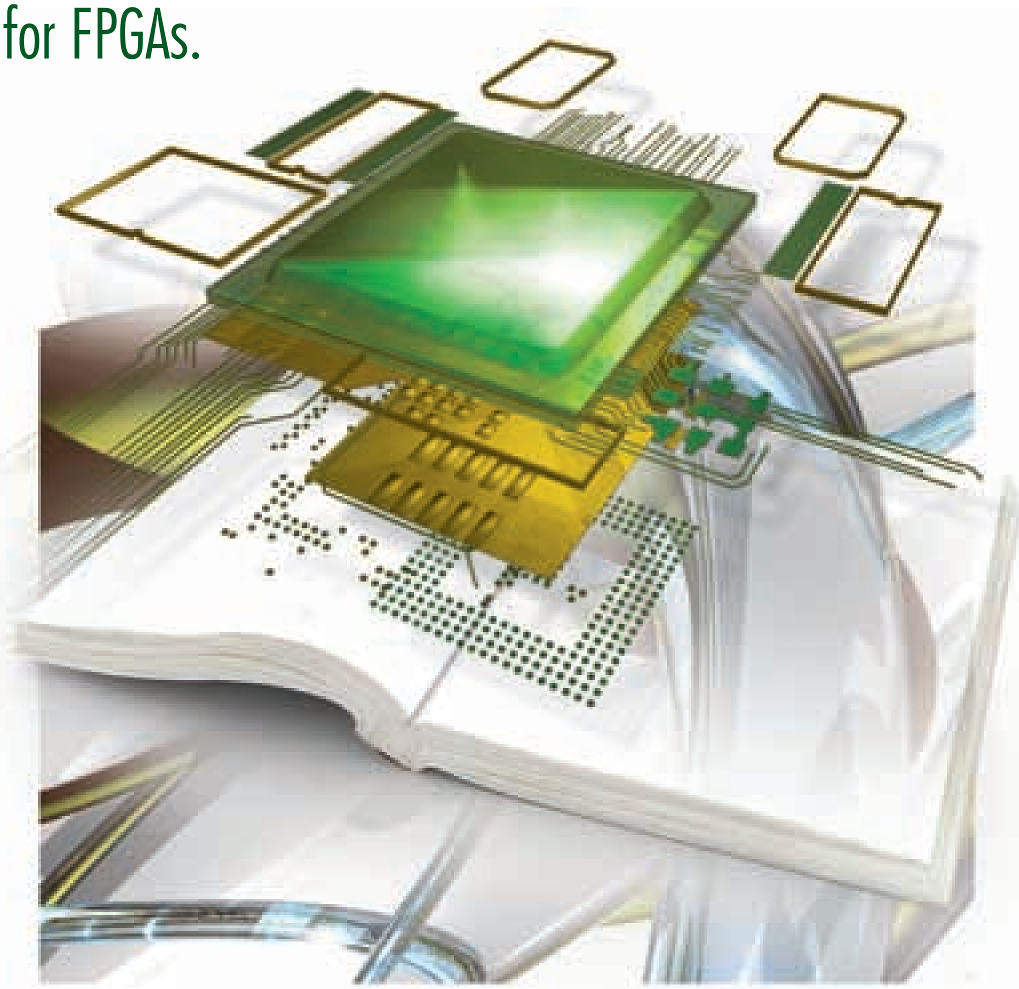
DSP Performance of FPGAs Revealed

Popular report provides independent DSP benchmark results for FPGAs.



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FPGAs are increasingly considered for use as processing engines in high-performance DSP applications such as wireless base stations. In these applications, they may compete with DSP processors or work side-by-side with them.

With more choices, system designers need a clear picture of the signal processing performance of high-end FPGAs, both relative to each other and to high-end DSP processors. Unfortunately, the most commonly used performance figures are unreliable, confusing, and often contradictory.

For example, because DSP applications often rely heavily on multiply accumulate (MAC) operations, DSP processor and FPGA vendors sometimes use peak MACs per second as a simple metric for comparing digital signal processing performance. But MAC throughput is a lousy predictor of performance for FPGAs and DSPs alike. Let's examine a few reasons why.

Simple Metrics Fall Short

The MAC performance numbers for FPGAs often assume that the hard-wired DSP elements are operating at their highest possible clock rate. In practice, typical FPGA designs will operate at lower speeds. Plus, using hard-wired elements is not the only way to implement MACs on FPGAs; you can achieve additional MAC throughput using programmable logic resources and distributed arithmetic. This approach can yield higher MAC throughput than using hard-wired elements alone.

Yet another consideration is that typical DSP applications rely on many operations other than MACs. Viterbi decoding, for example, is a key DSP algorithm used in telecommunications applications that makes no use of MACs at all.

Another approach for assessing signal processing performance is to use common DSP functions like FIR filters. But this approach can have drawbacks too. One problem is that each vendor typically uses a different implementation of these functions – perhaps using different data widths, a different algorithm, or different implementation parameters such as latency. This means that results from different vendors are generally not comparable.

Furthermore, small kernel functions typically aren't effective for FPGA benchmarking because the way you would implement a function within a full FPGA application is often quite different from the way you would implement the function alone. (For processors, in contrast, these little benchmarks are usually pretty good at predicting overall DSP application performance.) Benchmarks implemented by processor or FPGA vendors often lack independent verification, making it difficult for engineers to make confident comparisons between devices.

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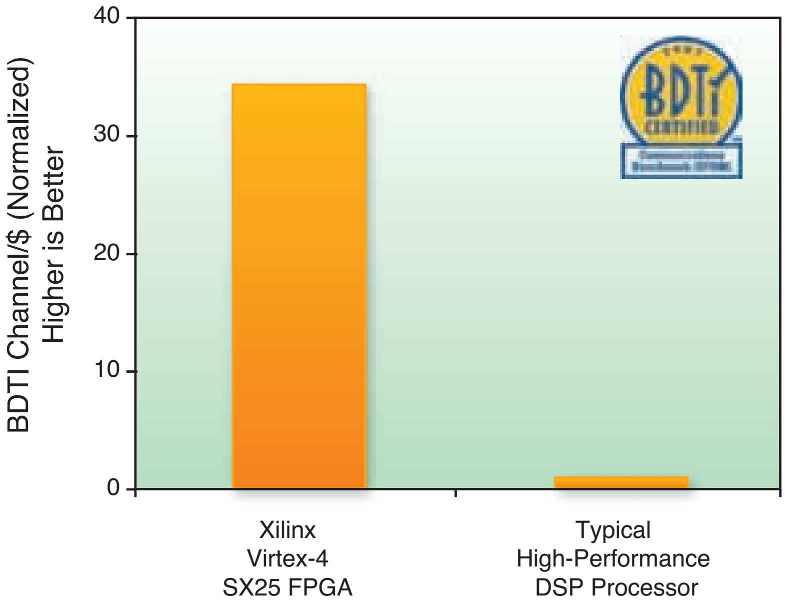


Figure 1 – BDTI Communications Benchmark (OFDM)
BDTI-certified cost-/performance-optimized results

Independent Benchmarks Fill the Gap

BDTI is the most respected source for signal processing benchmarks. Our benchmarks are used by dozens of semiconductor vendors and thousands of chip users to evaluate, compare, and select signal processing engines. BDTI has benchmarked the signal processing performance of processors for nearly 15 years, and has expanded its benchmarking activities to include FPGAs, multi-core chips, and other technologies.

Several years ago BDTI recognized the need for independent, accurate, apples-to-apples performance comparisons between FPGAs and processors targeting DSP applications. To address this need, BDTI developed a new application-oriented benchmark, the BDTI Communications Benchmark (OFDM), based on an orthogonal frequency division multiplexing (OFDM) receiver. This benchmark is designed to be representative of the "baseband" signal processing workloads increasingly found in communications equipment for applications such as DSL, cable modems, and wireless systems. It is suitable for implementation on FPGAs, DSP processors, multi-core chips, and many other signal processing engines, yielding apples-to-apples benchmark results.

Last year, BDTI used the BDTI Communications Benchmark (OFDM) to evaluate several new high-performance FPGAs and DSP processors. The full results of this analysis are published in our report, "FPGAs for DSP: Second Edition," which has attracted considerable attention among DSP system designers. The report includes two sets of benchmark results: high-capacity results (optimized to support the maximum number of channels per chip) and low-cost results (optimized for lowest cost per channel). Figure 1 shows normalized, low-cost results for a Xilinx® Virtex™-4 SX25 FPGA and a typical high-performance DSP processor.

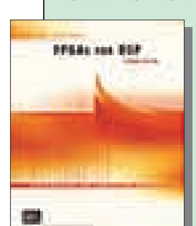
As Figure 1 demonstrates, BDTI's benchmark results provide a dramatic demonstration of the potential cost advantages of using FPGAs for high-performance DSP applications. The Virtex-4 SX25 device is more cost-effective by more than an order of magnitude over a typical high-performance DSP processor on this benchmark. This information is extremely valuable for system designers, who may have suspected that FPGAs could provide better chip-level cost/performance than DSPs in some applications but were not sure how much better. In the report, BDTI also compares cost/performance results for FPGAs from competing vendors.

Of course, benchmark results alone are not enough to answer the question of whether to use an FPGA in a new system design, or which FPGA to choose. Designers need to understand how their choice of processing engine will affect development flow, implementation effort, and system design. For this reason, BDTI's report explores the qualitative factors that influence the decision of whether to use an FPGA, a DSP, or both, and provides guidance on how to make an informed choice. The report also highlights the key questions that will affect the long-term success of FPGAs in high-end DSP applications, such as FPGA energy efficiency and the effectiveness of new high-level synthesis tools for FPGAs.

Conclusion

BDTI plans to conduct further analysis in these areas and we will continue to evaluate the signal processing capabilities of new FPGAs, DSPs, and massively parallel processors. The competition among signal processing engines is heating up, and BDTI will continue to provide the data and analysis needed to make confident choices.

BDTI's report, "FPGAs for DSP, Second Edition," is the authoritative source for independent FPGA signal processing benchmark results. *Xcell Journal* readers can request detailed report excerpts via e-mail; send your request to *fpga_samples@BDTI.com*.



For more information about "FPGAs for DSP, Second Edition" (including an order form), visit *www.BDTI.com/fpgas2006*. For more information about BDTI, visit *www.BDTI.com*.