The Virtex-5 SXT Option for High-Performance Digital Signal Processing

Understanding the demand for high-performance DSP.

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The thirst for data in the information age is driving digital convergence. Triple-play, medical imaging, image processing, defense, aerospace, security, and encryption require higher performance digital signal processing (DSP), putting a strain on traditional solutions, technologies, and techniques.

To understand this, you need only explore the technology advances and resulting increases in algorithm complexity that strain existing solutions. Figure 1 illustrates this point with Shannon's limit, the theoretical maximum information transfer rate of a communications channel at given noise level. As Figure 1 shows, traditional general-purpose processors (GPP) and DSP solutions are unable to efficiently address this limit.

The alternative is to implement digital signal processing algorithms using FPGA technology, enabling performance increases up to an order of magnitude over traditional solutions. The Xilinx® Virtex™-5 SXT device family has been designed to address this alternative FPGA approach, providing a unique ratio of resources to efficiently enable the highest performance digital signal processing possible.

Traditional DSP Versus FPGA DSP

Break up even the most complex DSP algorithm to its atomic parts and you'll find multipliers, adders, and some delay element. By combining these basic elements, you can implement even the most complex DSP algorithms.

Traditional DSP solutions combine sequential control logic with a number of arithmetic logic units (ALUs). The ALUs provide the multiply add capability, while the sequential control logic enables code interpretation and control. Bandwidth is determined by the frequency of the system and the number of ALUs that can run in parallel. A solution that runs at a base fre-

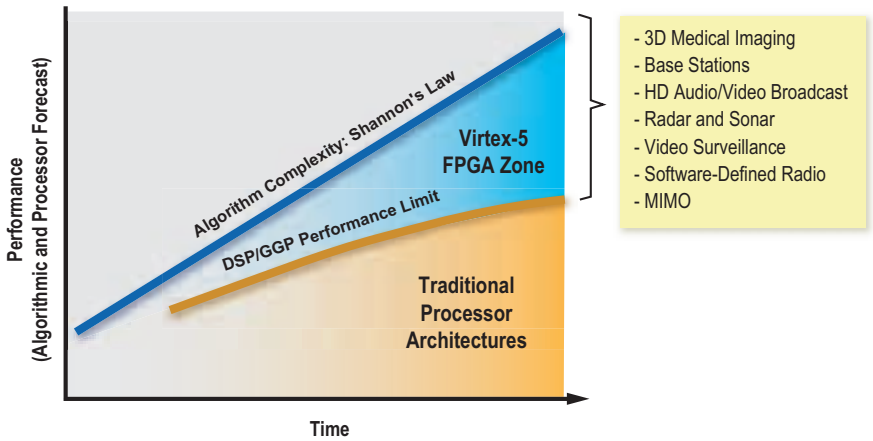

Figure 1 – Digital signal processing performance requirements over time

quency of 2 GHz with eight parallel ALUs will provide 16 GMACs (16 billion multiply accumulates per second) DSP bandwidth.

FPGAs provide user-defined control through programmable logic or a hardened embedded processor. The primary performance enabler is the variable number of DSP slices that provide the multiply add capability (see Figure 2). Bandwidth is determined by the base frequency and the number of DSP slices. The Virtex-5 SXT device runs at up to 550 MHz with as many as 640 DSP slices, providing up to 352 GMACs DSP bandwidth. The Virtex-5 SXT solution provides as much as 40x the number of DSP resources at a given frequency compared to the most advanced traditional DSP solution.

The Virtex-5 SXT High-Performance DSP Solution

The key to achieving this higher DSP bandwidth in Virtex-5 SXT FPGAs is a well-architected solution that achieves 550 MHz performance and reduces system bottlenecks through dedicated resources. The keys to implementing this complete solution are a focus on the following:

- The DSP48E utilizes a systolic implementation technique that allows each of the 640 self-contained DSP48E slices in Virtex-5 devices to operate alone or in combination, using identical interconnects that exist between each of the slices (see Figure 3).

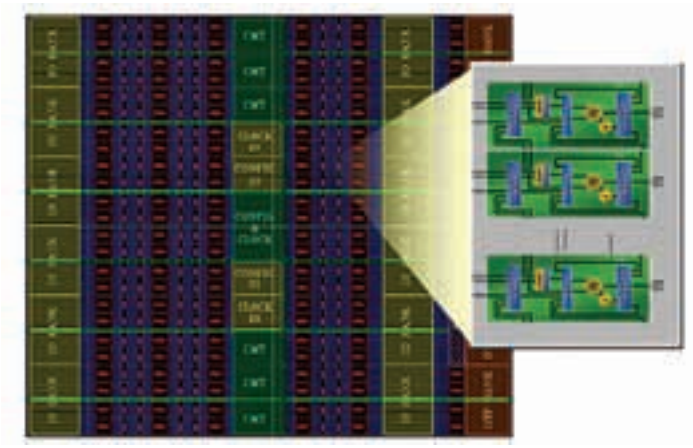

Figure 2 – Virtex-5 SX95T FPGA and DSP48E slice column

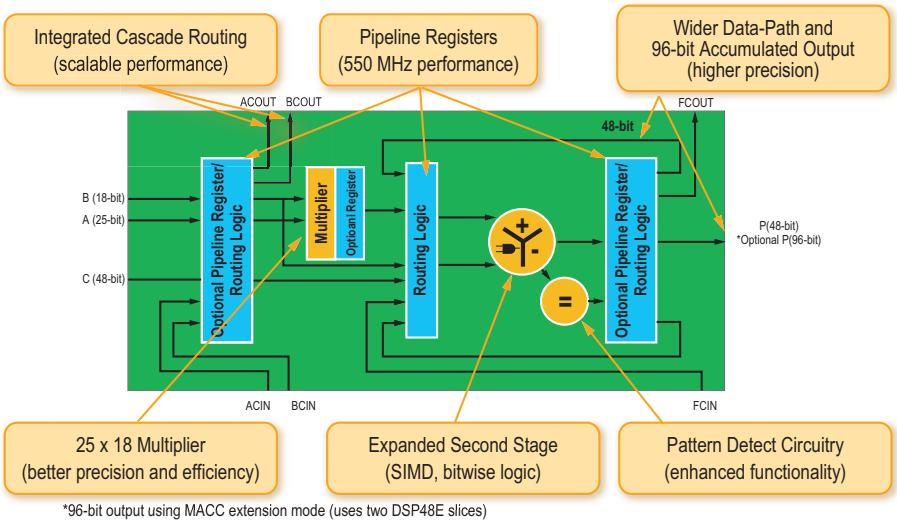

Figure 3 – Single DSP48E slice

- The DSP48E slices in Virtex-5 devices have been optimized for 65-nm process geometry and use advanced MathIP from Arithmetica to achieve maximum performance.
- The entire system – DSP48E slices, processor system, programmable logic, and memory – are all designed to work together using an external system clock operating up to 550 MHz. The system performance is tied together, controllable and sustainable.

Using the Virtex-5 SXT Solution

There are trade-offs between a traditional DSP solution and one using Virtex-5 SXT FPGAs. Traditional DSP leverages a well-established code base that runs on the sequential control logic or processor. This solution enables the reuse of existing code and provides an easy-to-use programming model.

FPGAs provide greater single-chip performance that is flexible and scalable, but requires implementation using a new set of tools or FPGA design techniques. Depending on the application, performance required, or history of the solution, one may be better than the other. Often a combination of solutions is best. To illustrate possible implementations, let's look at three different challenges, possible solutions, and the benefits of these solutions:

- **Example 1:** Legacy system utilizing a complete library of algorithms and implementation techniques that is running out of performance.
- **Plan for Example 1:** Identify DSP performance bottleneck and implement this portion of the design in a Virtex-5 SXT FPGA. Accelerate the design and achieve the required performance.
- **Benefits for Example 1:** This solution allows engineers to maintain legacy code for flexibility, ease of use, and compliance, while at the same time increasing system performance. One of the smaller Virtex-5 SXT devices may be ideal for this for co-processing, or pre-processing acceleration to a tradi-

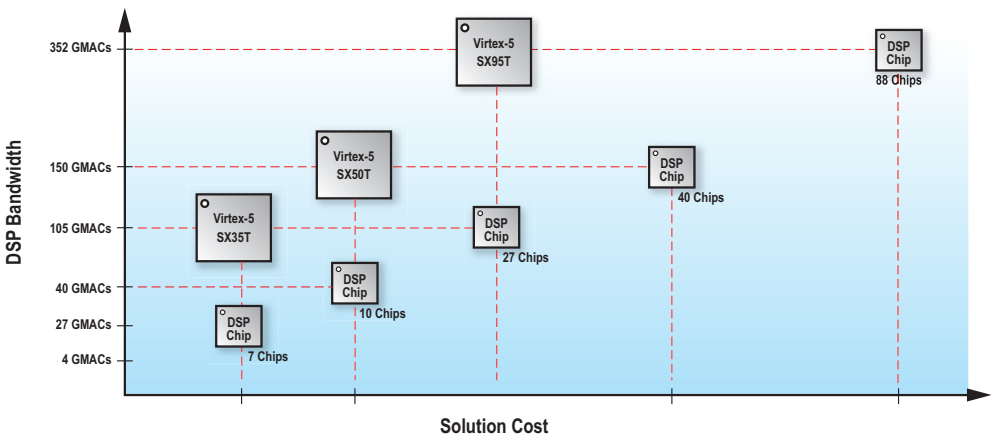

Figure 4 – Comparing performance using multiple DSP chips to a single FPGA DSP solution

tional DSP. Communication between the traditional DSP solution and the Virtex-5 SXT device is accomplished using SelectIO™ technology or using the GTP high-speed serial transceivers. Depending on the complexity of the design and algorithms implemented in the FPGA, outside technical resources may work to facilitate the implementation.

Our next example requires a significant increase in processing performance.

- **Example 2:** Performance requirements necessitate a completely new implementation to achieve much higher performance.
- **Plan for Example 2:** Re-implement the entire design into one of the larger Virtex-5 SXT devices. Use the programmable logic, I/O, and internal block RAM to implement equivalent control functionality. Use the DSP slices to implement higher speed DSP algorithms, leveraging massively parallel design techniques enabled by the systolic architecture. Overcome the new design methodology by using System Generator for DSP or the AccelDSP™ synthesis tool from Xilinx.
- **Benefits for Example 2:** Achieve orders of magnitude higher performance in a single-chip solution. Reduce board space and BOM cost compared to a traditional solution implemented using multiple DSP chips (see Figure 4).

The last example involves a redesign of a current FPGA system to achieve higher performance DSP:

- **Example 3:** Use the DSP slices available in any of the Virtex-5 FPGAs to implement high-performance DSP algorithms in addition to a standard FPGA implementation. As more DSP resources are required, move to a pin-compatible Virtex-5 FPGA platform.
- **Plan for Example 3:** Redesign an existing implementation while leveraging DSP resources, reference designs, and design techniques for Virtex-5 SXT devices.
- **Benefits for Example 3:** Higher performance and an integrated solution, which leverages the scalability and parallelism possible using DSP slices available in any of the Virtex-5 FPGA devices and platforms.

Although the DSP slices available in the Virtex-5 FPGA family enable fast and flexible digital signal processing implementations, you must take into consideration the whole solution. High-speed data plane processing requires not only high-performance DSP, but also fast input, output, and memory to store data and coefficients.

The Virtex-5 SXT device is the only FPGA that combines high-speed multi-gigabit serial transceivers for streaming data into and out of the FPGA, with a unique ratio of block RAM and distributed RAM perfect for sample data and coefficient storage. Finally, the SelectIO interface, with ChipSync™ technology, enables easy and efficient memory interfaces that simplify printed circuit board layouts. Combine this with a flexible programmable technology that enables adaptability to changing standards, and a shorter design time to meet aggressive time-to-market as well as time-in-market requirements.

For cost reduction, the Virtex-5 SXT family is available in an EasyPath™ program that allows up to a 40% cost reduction without losing the use of DSP48E slices or multi-gigabit transceivers (MGTs).

Conclusion

As digital convergence drives digital signal processing performance beyond what traditional solutions can address, explore an FPGA solution. Whether accelerating a traditional DSP solution, embarking on a new high-performance design, or rethinking your current usage of FPGAs, Xilinx has the right technology, tools, IP, and reference designs for you to succeed.

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These resources are available today and can help accelerate your design performance regardless of your use model.

- Buy the Virtex-5 SXT ML506 DSP general-purpose evaluation and development platform, which includes a variety of on-board memories and industry-standard connectivity interfaces.
- View an online demo-on-demand and learn how to accelerate FPGA designs with the AccelDSP synthesis tool and System Generator for DSP.