

Intellectual Property Offerings

Xilinx DSP Intellectual Property Offerings

The Xilinx XtremeDSP Initiative helps you develop tailored, high-performance DSP solutions.

Xilinx® DSP intellectual property (IP) offerings implement simple algorithms (filters and transforms, for example) with varying implementations that allow you to trade-off algorithmic performance for area and speed. Thus, you can achieve faster time to market by focusing on the algorithms and implementations that differentiate your designs from the competition. Xilinx DSP IP includes both free and for-purchase cores.

Table 1 lists the broad categories of Xilinx DSP IP cores.

What's New

Fast Fourier Transform (FFT)

The FFT v5.0 provides four different architectures, along with system-level fixed-point C-models, and reduces typical implementation times from three to six months to the push of a button.

FFT v5.0 expands the focus on orthogonal frequency-division multiplexing (OFDM) systems, providing reduced area for OFDM multi-channel systems like WiMAX and 3GPP-LTE through increased coverage of the multi-channel architecture and cyclic-prefix insertion.

A typical FFT used in a 2 x 2, three-second modem has 42% and 54% fewer logic resources in memory usage when comparing version 5.0 to version 4.1. This LogiCORE™ IP was released in ISE™ software 9.2i, CORE Generator software IP update 2.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=FFT



Xilinx DSP IP	
Filters	Error Correction
Transforms	Basic Math
Waveform Synthesis	Floating Point
Linear Algebra	Trigonometric Functions

Table 1 – Categories of Xilinx DSP IP cores

FIR Compiler

The FIR filter is one of the most ubiquitous and fundamental building blocks in DSP systems. Version 3.2 of the FIR Compiler expands device support to the lowest cost Spartan™-3A/3E device families. This LogiCORE IP was released in ISE software 9.2i, CORE Generator software IP update 2.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=FIR_Compiler

Cascaded Integrator Comb (CIC) Compiler

The CIC Compiler version 1.0 reduces filter implementation time to the push of a button, while also providing you with the ability to make trade-offs between differing hardware implementations of your CIC filter specification.

Along with greater than 50% area savings versus older CIC filter IP offerings from Xilinx, the version 1.0 of the CIC Compiler also comes close to the 450 MHz (-1) and 250 MHz (-4) achievable in Virtex™-5 and Spartan-3A DSP devices. This high-performance capability enables support for the highest performance ADC and DAC technology available, or alternatively supports more channels in a single structure to save area. This LogiCORE IP was released in ISE software 9.2i, CORE Generator software IP update 2.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=CIC

Xilinx Wireless Intellectual Property Offerings

Xilinx offers high-performance, cost-effective solutions for wireless networking equipment.

Xilinx wireless intellectual property (IP) offerings are suitable for RF digital front-end (DFE) signal processing, baseband processing (including forward error correction [FEC], FFTs, and adaptive modulation), and advanced interfacing, connectivity, and bridging solutions.

Xilinx Radio Reference Designs

Xilinx has developed a number of reference designs for customers supporting various air interface standards. These designs support Virtex™-4, Virtex-5, and Spartan™ DSP devices and demonstrate how to design efficiently for FPGA architectures leveraging high clock rates and specific architectural features.

Our WCDMA, WiMAX, and TD-SCDMA designs include digital up conversion (DUC), digital down conversion (DDC), automatic gain control (AGC), and crest factor reduction (CFR).

These designs are developed in System Generator, allowing you to test and verify your designs using Xilinx-supplied MATLAB scripts. They are also easily modifiable.

Using these techniques, you can quickly realize efficient digital radio implementations, resulting in lower equipment costs. For more information about the reference designs shown in Table 1, visit www.xilinx.com/esp/wireless.htm#rf.

Xilinx Baseband IP

Demonstrating our commitment to delivering optimized system-level solutions for

commercial wireless applications, ISE™ software v9.2, IP update 1, includes three new system-level LogiCORE™ IP products for 3GPP release 6.

3GPP Downlink Chip Rate

The 3GPP Downlink Chip Rate LogiCORE solution provides a release 6-compliant, Xilinx FPGA-optimized solution for femtocell, picocell, and macrocell solutions. The architecture has been designed to provide efficient use of FPGA logic, while offering a low-bandwidth interface to an external DSP or microprocessor and reducing system-level overhead using a built-in OCP interface.

The FPGA performs timing-critical operations, which simplifies the software impact with traditional DSP solutions, allowing for an optimum software/hardware balance. The core is fully optimized for speed and area while supporting all frequency division duplex (FDD) channels. This LogiCORE IP was released in ISE software 9.2i, CORE Generator software IP update 1.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=DO-DI-DLCR-3GPP

3GPP RACH Preamble Detector

The 3GPP RACH preamble detector is used in WCDMA transmission systems. This LogiCORE IP allows you to scale the solution from femtocell up to macrocell architectures. The LogiCORE IP is also highly cost-effective, with minimal utilization by using streamed correlation calculations and supporting coherent and non-coherent detection methods.

Scalability is maximized through customizable inputs such as search window size, coherent accumulation window size, number of antenna, hardware over sample rate, and I/O quantization. It also offers ease of integration with a suitable DSP or microprocessor through Open Core Protocol (OCP) interfaces. This LogiCORE IP was released in ISE software 9.2i, CORE Generator software IP update 1.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=DO-DI-RACH-3GPP

3GPP Searcher

The 3GPP Searcher is used in WCDMA transmission systems to identify the multiple user transmission paths in a 3GPP uplink. This LogiCORE IP offers a compact and scalable solution when used for either picocell/femtocell or macrocell applications, resulting in the lowest cost for the given target application.

The core includes all of the logic required for scramble code generation, correlation, accumulation, and filtering functions in a single co-processing solution, easily integrated with either a DSP or microprocessor using available OCP interfaces. The CORE Generator software GUI allows you to fully customize to your own needs. This LogiCORE IP was released in ISE software 9.2i, CORE Generator software IP update 1.

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=DO-DI-SEARCHER-3GPP

Conclusion

To access the IP solutions highlighted in this article, visit www.xilinx.com/ipcenter.

Topic	Resource	Type	Provider
WCDMA/HSPA	WCDMA/HSPA Reference Design (Login Required) Device Architecture: Virtex-4, Virtex-5 FPGAs DUC: Three Carrier DDC: Six Carrier (Receiver Diversity) CFR: Three Carrier (PAPR<6 dB@<11% EVM, >60 dB ACLR)	Reference Design	Xilinx
WiMAX	WiMAX Reference Design (Login Required) Device Architecture: Virtex-4, Virtex-5 FPGAs DUC: One carrier (dynamic switching 3.5, 5, 7, and 10 MHz) DDC: One carrier (dynamic switching 3.5, 5, 7, and 10 MHz) CFR: One carrier (PAPR>1.5 dB@2% EVM) WiMAX Reference Design (Login Required) Device Architecture: Spartan-3A DSP FPGA DUC: One carrier (Dynamic Switching 5 and 10 MHz) DDC: One carrier (Dynamic Switching 5 and 10 MHz)	Reference Design	Xilinx
TD-SCDMA	TD-SCDMA Reference Design (Login Required) Device Architecture: Virtex-4 FPGA DUC: Up to Six Carrier DDC: Up to Six Carrier	Reference Design	Xilinx
Common Digital Radio System (CDRSX)	Common Digital Radio System Development Platform Device Architecture: Virtex-II Pro, Virtex-4 FPGAs	Development Board	Axis Networking

Table 1 – Xilinx radio reference designs