

# Implementing Industrial Ethernet

You can implement a Powerlink real-time communication protocol with support from protocol-optimized Ethernet MAC controllers.

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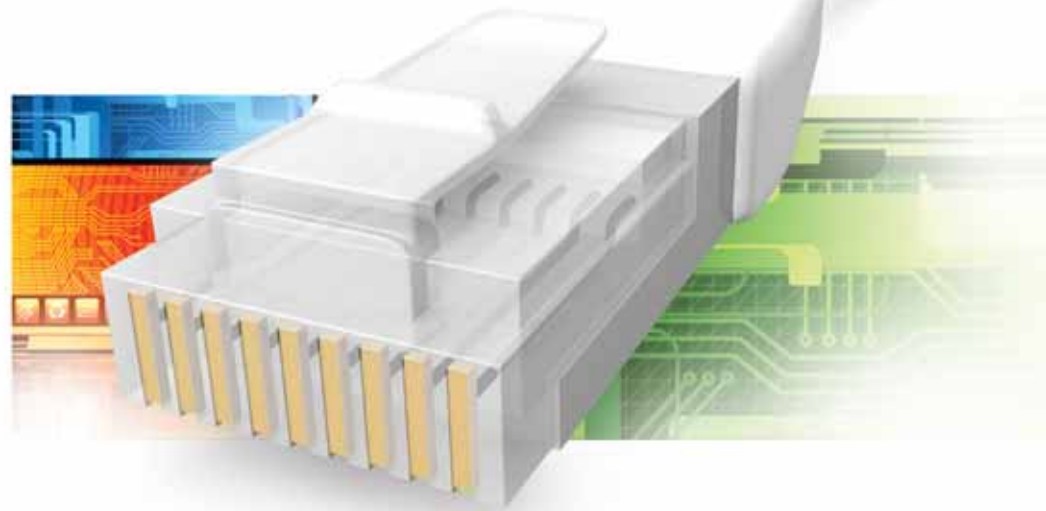
In the last decade, industrial communication in machine building was the domain of field buses like DeviceNet, CANopen, and Profinet. Although sufficient in most cases, in high-end application determinism and high bandwidth are required.

For some years now talk has centered around an Ethernet-based network to fill this gap. One of these networks is Ethernet Powerlink, introduced in 2001 by the Austrian company B&R. Powerlink is a very flexible real-time communication protocol. Its main advantage is that devices, controlled nodes (CN, or slaves), and managing nodes (MN, or master) can be built using standard Ethernet components for 100-Mbps Ethernet-like PHY, Ethernet MAC controllers (EMACs), cables, and other infrastructure components.

Nevertheless, for reaching best real-time behavior, short delays, and short response times, it is desirable to have hardware support in the EMAC. A second requirement for CNs is that they should have a built-in hub in order to connect devices in a line network structure like in conventional field buses.

FPGAs can fulfill both requirements.

Like Ethernet/IP, Modbus TCP, and Profinet, Powerlink's open, software-based, real-time communication system runs on standard Ethernet hardware, rendering special hardware components unnecessary. Component manufacturers therefore do not need to develop proprietary ASICs and run time-consuming tests. You can produce encoders, for example, featuring the same hardware and appropriate software. Software



implementations and new developments are therefore easy to realize, which means that second-source availability for Powerlink is better than for proprietary systems.

Moreover, Powerlink's open structure allows for a flexible use of hardware components: if machine and plant engineers need to integrate a device operated under a different network protocol into a Powerlink application, another standard controller and additional field bus trunk are all it takes. Standard diagnostic and measurement systems like cable testers and network analyzers can often be used for service and maintenance tasks on Powerlink networks, considerably reducing operating costs.

FPGA designs for industrial real-time communication are not just restricted to standard Ethernet. Designs for EtherCAT, which uses standard Ethernet frames but cannot use standard Ethernet MAC controllers on network slaves, can be implemented using FPGAs. And although protocols like Ethernet/IP and Modbus TCP can use Xilinx® standard tri-mode Ethernet MACs, Powerlink designs gain a lot of additional performance with specialized MAC controllers.

Implementing Powerlink to achieve true 100-Mbps speed requires more than simply choosing the right medium and infrastructure components. Much of the Powerlink throughput depends on the endpoints. Increasingly more expensive and higher performance systems are required to keep pace with network throughput. Powerful optimized FPGA solutions are the way to go.

Let's discuss some implementation variants for Powerlink with different functionality and complexity.

## Powerlink Implementation Variations

Ethernet Powerlink distinguishes between real-time domains and non-real-time domains. This separation matches typical machine and plant concepts. It also satisfies increasing security demands to prevent harm through erroneous data communication on higher network hierarchies. Hard real-time requirements are met within the real-time domain. Data that is less time-critical is routed transparently between the real-time domain and the non-real-time domain using standard IP frames.

The current physical level is 100Base-X Fast Ethernet (IEEE 802.3). All network

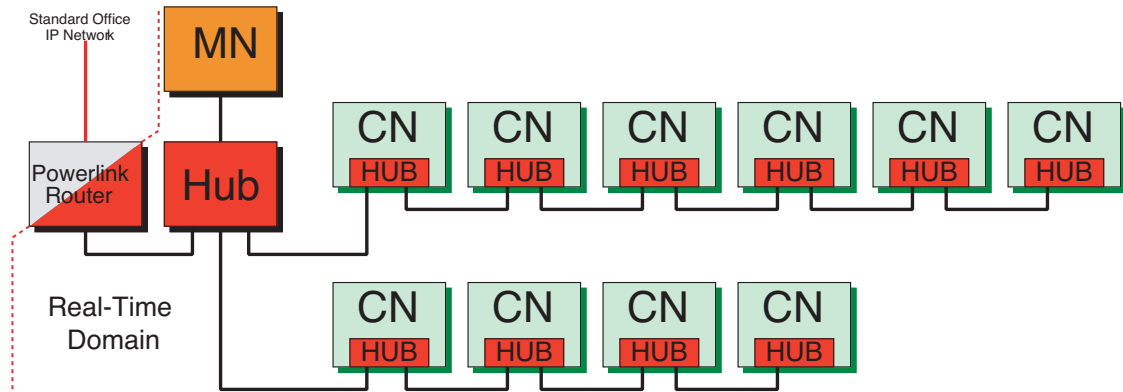


Figure 1 – Typical network topology and the need for integrated hubs

topologies are possible. To create a topology, we recommended using repeating hubs instead of switches within the real-time domain to minimize delay and jitter. Figure 1 shows a typical network topology and the need for integrated hubs.

### Powerlink Ethernet Hub

The simplest FPGA design that you can use in Powerlink devices is an Ethernet hub. The typical Ethernet infrastructure is a star topology, but industrial networks often require a line topology. This can be achieved by implementing an Ethernet hub in each of the Powerlink nodes. Figure 2 shows a controlled node using an FPGA-implemented hub.

For speed reasons, the Powerlink standard requires a low signal delay in hubs – less than 500 ns. This only can be reached by connecting the PHY through a MII interface.

All other components on the Powerlink device are standard network components or standard microcontrollers. Instead of a microcontroller with integrated EMAC, a stand-alone Ethernet MAC controller can be used together with any standard microcontroller running the Powerlink stack and device application firmware.

### Powerlink Ethernet MAC

The next step implements the most important piece of VHDL code for effective Powerlink protocol handling: a specialized Ethernet MAC controller optimized for Ethernet Powerlink for Xilinx FPGAs. Through several special transmit buffers and the option to respond automatically to Powerlink request frames by hardware, you

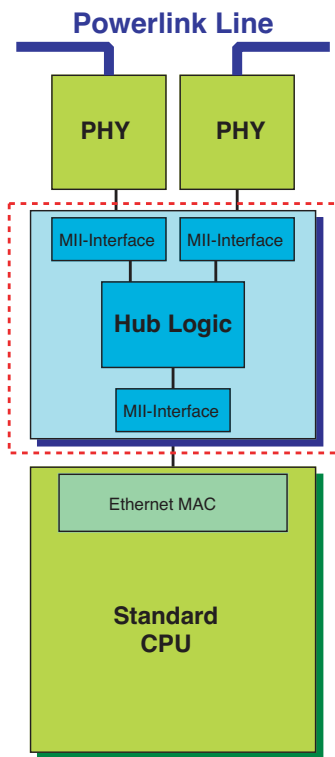


Figure 2 – FPGA-based hub

can achieve extremely short response times. Special receive filters allow pre-filtering of Powerlink messages by the MAC controller, releasing the software from this task.

These filters support the pre-selection of Ethernet frames that are needed by the processing software. Based on the used settings, only those frames that match the filters are stored in the receive buffers. This mechanism releases the CPU from processing frames not relevant for the software.

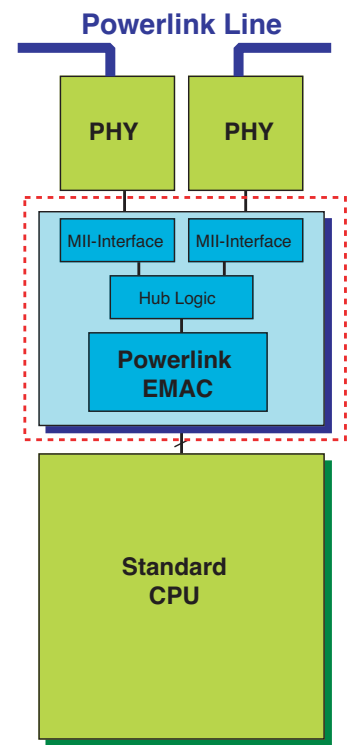


Figure 3 – FPGA-based EMAC

The Powerlink MAC – which we refer to as PE<sup>2</sup>MAC – is a stand-alone component linked to the processor through registers (control and status information), a dual-port memory (data buffer), and an interrupt request signal. The processor interface is 32 bits wide. Furthermore, a separated signal is provided that signals an incoming SOC packet. If this interface is provided at the FPGA pins, even a small FPGA can be used purely as a Powerlink MAC controller in

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connection with any standard microcontroller. A special Powerlink-MAC driver provides an optimal interconnection to the Powerlink protocol library offered by our company, port, written in C.

Figure 3 shows a design with an FPGA-based EMAC and standard CPU.

### Powerlink All-In-One Solution

In larger FPGAs, it is possible to extend the design to an all-in-one solution. Not only is the hub and PE<sup>2</sup>MAC implemented, but so is the CPU as a soft core for higher layer protocol and application handling. Figure 4 shows this FPGA-based Powerlink all-in-one solution for a controlled node.

The CPU IP core is driven by C programs. A special Powerlink MAC driver provides an optimal interconnection to port's Powerlink protocol library. The Powerlink protocol library provides all required services for a compliant communication according to communication profile V2.0.

The Powerlink protocol library is completely written in ANSI-C and can be compiled with every ANSI-C-compliant compiler. One possible combination is the Xilinx MicroBlaze™ embedded processor and GNU gcc compiler. In connection

with the Powerlink hub, a straightforward connection to a Powerlink network is provided. Additionally, a sophisticated solution with technical parameters (short response times, fast reaction to network events) that conforms to the requirements of the Powerlink standard is available.

The CPU has to handle the software part of the Powerlink protocol and the application software. Note that in such single CPU solutions the Powerlink protocol should have priority to guarantee good network performance. The Powerlink MAC is responsible for fast responses, but has to be fed with new data if network cycles are short.

### Powerlink Communication Coprocessor

If the application itself is very time-critical and demands response times in the lower microsecond range (like control loops of motion controllers), then you must choose a

real-time communication coprocessor. The design has the communication and application processor coupled by a dual-ported RAM interface. Both controllers can handle their time-critical domains, which results in fast response times in both domains. Figure 5 illustrates a design with an FPGA-based communication coprocessor.

Putting the communication coprocessor in the FPGA has many benefits. The FPGA can hold the hub (required in many protocols), the MAC controller for the respective protocol, a general processor for handling the protocol-specific data link layer, and the dual-port (DP)-RAM.


This way, the communication coprocessor can be used for Powerlink, EtherCAT, Modbus TCP, and Ethernet/IP, including CIP-SYNC and even Profinet RT.

### Conclusion

FPGAs are well suited to implement powerful communication interfaces for industrial control applications, not only – but especially – for Ethernet Powerlink.

In the future, Ethernet Powerlink with Gigabit Ethernet (IEEE 802.3ab) will support a transmission rate 10 times higher (1,000 Mbps) than today. That offers a real perspective for the future to extended systems with major production performance, a series of module control systems, numerous drives, and completely integrated security equipment. This technology is portable to FPGAs too.

To achieve true 100-Mb performance, systems must be designed and configured to support 100 Mb throughout the network. This includes improving Powerlink protocol processing through hardware assistance so that the CPU has more cycles for application processing (to make sure that associated software is written effectively) and having chipsets with memory subsystems that will not limit system performance.

For more information, visit [www.epl-tools.com](http://www.epl-tools.com) to request more information about the POWERLINK-enhanced Ethernet MAC controller, PE<sup>2</sup>MAC. 

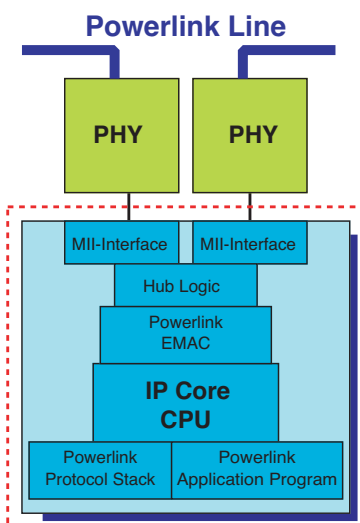


Figure 4 – FPGA-based Powerlink all-in-one solution

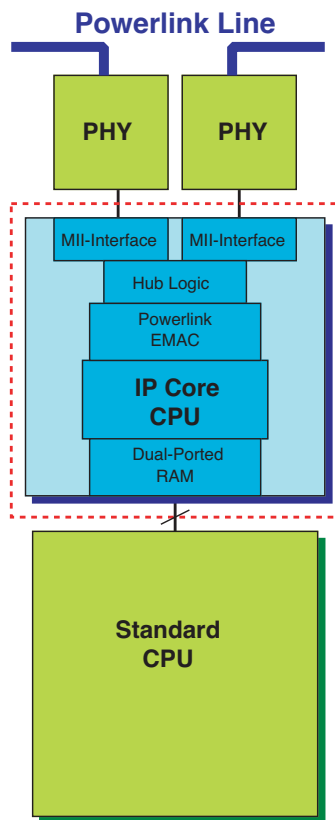


Figure 5 – FPGA-based Powerlink communication coprocessor