



Designing GPS Systems Using CoolRunner-II CPLDs

Expanding functionality using low-power CoolRunner-II CPLDs.

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Asking for directions is becoming a foreign concept. It's fast dying out, much like the art of folding a map or a newspaper. Its impending extinction can be attributed to the increasing popularity of the Global Positioning System (GPS).

GPS is present in a growing number of products: automobiles, cell phones, personal data assistants, even wristwatches. With each GPS vendor showcasing a product line of several dozen GPS products, consumers are overwhelmed with the selection.

Therefore, success lies in product differentiation and specialization. Xilinx® CoolRunner™-II CPLDs are the ideal chips to add features or interface with another device to make your GPS product stand out from the rest – without breaking the power budget.

The Power Advantage

Both portable and in-dash GPS devices must adhere to a strict power budget. CoolRunner-II CPLDs have the advantage of minimal power consumption without the need for sleep mode states. The smallest CoolRunner-II device has a quiescent power of 13 μ A. In some portable applications, a sleep mode is sufficient and a wake-up time in the hundreds of milliseconds is acceptable.

In some cases, however, the current design states are lost. When using sleep mode, your entire device shuts down. You must rely on a secondary device to poll for interrupts and initiate a wake-up sequence. CoolRunner-II devices offer a unique sleep mode without the associated design headaches through its DataGATE feature, a self-contained and user-configurable circuit that allows you to disable as much of the device as you desire.

By enabling DataGATE, you can turn off whichever inputs you choose in several nanoseconds, thereby shifting the power consumed by the CPLD closer to a quiescent state. This could be done periodically, such as when polling for an interrupt, or it could be dependant on a



particular state of operation. Thus, portions of the CoolRunner-II device can remain active while others are in standby.

Let's look at an example to explain further. The CPLD sits on an address and data bus between a microprocessor, mobile SDRAM, and SD flash card. Data moves between each of the devices. The CPLD monitors the data activity and blocks traffic based on the particular function. If the current task is to move data from the microprocessor to the SD card, then the CPLD blocks any data to and from the SDRAM using DataGATE.

Within the CPLD, you can write code to simply decode the function being performed (either from watching the address lines or by parsing frame data) and then enable/disable whichever data path is required. This is a trivial example that is possible to a much lesser degree with other programmable logic devices (PLDs) by using output 3-states.

The advantage of DataGATE is that it effectively 3-states at the input of the CPLD. Power savings increase because the CPLD I/O as well as core circuitry are placed in a quiescent state, whereas alternate solutions require the entire PLD to stay in active mode.

The Security Advantage

GPS system pricing makes it an attractive target for product cloning. To help prevent this, you can utilize CoolRunner-II CPLD's read/write protect security to implement a security system that prevents cloning by overbuilding. Overbuilding occurs when a contract manufacturer orders extra components for a given production run and then builds extra products that are identical to the authentic versions.

The concept is that the system requires interaction with the CPLD to perform any desired function. You can implement this security in any number of ways. The most straightforward solution would be to have a CPLD act as a data-traffic cop, directing data between the individual devices on the board.

A more complex solution involves using the CPLD to implement a block cipher. This would have the microprocessor submit a random stream of data to be encrypt-

ed by the CoolRunner-II device and returned. This data would then be decrypted and verified against the original data.

The CoolRunner-II CPLD's security is implemented through multiple programming bits, so someone attempting to determine which bits are relevant for security must find and disable several bits out of tens of thousands in the non-volatile array. The security in CoolRunner-II CPLD read/write security prevents readback and programming on top of the existing pattern. So the device

blank CPLDs is not useful without access to the programming file.

Achieving Product Differentiation in GPS Units

Original consumer GPS units were straightforward. They simply gave location information in the form of latitude and longitude. Today's GPS units not only offer real-time maps and directions, they offer MP3 playback or integration with cell phones via Bluetooth. There are also market-specific GPS systems with features such as traffic updates for in-car navigation,

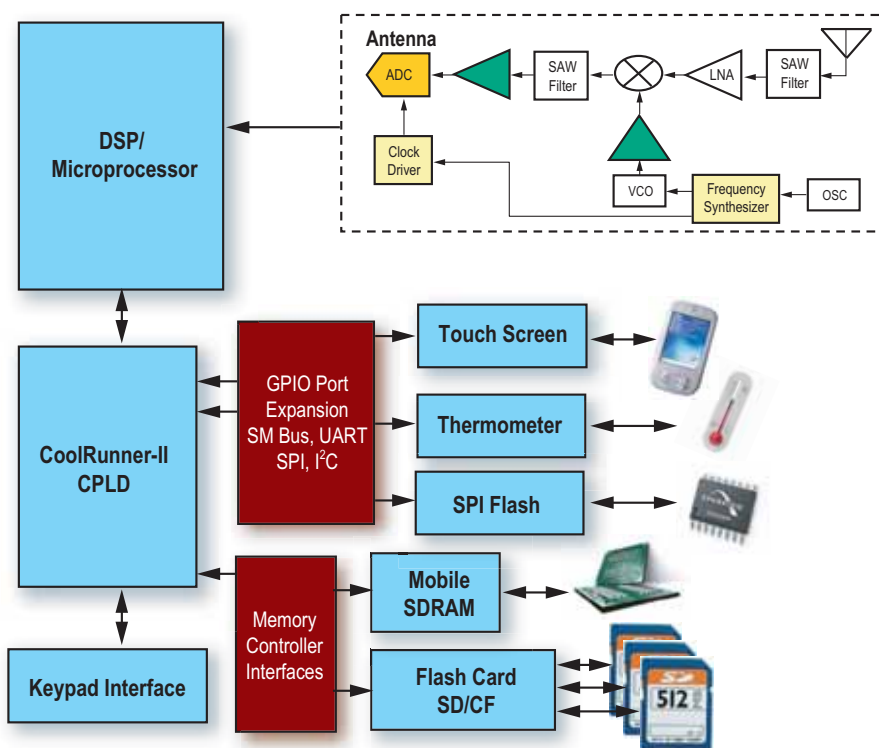


Figure 1 – GPS block diagram

will not permit extraction of the programmed JEDEC file, nor will it allow someone to overlay a modified version of the code on top of an existing pattern. To reprogram the device, the entire device must first be erased, in which case the design information is lost.

A critical factor in any of these flows is that pre-programmed CPLDs must be provided to the contract manufacturer from a trusted source (Xilinx or an authorized Xilinx distributor). This prevents overbuilding – because simply ordering more

ultra-small units for runners or cyclists to measure their pace, units with sonar for fishermen – even GPS-enabled collars for keeping tabs on the family pet.

Each product requires an interface to something different – and that's where the CoolRunner-II CPLD is a perfect fit. The following topics demonstrate some uses for CoolRunner-II CPLDs. I've also listed associated Xilinx application notes at the end of this article. Figure 1 demonstrates functions where Xilinx CPLDs can benefit a GPS application.



Xilinx CoolRunner-II CPLDs demonstrate their usefulness in lowering power, increasing security, and providing connectivity solutions for today's GPS systems. With our portfolio of small form-factor packages, these devices can fit into the smallest portable packages such as cell phones, dog collars, and wristwatches.

SD Card Interface

SD memory (in its various physical formats such as mini-SD and micro-SD) has separated from the pack of memory interfaces that competed a few years back. Although other interfaces such as MMC and Compact Flash are still around, they represent only a small percentage of the market. Flash cards are essential for any product with picture or MP3 playback; both features are becoming more prevalent in GPS handheld units.

Mobile SDRAM Interface

You can simplify microprocessor code by allowing the CPLD to act as the memory interface. If your high-end model requires multiple memory modules but your low-end product does not, let the CPLD code change, not your microprocessor.

Level Translation

As GPS moves into newer consumer areas, they connect to components that are not yet optimized for low-voltage operation. CoolRunner-II CPLDs have a minimum of two I/O banks (increasing to four I/O banks in the largest device), allowing multi-voltage interfaces to be addressed easily. Supported voltage standards include 1.5 V, 1.8 V, 2.5 V, 3.3 V, SSTL 2-1, SSTL 3-1, and HSTL-1. 5-V interfaces are supported with some external circuitry.

Keypad Scanner

Many of the lower end GPS models cannot use a touch-screen interface because of cost constraints or size limitations. Even in the expensive models, a few buttons are designated for certain features such as power or volume control. Some form of keypad or button interface is used in most models. This is an ideal use for CoolRunner-II CPLDs because when there is inaction from users, the CPLD remains in a quies-

cent state and can immediately respond to a user key press without having to wake up from sleep mode. Furthermore, it can be designed to verify user data before waking up the rest of the system.

For example, many cell phones require that you press two keys in sequence before waking up to ensure that the buttons weren't accidentally pressed.

Microprocessor Interface

A common role for CoolRunner-II CPLDs is port expansion. Many microprocessors simply lack sufficient I/O for the multitude of devices with which they must communicate. CoolRunner-II CPLDs allow a product platform design to add and change modules without changing the core processor.

Serial Peripheral Interface (SPI)

SPI is a common interface used by many peripherals, including flash storage chips, LCDs, touch screens, and temperature sensors. Its popularity can be attributed to a simple four-wire interface and improved throughput over I²C or SMBus.

Conclusion

Xilinx CoolRunner-II CPLDs demonstrate their usefulness in lowering power, increasing security, and providing connectivity solutions for today's GPS systems. With our portfolio of small form-factor packages, these devices can fit into the smallest portable packages such as cell phones, dog collars, and wristwatches. Personally, I can't wait until they embed a GPS into car keys. ●●●

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- Start evaluating CoolRunner-II CPLDs for your GPS application and purchase the CoolRunner-II Design Kit.
- Learn more from these Xilinx application notes:
 - XAPP347, "Decreasing Processor Power Consumption using a CoolRunner-II CPLD"
 - XAPP395, "Using DataGATE in CoolRunner-II CPLDs"
 - XAPP906, "Interfacing with Multiple SD Devices with CoolRunner-II CPLDs"
 - XAPP398, "CompactFlash Card Interface for CoolRunner-II CPLDs"
 - XAPP394, "Interfacing to Mobile SDRAM with CoolRunner-II CPLDs"
 - XAPP785, "Level Translation Using Xilinx CPLDs"
 - XAPP512, "Implementing Keypad Scanners with CoolRunner-II"
 - XAPP799, "An SMBus/I²C Compatible Port Expander"
 - XAPP341, "UARTs in Xilinx CPLDs"
 - XAPP386, "CoolRunner-II Serial Peripheral Master"