

# Implementing Next-Generation Wireless Standards Using Virtex-5 FXT Device Parts

The Xilinx LTE baseband reference design shows how the Virtex-5 FXT device enables hardware, software, and high-speed off-chip comms for wireless baseband processing — implemented on a single device.

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The next generation of the 3GPP wireless standard is called long-term evolution (LTE). It provides a leap in performance and a complete move to packet-based processing. In the physical (PHY) level of the LTE specification, specific challenges exist when dealing with higher data throughput rates, as well as the move to OFDM (orthogonal frequency-division multiplexing) for transmission.

Xilinx has developed — or is in the process of developing — several new or revised DSP LogiCORE™ solutions to meet the demands of the new specification. With such blocks it is critical not only to verify them as stand-alone blocks, but also to validate them in real systems with real-world data. The Xilinx 3GPP downlink reference design provides this validation, as well as providing a reference to customers about how to use the blocks.

The higher data rate in LTE places increased processing demands on all parts of the system: increased DSP hardware processing in the baseband, increased software processing to implement the higher layers of the UMTS protocol stack, and increased I/O communication bandwidth to accept packets and pass data to remote heads.

In this article, I'll review some of the new features of the LTE specification and how Xilinx® Virtex™-5 FXT devices address the increased processing demands of LTE through its tight integration of microprocessor subsystem, DSP-enhanced FPGA fabric, and high-speed communication links.

### The 3GPP LTE Physical Layer

One of the key changes in the Layer 1 (PHY layer) of the 3GPP LTE is the change from CDMA (code-division multiple access) to OFDM (orthogonal frequency-division multiplexing). One of the main benefits of OFDM is that it reduces the problems associated with multiple paths in the radio channel. In CDMA, a significant amount of processing must be devoted to characterizing and tracking the radio channel to compensate for the effects of fading in the channel.

Figure 1 illustrates the structure of an example LTE subframe. The subframe comprises a number of OFDM symbols. Each OFDM symbol provides the data input for an inverse fast Fourier transform (IFFT). In LTE this may be as many as 2,048 input points for in-phase (I) and quadrature (Q) components.

A subframe can be represented as a resource grid, where each resource element in the grid comprises a single I/Q input point for the IFFT in an OFDM symbol. Resource grids can be layered to provide data to multiple antennas, supporting transmission schemes such as transmit diversity or MIMO (multiple input/multiple output) techniques.

The resource grid is allocated to different purposes. Resource elements are allocated to control channels, data channels, and synchronization signals. The diagram also shows the packetization of data on the channel – different areas of the resource

grid are allocated to different users' data as resource blocks. The task of scheduling data transmission and allocating resource blocks to users is performed by the higher software layers in the LTE stack.

### 3GPP LTE Downlink Processing

Figure 2 shows the processing stages in the baseband section of the 3GPP LTE downlink. The processing for both transmit and receive can be split into two main sec-

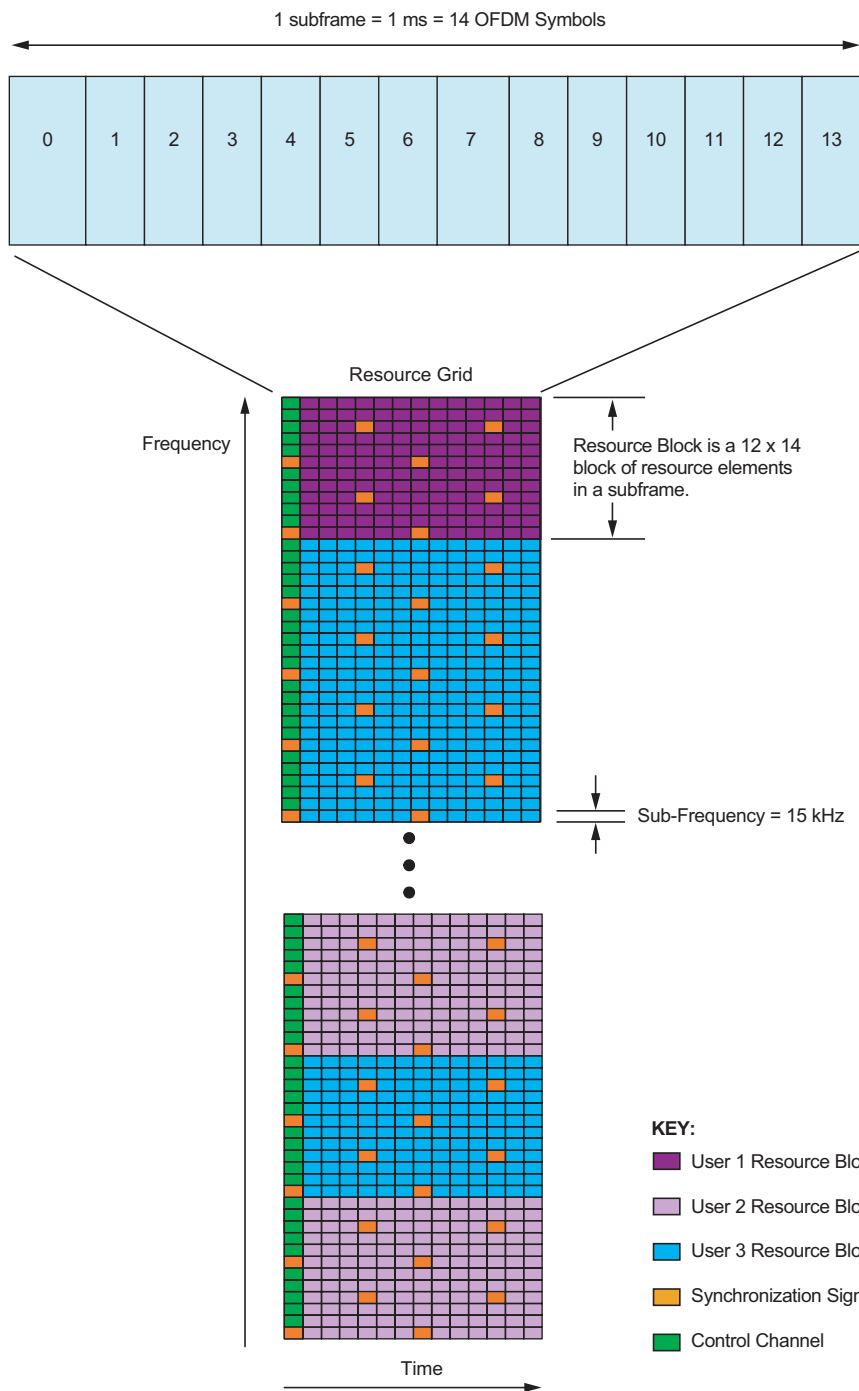


Figure 1 – LTE uses OFDM. A subframe comprises a resource grid, with areas allocated to control, synchronization, and user data. Each column of the grid forms an OFDM symbol that is converted to the time domain by an IFFT.

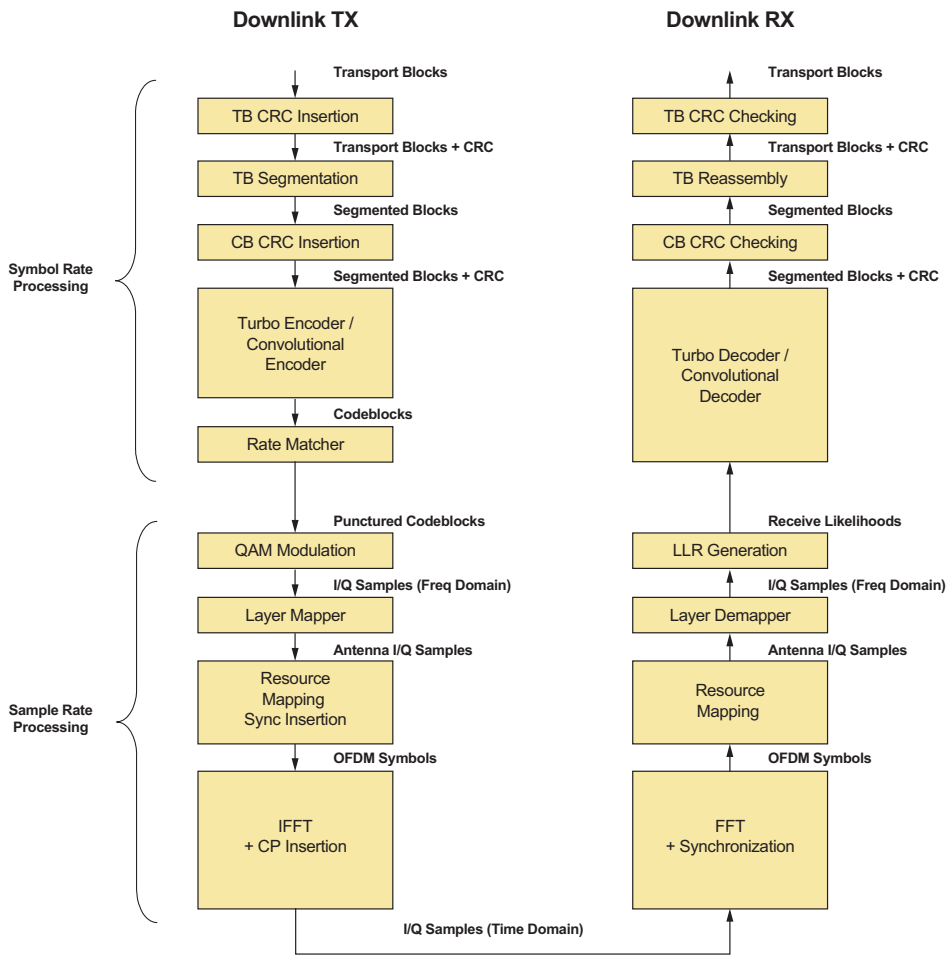


Figure 2 – 3GPP LTE downlink processing: transmit and receive chains

tions: symbol rate processing and sample rate processing.

Symbol-rate processing is centered around forward error correction, used to add redundancy to the data stream in a bandwidth-efficient manner and to recover data on the receiver. Sample-rate processing is centered around the IFFT/FFT that performs the OFDM part of the baseband operation.

**Transmit Symbol Rate Processing**

The first stage in the Layer 1 (PHY) processing of the LTE downlink takes transport blocks from the media access controller (MAC) layer. Transport blocks have cyclic redundancy checks (CRCs) added, while larger transport blocks may be segmented to ensure that blocks do not exceed a maximum size supported by the forward-error encoder.

Each segment then has a CRC added before it is supplied to the forward-error encoder: for data channels this is a turbo encoder and for control channels this is a convolutional encoder. Following the encoding, rate matching is applied to the output to puncture the data so that it will fill the available resource blocks in the OFDM resource grid. Finally, the data stream is modulated with a specified modulation (QPSK, QAM16, or QAM64) to give a sample value to go in the OFDM resource grid.

**Transmit Sample Rate Processing**

Samples are first mapped to different antenna layers. This mapping allows support for schemes such as transmit diversity (multiple transmit paths to reduce noise at receiver) or MIMO (MIMO techniques utilize multiple channels

between transmitter and receiver to increase data rates).

The next step is to map samples to resource elements in the OFDM resource grid. This stage also adds synchronization signals to the resource grid, allowing the receiver to synchronize with the transmitter. The output of this stage is passed to an IFFT. The IFFT takes the samples from the frequency domain to IQ signals in the time domain, which are ready to be sent to the radio-head for transmission. OFDM requires a cyclic prefix (CP) added to the data, which repeats the end of the time-domain signal at the start of the output. The CP size is determined by the size of the mobile cell and reflections. A sufficiently larger CP is required to remove multi-path effects from the OFDM symbol.

**Receive Sample Rate Processing**

The receive processing generally follows the inverse of the transmit processing. The first step is to do an FFT on the incoming data to convert the time-domain signal back to the frequency domain. In the reference design, data is received across all OFDM sub-frequencies for all users, but a real mobile user would only decode data on the resource blocks that it had been allocated. Synchronization at this step is also performed to synchronize the system to the start of each sub-frame in the OFDM data. The output of the FFT is processed through a layer demapper that inverts the layer mapping in the transmission.

**Receive Symbol Rate Processing**

The first step in the receive processing is to take modulation symbols and convert them to individual bits. For turbo-encoded data, this is a set of probabilities in the form of logarithmic-likelihood-ratios for the turbo decoder. For convolutionally encoded data, it is a distance metric that is then fed to a Viterbi decoder. The output of the error correction is checked for CRC validity and reassembled into the original transport blocks.

**The LTE Baseband Reference Design**

LTE has required a number of new or revised Xilinx LogiCORE solutions to meet

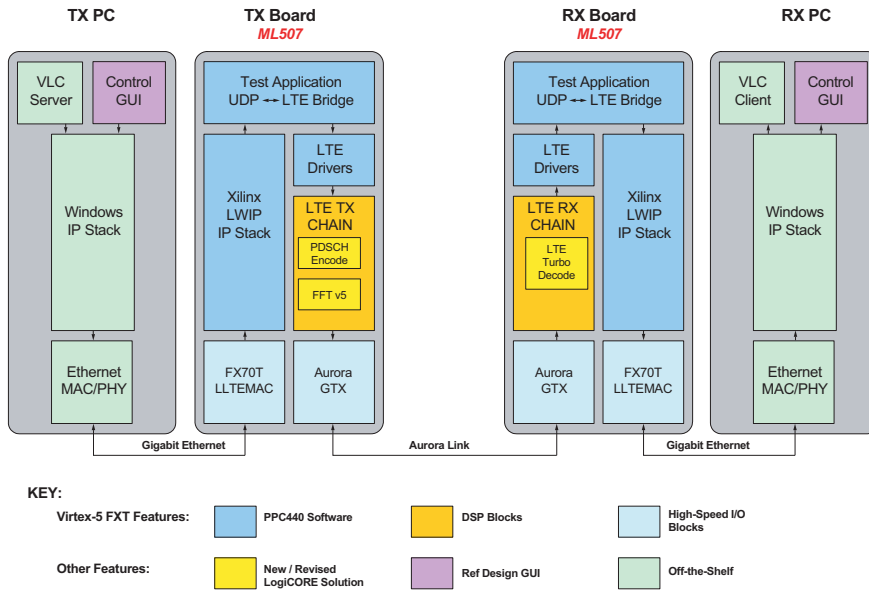


Figure 3 – Xilinx LTE baseband reference design showing system integration of hardware and software blocks. Blocks are stacked into respective protocols so that higher layers use services of lower-layer blocks. Peer-to-peer communication goes from left to right.

the new requirements of the specification. For example, the turbo encoder uses LTE-specific interleavers; the IFFT requires the addition of a variable-length cyclic prefix; and the turbo decoder requires a far higher throughput than previous 3GPP standards.

Verifying these individual blocks presents a number of challenges. First, the LTE standard is still changing and has not been ratified. Second, the size of OFDM symbol (potentially 2,048 points) and the length of the sub-frame and turbo-decoder iterations required mean that a large number of simulation cycles are required to verify the behavior of even a single transport block being decoded. This can limit the test coverage achievable in simulation. Finally, just running unit tests on blocks does not test the macroscopic behavior of systems such as transport-block error rates, or validate that blocks have compatible interfaces.

To address these issues, the design team decided to implement an LTE reference system design that would provide system-level validation of the new LTE LogiCORE IP using real-world data sources such as video streams.

Since the main aim of the reference system was to validate new IP LogiCORE solutions, we wanted to minimize the

amount of additional design work for the reference design. We also wanted to minimize the system integration and tool issues and use off-the-shelf boards and IP blocks as much as possible.

Previous reference systems for WCDMA Release 6 of the 3GPP specifications had used a separate DSP microprocessor board coupled with an FPGA board. This meant using different tool flows for software and hardware design, plus the overhead of designing interposer boards to connect the main boards together.

For the LTE baseband reference design, we chose to avoid these issues by gaining early access to the Xilinx Virtex-5 FXT device silicon. The FXT parts integrate on a single chip a PowerPC 440 microprocessor, DSP-enhanced FPGA fabric, and high-speed GTX off-chip communication blocks. This decision minimized our system integration problems (as all the key components were on a single chip) and allowed us to use the standard customer design board, the ML507.

In addition, the design simplified our tool flow. The top level of the system was integrated in Xilinx Platform Studio (XPS), which allows a large number of pre-verified blocks to be pulled into the system from the Xilinx Embedded Development Kit

(EDK). XPS was the framework to pull in the various LogiCORE systems that needed validating, plus additional blocks that were implemented in a mixture of VHDL and Xilinx System Generator for the DSP portions of the design.

### Implementing on the Virtex-5 FXT FPGA

Figure 3 shows a top-level block diagram of the LTE baseband reference design. The system shown consists of two ML507s, which act as IP packet bridges between the Gigabit Ethernet and LTE protocol stacks.

The reference application is video streaming using the open-source VideoLAN Server. The VideoLAN server runs on the transmitter PC, which communicates to the system over the Gigabit Ethernet link. Video is received by the VideoLAN client on the receive PC. A control GUI also runs on the PC, allowing you to set up the LTE blocks to be changed and monitored remotely.

Video packets are transmitted through the LTE software driver and into the LTE downlink transmission blocks previously described. The output I/Q data from the LTE downlink is then sent out over an Aurora link. Aurora was chosen initially over dedicated base station standards such as CPRI/OBSAI protocols because of its early availability on FXT parts.

The I/Q data is received on the receive ML507 board and passed into the LTE downlink receive chain. Processing and communication follows an inverse order to that for the transmission, and finally delivers video packets to the VideoLAN client on the receiving PC.

Figure 3 is color-coded to highlight how the different features of the FXT parts are used. The software elements of the system that run on the PowerPC 440 are highlighted in dark blue. DSP functions comprising the LTE downlink transmit and receive processing are in orange and high-speed I/O blocks are in light blue. New or revised LogiCORE solutions are shown in yellow.

We found we could implement both transmit and receive functionality on a single FX70T part, so by looping back the data on the Aurora link, we could implement the system on a single ML507.



Figure 4 – Screenshot of demo running. The GUI allows variable modulation, encoding rate, and channel noise. Transmitted video is in the upper right-hand corner. Received video (with time lag for software video decode buffers) is shown for two users in the bottom half of the figure. Uncorrected errors appear as artifacts in the video decode.

### Final Demonstration System

Figure 4 shows a screenshot of the final demonstration system in operation. The transmit video stream is shown along with the video stream received by two different LTE mobile users after the packets were transmitted over a noisy channel. The control GUI allows variable noise in the channel, along with modulation and encoding rate parameter settings for each user. The number of iterations used by the turbo decode is also variable.

The demonstration allows us to examine the behavior of the LogiCORE solutions when placed in a system with real-world data. In the case of the video streams shown in Figure 4, we used the same modulation scheme (QPSK) for both users. However, for user 1, we started increasing the data encoding rate, thus reducing redundancy in the data.

As we pass an encoding rate of 0.8, we cross a threshold and start to see a significant number of errors in the decoded video stream at this value of SNR. These errors appear as artifacts in the decoded video stream. In a real base station, higher layers in the LTE protocol stack would retransmit extra redundant data for the packet. To max-

imize efficient use of the channel, the base station has to balance the cost of retransmission against the benefits of lower overall data encoding rates, and also attempt to minimize latency in the system. These may feed into quality of service (QoS) parameters used by higher layers in the LTE protocol.

### Conclusion

The Xilinx Virtex-5 FXT device provides a tightly coupled integration of processor subsystem, DSP-enabled FPGA fabric, and high-speed communication. Such high levels of integration have allowed both the hardware and software elements of the LTE baseband reference system to be integrated on a single Xilinx FX70T part using standard hardware boards.

By using blocks available in the EDK toolkit to maximize IP reuse, and using Xilinx Platform Studio as a single integration framework, design teams can concentrate on the novel parts of the LTE downlink design. This has allowed rapid development and tracking of changes in the LTE specification as it approaches ratification. ●●

*Many thanks to other members of the LTE baseband design team: Beth Cowie, Graham Johnston, Andrew Laney, Neil Lilliot, Jorge Seoane, and Bill Wilkie.*



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