Design Embedded Systems with Xilinx and Synplicity

You can use the integrated Xilinx EDK and Synplicity's Synplify Pro or Synplify Premier software development flow to synthesize and debug.

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The Xilinx® Embedded Development Kit (EDK) is available to designers wishing to implement embedded designs using IBM PowerPC hard processor cores, Xilinx MicroBlaze™ embedded processor cores, and Xilinx-supplied implementations of buses, block RAMs, and peripherals such as USB and PCIe.

If you generated an embedded processor subsystem with EDK and wish to synthesize and debug your complete system for implementing on a Xilinx FPGA, you can do so using the Synplify Pro and/or Synplify Premier (referred to in this article as Synplify Pro/Premier) integrated embedded design flows from Synplicity, Inc. These Synplify Pro/Premier/EDK flows allow you to perform optimization and debug operations on an entire embedded FPGA system, including Xilinx embedded cores.

An integrated Synplify Pro/Premier/EDK flow allows designers to synthesize an entire design top-down as one design entity, handled as a single Synplify Pro/Premier design project.

Flow	When to Use	Details
ISE software/EDK hardware development flow (.ise project file)	Most processor-based embedded subsystems and designs with non-peripheral custom logic	• Allows the addition of non-peripheral custom logic to the system • Allows the addition of HDL files that contain non-peripheral custom logic directly to the project • You can integrate processor subsystems as either top-level modules or sub-modules
Standalone EDK hardware development flow (.xmp project file)	PowerPC or MicroBlaze processor-based embedded system or sub-modules	• The flow includes system top-level hardware synthesis, mapping, and place and route processes in the background so that it is not necessary to work with Xilinx ISE software to generate the configuration bitstream file. • Compiles and executes multiple software applications, generates libraries for the code, and merges software with hardware files for downloading to a target board. • Each hardware component is treated as an independent core (a separate XST project file is generated for each core). • During synthesis, XST automatically runs on each core separately to generate netlists (NGC files) through the Xilinx Xflow. • If the core is encrypted (MicroBlaze processor cores, for example), XST is always invoked to provide an NGC netlist.

Table 1 – Choosing which Synplify Pro/Premier/EDK flow to use

In addition to automating the flow, this integrated Synplify Pro/Premier/EDK flow offers the following advantages:

- Better quality of results (QoR): Synplify Pro/Premier considers the design in its entirety when performing timing-driven and area optimizations. Moreover, the tools can time through the core and may potentially optimize across EDK core boundaries, which improves design performance QoR.
- Visibility and debugging capabilities during implementation. You only need to run synthesis once to generate the final design netlist. Debugging and optional floorplanning can be performed on the entire design. You can also use Synplify Pro/Premier's HDL analyst, timing analyst, physical analyst, island timing analyst, and add-on Identify RTL debugging tool to debug and analyze the entire design.

Let's describe this flow in more detail.

Overview of Xilinx EDK Flow

The Synplify Pro or Synplify Premier tool from Synplicity is required to perform synthesis, as a part of the overall embedded FPGA hardware creation process, after the EDK cores have been included in the design. You can use the two available Xilinx EDK embedded hardware development flows that exist today to create your embedded design and to generate the embedded hardware in HDL format.

The two flows are:

- Xilinx stand-alone EDK hardware development flow for those using Xilinx Platform Studio (XPS)
- Xilinx ISE™ software/EDK hardware development flow for those using Xilinx ISE software

Table 1 includes additional details about which of these two flows to use. Figure 1 illustrates the overall design flow steps for both flows.

Integrated Synplify Pro/Premier/EDK Flow

The Synplify Pro/Premier/EDK flow comprises four steps, as shown in Figure 2.

Here are some details about each step.

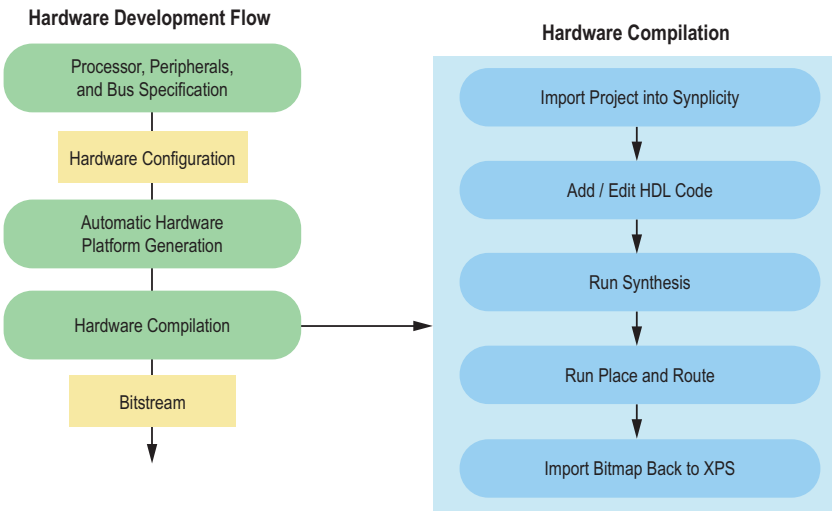

Figure 1 – Synplify Pro/Premier/EDK flow. Embedded cores are read into the Synplify Pro/Premier tool, where the design is fully synthesized. The post-place and route-generated bitmap is returned to Xilinx Platform Studio.

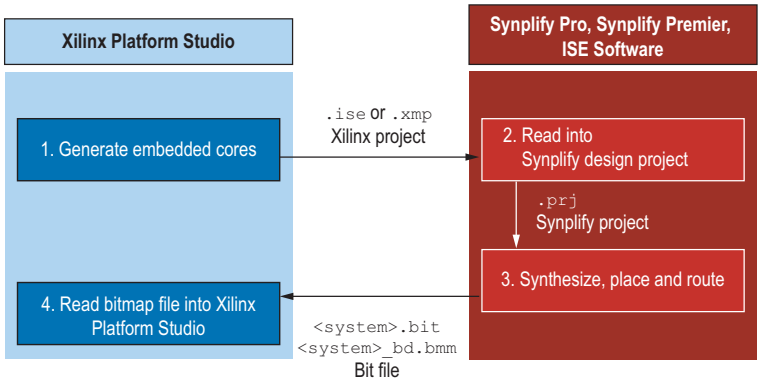

Figure 2 – The four steps involved in the EDK Synplify Pro/Premier flow.

1. Generate embedded cores using XPS or ISE software. Create an EDK project that Synplify Pro/Premier can read to generate a core netlist using one of the two flows for XPS users:
   - The Xilinx stand-alone EDK hardware (generates an .xmp file)
   - Xilinx ISE software/EDK hardware development flow (generates an .ise file) for ISE software users

   In the XPS GUI:
   - Select Project > Project Options > Hierarchy and Flow
   - Select Implement Design in ISE software (Export to Project Navigator Flow: Depreciated)
   - Select Hardware > Generate Netlist to generate the netlist

   The .ise or .xmp file generated will refer to a variety of design files that represent the core. These files are shown in Table 2.

2. Read the generated files into Synplify Pro/Premier design project. The files that Synplify Pro and Synplify Premier automatically read are listed in Table 3. The Synplify Pro/Premier tools read the NGC netlist and EDK-generated platform (as specified by the .ise/.xmp project files); they are automatically included in the design project. The Synplify Pro/Premier software reads many different files that are part of the Xilinx project file, including RTL, netlists, and constraints (V/VHD, EDN, NGC, NGO, SDC, UCF, OPT). It adds these definition and constraints files to the synthesis project it creates before running synthesis.

Files and Directories Created by EDK	
.xmp	Xilinx microprocessor project file
.mhs	Microprocessor hardware specification file
.mss	Microprocessor software specification file
pcores/	User IP cores
hdl	HDL wrappers (encrypted cores)
etc/	UCF Xilinx constraint files
data/	Place and route option files
synthesis/	Synthesis files
implementation/	Top-level place and route results, block .ngc netlist files

Table 2 – The embedded core files generated by EDK software

Note that any custom HDL logic will be included in the .ise project file and read automatically by the Synplify Pro/Premier tool if you used the Xilinx EDK/ISE hardware development flow. However, you must add these files manually to the Synplify Pro/Premier project if you are using the Xilinx stand-alone EDK hardware development flow.

3. Invoke and run Synplify Pro/Premier, then place and route.
   - In the Synplify Pro/Premier tool, open the Synplify Pro/Premier design (.prj) project, which now includes the .ise/.xmp embedded cores. The cores will now be part of the Synplify Pro/Premier design.
   - If the EDK cores are a subsystem in a larger design, simply instantiate the subsystem into the top-level HDL design.
   - Run synthesis and then complete place and route using the normal Synplify Pro/Premier ISE software flow. You can run Xilinx place and route from the Synplify Pro/Premier interface to generate a top-level hardware bitmap file.

Table 4 shows the output files created after synthesis, including a bitmap file.

4. Read bitmap back into XPS.
   - Import the bitmap file back into the XPS environment. The <system>.bit and <system>_bd.bmm files originally found in the synplify/rev_1/par_1 directory should be placed in the "implementation" directory within the EDK project directory. In the XPS GUI, select Project > Import from ProjNav.
   - Select the BIT and BMM files from the PAR directory
     - BIT file synplify/rev_1/par_1/<system>.bit
     - BMM file synplify/rev_1/par_1/edkBmmFile_bd.bmm

Input Files Read by Synplify Pro/Premier	
.ise	Project file in ISE software project directory, if created
.xpm and .mhs	Project file in EDK project directory, if created
.mpd, .pao, HDL (.v, .vhd), .edn, .ngo, .ngc	Design specification files in EDK project directory, if available, or in EDK hardware library in a location specified through the EDK installation path

Table 3 – These EDK files are read by Synplify Pro and Synplify Premier

Output Files Created by Synplify Pro/Premier	
.prj	Project file
.sdc	Constraint file
.ucf	Xilinx user constraint file
OPT file and core wrapper file	Xilinx Xflow OPT file and core wrapper file generated, if the core is a black box to the Synplify directory (for example, if the core was encrypted)
.bmm	Bitmap file – in Synplify Pro/Premier place and route directory

Table 4 – Output files generated by Synplify Pro and Synplify Premier, ready for Xilinx Platform Studio to read

   - Click OK
   - Run Device Configuration > Update Bitstream. You can now download the bitstream into the FPGA.

Encrypted Cores

In some cases, the cores are encrypted by Xilinx (for example, Xilinx MicroBlaze processors). You can merge these cores into your design with Synplify Pro/Premier. The core may appear as a black box in the tool.

The PAO file generated by XPS will point to an encrypted IP core definition file. Synplify Pro/Premier software allows you to specify the appearance of the core as a black box (in which case the core wrapper file will be present and copied into the Synplify Pro/Premier folder). If you specify that the core should not be treated as a black box – in other words, a predefined netlist exists for the core – the tool will seek to locate a definition file named implementation/<core>.ngc. If it finds the file, it adds it to the Synplify Project .prj file. If it does not find the implementation/<core>.ngc file, it issues an error message.

In Synplify Pro/Premier software version 9.0.2 and above, a new secure .ngc flow exists that allows you to easily include encrypted cores in the synthesis flow. It also allows the Synplify Pro/Premier tool to additionally optimize inside cores, resulting in better overall QoR.

Conclusion

An increasing percentage of FPGA designs include cores. For designers generating microprocessor and peripheral design cores using the Xilinx Embedded Development Kit (EDK), the Synplify Pro and Synplify Premier software tools offer a fully integrated flow that allows you to synthesize and implement an FPGA system.

These tools offer better QoR and a more convenient flow, as well as full design debugging and analysis during the synthesis and placement phases. For more information, contact Synplicity customer support at *support@synplicity.com.*