

# Application Notes

If you want to do a bit more reading about how our FPGAs lend themselves to a broad number of applications, we recommend these application notes.



**XAPP1106: Using and Creating Flash Files for the MicroBlaze Development Kit – Spartan-3A DSP 1800A Starter Platform**

[www.xilinx.com/support/documentation/application\\_notes/xapp1106.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1106.pdf)

In this application note, Sundararajan Ananthakrishnan describes the files for programming the serial flash memory and the StrataFlash memory for the MicroBlaze™ Development Kit – Spartan™-3A DSP 1800A Starter Platform.

The reference system executes the HelloWorld software application (running from serial flash) using the SPI configuration mode and the BlueCat Linux image (from StrataFlash) in BPI configuration mode. Ananthakrishnan includes the files you need to run the BlueCat Linux reference system from StrataFlash memory and the HelloWorld application from the serial flash. The application note also describes how to use the files – as well as create new files – to run the reference system successfully from flash memories.

**XAPP514: Audio/Video Connectivity Solutions for Virtex-II Pro and Virtex-4 FPGAs: Reference Designs for the Broadcast Industry: Volume 1**

[www.xilinx.com/support/documentation/application\\_notes/xapp514.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp514.pdf)

This is a comprehensively updated collection of reference designs for designers tackling applications in the broadcast industry.

Xilinx updated XAPP514 earlier this year, adding among other things a new chapter (Chapter 9), entitled “Introduction to the SMPTE High-Definition Serial Digital Interface Standards.” The new chapter describes how the SMPTE 3G-SDI standard is emerging to replace dual-link HD-SDI, to accommodate higher bandwidth video formats running at 3 Gbps and higher. The standard uses the same electrical characteristics and scrambling as HD-SDI, but doubles the bit rate to almost 3 Gbps.

This document also discusses why 3G-SDI is an attractive alternative to dual-link HD-SDI because it uses a single cable instead of a pair of cables.

**XAPP860: 16-Channel, DDR LVDS Interface with Real-Time Window Monitoring**

[www.xilinx.com/support/documentation/application\\_notes/xapp860.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp860.pdf)

In this application note, Greg Burton describes a 16-channel, source-synchronous LVDS interface operating at double data rate (DDR). The transmitter (TX) requires 16 LVDS pairs for data and one LVDS pair for the forwarded clock. The transmitter operates at 6:1 serialization on each of the 16 data channels.

The receiver (RX) also requires 16 LVDS pairs for data and one LVDS pair for the source-synchronous clock input. The receiver operates at 1:6 deserialization on each of the 16 data channels. Burton describes the timing of the receiver in depth and characterizes it in hardware.

This application note has a sister note, XAPP855, entitled “16-Channel DDR LVDS Interface with Per Channel Alignment” ([www.xilinx.com/support/documentation/application\\_notes/xapp855.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp855.pdf)). The design technique discussed in XAPP860 has all of the same features, as well as an additional window monitoring circuit, boosting the performance above that of the design described in XAPP855. But the added performance comes at the expense of additional logic utilization.

**XAPP453: Spartan-3 FPGA Family Advanced Configuration Architecture**

[www.xilinx.com/support/documentation/application\\_notes/xapp453.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp453.pdf)

This 14-page application note presents an approach to configure Spartan-3 FPGAs from a 3.3-V interface. It provides a set of connection diagrams for each configuration mode. These diagrams are complete, ready-to-implement solutions.

You can also apply the approach outlined in this paper to the Spartan-3E family, although pin names and banks are different. The Spartan-3A/3AN/3A DSP families allow  $V_{CCAUX}$  to be 3.3V, simplifying the interface. ●●