

The Path to Successful Design

The Xilinx Customer Education group can help you gain the knowledge and skills you need to innovate with Xilinx FPGAs.

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With an ever-increasing number of electronics companies turning to Xilinx® FPGAs, our company has made it a top priority to make world-class training available to designers.

Today, our Customer Education group offers comprehensive curriculum paths, including our popular “FPGA Design Curriculum Path,” comprising three core classes:

1. “Fundamentals of FPGA Design”
2. “Designing for Performance”
3. “Advanced implementation Techniques”

In the “Fundamentals of FPGA Design” course, we focus on the use of Xilinx Project Navigator to implement and simulate an FPGA design. We’ll show you how to read reports to determine whether you have met your design goals, and how to use the architecture wizard to create digital clock manager (DCM) instantiations.

We’ll also use the Floorplan Editor and PinAhead tools to help you with pin assignment, and the Constraints Editor to enter global timing constraints, locating and modifying implementation options as necessary.

In the “Designing for Performance” course, we build on the fundamentals by describing a flow to help you obtain timing closure. In this course, we also describe the architectural features of the Virtex™-5 FPGA and review the features of the DCM and phase-locked loop (PLL), explaining how you can use them to improve performance.

We’ll also look at how you can increase design performance through duplicating registers and pipelining, and describe different synthesis options and how they improve performance. We look at how to create cores and

integrate them into your design flow using CORE Generator™ software, and how to run behavioral simulation on an FPGA design that contains cores.

We’ll show you how to pinpoint design bottlenecks with timing analyzer reports and how to apply advanced timing constraints to your design to meet your performance goals. We’ll also show you how to use advanced implementation options to increase design performance.

Finally, if you are an advanced user, we offer a course on “Advanced Implementation Techniques.” In this course, we create and edit timing constraints in the UCF file and use Tcl-based scripting to implement a design.

We’ll also show you how to analyze I/O interface timing and implement timing

constraints and design modifications to meet system and source-synchronous I/O interface timing. We’ll demonstrate how to use partitions and SmartGuide™ technology to preserve timing results, and discuss floorplanning techniques to enhance timing and optimize the post-place and route design in the FPGA Editor for more efficient in-circuit testing.

This quarter, we are featuring all three of these classes at multiple North American locations. To see a schedule, visit www.xilinx.com/support/training/abstracts/Class-Schedule-by-Course.pdf.

In addition, our network of authorized training providers is dedicated to helping you become successful. To find your local authorized training provider, visit www.xilinx.com/support/training/atp.htm. 🌈

Upcoming Conferences

In addition to offering training at multiple locations, we exhibit our technologies at several conferences.

Conference	Date	Location
NI Week 2008	August 5-7, 2008	Austin, TX
IBC2008	September 11-16, 2008	Amsterdam, Netherlands
MAPLD Conference 2008	September 15-18, 2008	Annapolis, MD
Convergence 2008	October 20-22, 2008	Detroit, MI
SDR Forum	October 26-30, 2008	Washington, DC
Electronica 08	November 11-14, 2008	Munich, Germany
MILCOM 2008	November 17-19, 2008	San Diego, CA
Embedded Technology 2008	November 19-21, 2008	Yokohama, Japan
InterBEE	November 19-21, 2008	Chiba City, Japan
CES 2009	January 8-11, 2009	Las Vegas, NV
Mobile World Congress 2009	February 16-19, 2009	Barcelona, Spain
Embedded World 2009	March 3-5, 2009	Nuremburg, Germany
Embedded Systems Conference	April 1-5, 2009	San Jose, CA