

Xcuse Us

To err is human...

Welcome to a new section in Xcell Journal called “Xcuse Us: To err is human ...” If you use software of any kind, chances are you’ve encountered a software glitch or bug and had to locate a patch to fix the problem (if you haven’t used software of any kind, chances are you are an analog designer).

Imagine how hard it is to develop a conventional software program; now imagine how hard it is to develop a program that allows you to design and program IC technology, which is ever-changing. Here at Xilinx, our Solutions Group is constantly developing software and flows for new silicon and is even creating multi-discipline design tools by developing tools for embedded software and DSP development, as well as logic design.

As you can imagine, it isn’t easy task. We try to proactively catch issues with our tools, but sometimes a bug or 10 slips through our detection ... and we’re sorry. Fixing issues is a top priority as they arise.

Other times, we update tools simply to add new features to help you design more efficiently. Therefore, in each issue of Xcell Journal we’ll keep you up-to-date on our latest patches, updates, and service packs. You can also visit the Xilinx® Download Center at www.xilinx.com/download to see and download the latest patches developed between issues of Xcell Journal.

Here are the most current updates to Xilinx design products and IP as of June 30, 2008.

The Xilinx flagship FPGA development environment is ISE™ Foundation™ software, which is a configurable suite of individual design tools. You can select (and purchase) which tools in the suite are best suited to your specific design requirements; you don’t have to purchase tools you don’t need.

The ISE design suite includes logic tools: ISE Foundation software, ChipScope™ Pro analyzer, ChipScope Pro serial I/O toolkit, and PlanAhead™ design tools. It also includes the Embedded Development Kit for embedded software development, and System Generator for DSP and the AccelDSP™ synthesis tool for DSP programming.

Logic Design Tools

ISE Foundation Software

Description: The industry’s most complete programmable logic design solution

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to significant quality improvements, Service Pack 2 reduces simulation run times with improvements in the models for GTP transceivers in the Virtex™-5 FPGA family. You can expect 2x-7x faster simulation run times.

Service Pack 2 also provides support in the XPower estimator for the Virtex-5 FXT FPGA family; updated power modeling for the Spartan™-3A FPGA family; and numerous updates to the Xilinx power estimator spreadsheets for Spartan-3 Generation FPGAs.

ISE Software Simulator

Description: A complete, full-featured HDL simulator integrated with ISE Foundation software

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ModelSim Xilinx Edition III (MXE-III)

Description: A low-cost version of the industry’s most popular simulation environment

Latest Version Number: 6.3c

Date of Latest Release: March 2008

Previous Release: 6.2g

Download the Latest Patch: N/A

Revision Highlights: No new updates since the release of ISE software design suite 10.1

PlanAhead Design Tools

Description: A faster, more efficient FPGA design solution to help achieve your performance goals in less time

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ChipScope Pro Analyzer and the ChipScope Pro Serial I/O Toolkit

Description: Real-time debugging and verification tools for Xilinx FPGAs

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ISE WebPACK™ Software

Description: A free solution for your Xilinx CPLD or medium-density FPGA designs

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/webpack

Revision Highlights: See the revision highlights for ISE Foundation software; these improvements apply to all devices supported in ISE WebPACK software.

Embedded Design and DSP Tools

Platform Studio and EDK (Embedded Development Kit)

Description: An integrated development environment comprising embedded processing tools, a MicroBlaze™ embedded processor, IP, software libraries, and design generators

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements, Service Pack 2 provides full access to the Virtex-5 FXT family of FPGAs and new support for the automotive versions of the Spartan-3A and Spartan-3A DSP FPGA families.

Base System Builder, included in the EDK, provides support for the ML507, a general-purpose FPGA, RocketIO™ GTX transceivers, and an embedded system development board.

A new floating-point unit core is now available for designs targeting Virtex-5 FPGA families. This new core includes an APU interface and is supported in the Base System Builder.

System Generator DSP Tool Kit

Description: Enables the development of high-performance DSP systems using products from The MathWorks

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements and support for MATLAB 2008a from The MathWorks, Service Pack 2 introduces a new clocking option to automatically include a digital clock manager (DCM), allowing designs to have more than three clocks and clock rates.

Service Pack 2 also includes two new DSP block set enhancements with the addition of the FIR Compiler 4.0 – with all of the features supported by the FIR Compiler LogiCORE IP v4.0 – and Divider Generator 2.0, which generates arithmetic division algorithms for integer division.

AccelDSP Synthesis Tool

Description: Option for System Generator for DSP, enabling a top-down MATLAB language-based DSP design methodology

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements and support for MATLAB 2008a from The MathWorks, Service Pack 2 allows the use of Xilinx-optimized LogiCORE IP in generated HDL for all supported operators.

Xilinx IP Updates

Name of IP: ISE Software IP Update 10.1.2

Type of IP: All

Targeted Application: Xilinx develops IP cores and partners with third-party IP providers to decrease customer time to market. The powerful combination of Xilinx FPGAs and IP cores provides functionality and performance similar to ASSPs, but with flexibility not possible with ASSPs.

Latest Version Number: 10.1.2

Date of Latest Release: March 2008

Previous Release/Release Date: 10.1.1i (April 2008)

Access the Latest Version:

www.xilinx.com/download

Revision Highlights: Xilinx IP cores, including LogiCORE IP cores, are delivered through software updates available from the Xilinx Download Center. The latest versions of IP products have been tested and delivered with the current IP release.

In addition to quality improvements, Service Pack 2 for ISE software IP update 10.1.2 provides new features, functionality, and examples for many Xilinx LogiCORE IP cores.

Here is a partial list of significant changes in Service Pack 2:

- Endpoint block plus wrapper for PCI Express v1.8. Added new dual-core example design for Virtex-5 FX70T devices and Fast Functional Simulation model support for Virtex-5 FPGA GTP-based transceiver configurations.
- Virtex-5 FPGA RocketIO GTX wizard v4.1. Enhanced with new OBSAI and PCI Express Gen2 protocol templates and support for the GTX-DUAL Fast Functional Simulation model.

- Virtex-5 FPGA RocketIO GTP wizard v1.9. Added TX phase alignment updates, selectable PPM offset, support for the GTP_DUAL FAST Functional Simulation Model, and support for Synplicity's Synplify 9.2.
- Serial RapidIO v4.4. VHDL wrapper support for Virtex-5 FPGA families. Two new ports added to support capture and retransmission of request packet original destination IDs.
- FIR Compiler v4.0. Distributed architecture support for Virtex-5 FPGAs/Spartan-3A DSP devices, extended data and coefficient bit widths to 49 bits, polyphase filter bank for channelizer applications, and support for as many as 16 parallel data paths. System Generator 10.1.2 supports all features of FIR Compiler v4.0.
- Divider Generator v2.0. Added support for Virtex-5 FPGAs/Spartan-3A DSP devices. A new high radix divider algorithm supports as many as 54 bit operands, also supported in System Generator 10.1.2.

In addition:

- OBSAI v2.1. Added support for the Virtex-5 FXT family of FPGAs.
- SPI-4.2 Lite v4.3. Verilog support for the Synopsys VCS simulator.
- Aurora 64b/66b v1.2. Enhanced frame generator and frame checker, updated GTX attributes, and support for multiple lanes.
- Aurora v3.0 for Virtex-5 FPGA families. Xilinx ISE software simulator and Cadence NCSim simulator support, SecureIP encrypted model support for MTI ModelSim, and support for changing lane assignments within a tile.
- Discrete Fourier transform v3.0. Addition of 1296- and 1536-point sizes for 3GPP-LTE wireless systems and the option to trade off between area resources or speed performance. 🎨

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