Tools of Xcellence

News and the latest products from Xilinx partners.

Welcome to the "Tools of Xcellence" section. In each issue, our staff will interview tool, IP, and development board vendors about their latest product introductions and upgrades. From time to time, we'll also include write-ups of significant business moves that could impact the Xilinx user community.

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Combined Synopsys/Synplicity Holds Potential for FPGA Tool Innovations

Synopsys Inc.'s $223 million acquisition of its longtime FPGA synthesis rival Synplicity in May has left many Synplicity tool users wondering how the acquisition will affect them.

George Zafiropoulos, vice president of solutions marketing at Synopsys, said to only expect good things: no Synplicity tools are going away. Additionally, Ken McElvain, the cofounder of Synplicity and designer of Synplify, is staying at Synopsys indefinitely. The company will function as an independent business unit within Synopsys, developing tools leveraging the strengths of both companies.

In the early 1990s, McElvain and his wife Alisa Yaffa left Mentor Graphics to found Synplicity. The company's first product, the Synplify FPGA synthesis tool, was an instant success. In those days, FPGA synthesis tools were typically complex and had very long run times. In contrast, Synplicity users reported being stunned by Synplify's speedy run times – many users reported hitting the "synthesize my design" button more than once before figuring out that Synplify had actually synthesized their designs very quickly.

This success led to dominant market share in FPGA synthesis, an IPO in 2000, and product launches of Synplify variants and new tools like the Identify debugger, the Certify ASIC prototyping/partitioning tool, and Amplify ASIC/structured ASIC synthesis (Synplicity shelved the latter tool in 2007).

Synplicity even acquired Hardi Electronics to bolster its play in FPGA-based ASIC prototyping (see info about the new HAPS 51T prototyping board later in this article), leading to the release of the Confirma ASIC/ASSP platform, which combines Certify, Hardi boards, and Identify in one package.

Meanwhile, Synopsys – hoping to leverage its dominant position in ASIC synthesis tools – made three attempts to swipe market share from Synplicity over the last decade, first launching FPGA Compiler in the early 1990s, FPGA Express in the mid '90s, and FPGA Compiler II in the late '90s. All of these tools were fairly short-lived (FPGA Compiler II was "end of lifed" at the end of 2006), as Synplicity continued to innovate its tools with each new generation of FPGA silicon.

Indeed, Synopsys's acquisition is, in a way, an "if you can't beat 'em, buy 'em," acquisition.

Zafiropoulos said that Synplicity will now function as Synopsys's sixth business unit, headed by Gary Meyers, Synplicity's president and CEO, now GM of the Synplicity business unit. Ken McElvain, said Zafiropoulos, is essentially serving as the group's CTO, developing next-generation tools.

"Synplicity is extremely well-known for its FPGA synthesis tools, but over the years [the company] expanded into verification

and they've done some great work there," said Zafiropoulos. "Before the acquisition, our two companies had been collaborating on flows in the verification area and now we've stepped up development." Zafiropoulos declined to elaborate on future tool or flow offerings.

Verification Tools and Methodologies

Although Synopsys may not have had the greatest record competing against Synplicity in the FPGA space, Synopsys does own a full suite of verification tools, including the popular VCS simulator. It also has formal analysis, debugging, and test bench generation, all supporting advanced assertion-based verification.

Zafiropoulos points out that many FPGA designers today use VCS for simulating their code, but as FPGAs become more complex and reach into the millions of gates, FPGA designers are starting to apply ASIC verification methodologies to their FPGA verification flows.

A few years ago, Synopsys acquired SystemVerilog inventor Co-Design Automation. SystemVerilog is just finding traction in mainstream ASIC design, and it's just now starting to gain traction in FPGA design. It's possible that the combined Synopsys/Synplicity could accelerate usage of SystemVerilog methodologies in the FPGA design community.

A key to success in these endeavors will be making sure that the new technologies are suited to the varying skill levels of FPGA users. Indeed, over the last few years, the FPGA user base has expanded beyond traditional hardware designers to include embedded system developers and DSP programmers. Zafiropoulos points out that Synplicity has also been serving that growing user base, having released Synplify DSP in 2004, a DSP synthesis tool for both FPGA and ASIC end implementations.

Aldec Upgrades Active-HDL, Releases ALINT Design Rule Checker

Aldec Inc. (Henderson, Nevada) has released the 8.1 version of its flagship product, Active-HDL, adding various functionality and performance improvements to the tool. At the Design Automation Conference (DAC) in June, the company also announced a new design rule checker called ALINT.

Lori Nguyen, Aldec's director of marketing, said that with the 8.1 release, Active-HDL performs VHDL simulation faster than competing tools and simulates SystemVerilog with the same performance as competing tools. "And we're about 30% less expensive," Nguyen added.

Igor Tsapenko, manager of applications engineering, said that with version 8.1 Aldec is now making its SLP-enhanced Verilog simulation engine the default simulation engine for the tool. Previously, Aldec offered SLP as an option to the tool.

Active-HDL has included various coverage tools such as code coverage and expression coverage for several years now, but each tool used a separate database. In version 8.1, Aldec has added a unified code coverage database to Active-HDL.

The company also improved the performance of Active-HDL's waveform viewer and made general improvements to the tool, in particular Active-HDL's graphical entry tool. This tool allows designers to build designs with either a block diagram editor or finite state machine editor instead of hand-coding their designs using HDL. In the 8.1 release, the company is adding a code coverage engine to the FSM editor.

Nguyen said that in March 2009, the company plans to issue the 8.2 version of Active-HDL, which will add to the tool graphical entry support for SystemVerilog.

ALINT

At DAC, the company also announced a new linting product, ALINT. Linting tools essentially allow designers to check that their code complies with various styles and standards.

"What's unique about our tool is that we support the 2006 STARC rules set, where most other tools on the market today only currently support STARC's 2002 rules set," said Nguyen. "And we also support clock domain crossing rules sets."

The Semiconductor Technology Academic Research Center (STARC) in Japan specifies, among other things, a 250-rule synthesizable subset for HDL coding. This helps ensure that its member companies create code that can they effectively and efficiently synthesize with commercial EDA ASIC and FPGA synthesis and FPGA vendor synthesis tools.

In addition to support for various synthesis rules, ALINT also supports coding style rules as well as rules for various verification techniques.

The tool features two application interfaces: Configuration Manager and Violation Viewer. Configuration Manager allows you to specify what rules sets you'd like the tool to check. Violation Viewer allows you to locate violations in your source code so you can fix them.

Currently, the tool only supports Verilog, but the company expects to make full VHDL support available by October 2008, with complete Verilog, SystemVerilog, and VHDL mixed-language support by February 2009.

Nguyen said that ALINT currently includes several customization features that allow users to modify existing rules and policies to make sure designers are coding to their company's best practices guidelines. It plans to expand that feature in a future release to allow users to create their own rules. Plus, the company plans to add an Aldec rules set as well as rules sets from FPGA vendors to that release.

Nguyen claims that ALINT is more robust than other commercial tools, and at a starting price of $7,500 for a simulator upgrade and a stand-alone version for $13,000, roughly half the cost.

Aldec offers several versions of Active-HDL. The single-language version of the tool starts at $3,500, while the full-featured mixed language version is $20,000.

Synfora Launches PICO Extreme FPGA, a C-to-FPGA Algorithmic Synthesis Tool

At DAC, tool vendor Synfora Inc. (Mountain View, California) announced the availability of its new C-to-RTL algorithmic synthesis tool targeted for FPGAs, PICO Extreme FPGA.

In February 2008, Synfora and Xilinx announced that the two companies were beta-testing the new Synfora technology, specifically on Virtex™-5 devices and low-cost Spartan™-3A DSP FPGAs. The tool is now out of the testing phase, so Synfora is making it available (for a licensing fee) to the mass market supporting Spartan-3, Virtex-4, and Virtex-5 device platforms.

"If you look at an FPGA, it has certain fabric components like the MicroBlaze™ embedded processor, DMA, USB, PCIe ... these cores don't fully define the device," said Synfora's CEO, Simon Napper. "What defines the functionality is what we call the application engine: the wireless modem, the video codec, imaging pipeline. And increasingly, designers are specifying this type of functionality in C."

In the Synfora scheme of things, customers will typically use PICO Extreme FPGA at the beginning of a design project (see Figure 1). Users start a project by first creating an architecture template with the tool, which Napper said requires some knowledge of hardware but is essentially an untimed C file that you run in a GNU compiler, or the C compiler of your choice. "The architecture template is a C file that captures the hardware properties you desire (shared memory, streaming data)," said Napper. "To validate that this is correct, PICO Extreme FPGA generates a block diagram of the hardware it will create based on the C code."

After that, said Napper, you populate the diagram with C code and run the PICO Extreme FPGA compiler, which generates RTL. PICO Extreme FPGA also creates all of the scripts necessary to run the XST/Synplicity tool flows. "You don't really need to know anything about the hardware," Napper said. And if your design requires any optimizations, you can implement those in C as well, he added.

As with the ASIC version of Synfora's PICO Extreme, PICO Extreme FPGA also allows more advanced users to reduce the area of certain blocks in the FPGA using Synfora's tightly coupled accelerator blocks (TCABs). "TCABs are user-definable procedures that the compiler can encapsulate and reuse as a fundamental building blocks in your design," Napper explained. "If you have a function that the compiler calls many times, you can build it as a TCAB and reduce area. It will also improve the run time of PICO Extreme FPGA."

The maiden release of PICO Extreme FPGA is primarily focused on video for high-end TVs, video analytics, and imaging applications. "What we've done is work with Xilinx to integrate with their fixed fabric for video applications. There's essentially a slot where users insert their unique video algorithms," said Napper. At DAC, Synfora demonstrated the system running a Sobel algorithm on a Xilinx Spartan-3 device. "You could do the same thing with a deblocking filter algorithm or an image enhancement algorithm," said Napper. "Once you've created the fabric, you have a script file that just builds it."

Napper believes that Xilinx® users will find the tool especially useful if they are moving a design they've traditionally implemented in a DSP to an FPGA.

Xilinx customers can also use the tool complementary to The MathWorks's MATLAB-Simulink flow. "Many designers use MATLAB to create an executable specification of their functions," said Napper. "They can also now rewrite that specification in C using PICO Extreme FPGA and then do equivalence checking to make sure that the MATLAB specification and C are the same. It's easy to do equivalence at that level because MATLAB can accommodate C models."

PICO Extreme FPGA comes pre-characterized for Spartan-3, Virtex-4, and Virtex-5 devices and with an existing board support package for the Spartan-3E Development Kit. Pricing for PICO Extreme starts at $210,000.

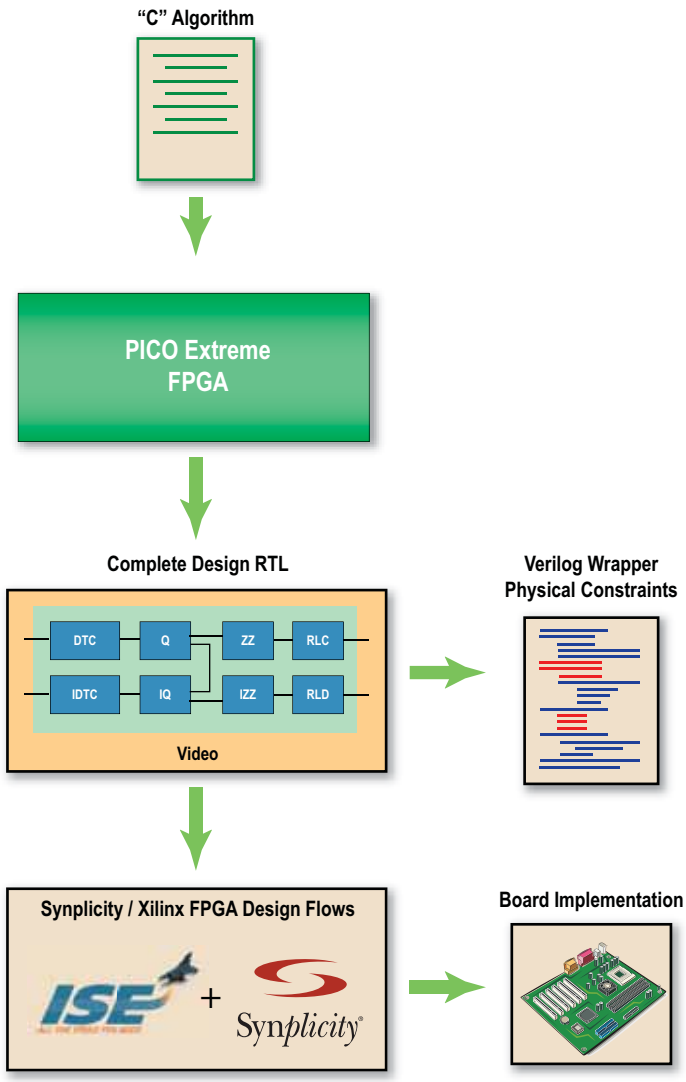

Figure 1 – The PICO Extreme flow synthesis tool generates RTL from C.