

AccelDSP can also generate gates directly from MATLAB code and we can use it synergistically with System Generator for DSP. Furthermore, the AccelDSP synthesis tool is well suited for feasibility analysis and fast prototyping. It automatically quantizes the original floating-point MATLAB into fixed-point, and it maps the various MATLAB instructions into the FPGA resources. This is probably the easiest-to-use DSP tool that Xilinx provides to driver assistance algorithm designers and system architects.

In short, algorithm designers and system architects working on driver assistance technology can nowadays rely on a highly sophisticated DSP design tool to build their reference algorithmic models, and then easily implement those models into Xilinx FPGA low-cost devices. The

result is high quality, high performance and low cost simultaneously.

One crucial feature of System Generator for DSP is the capability to implement a portion of the design into the silicon target device (of a specific board connected via Ethernet) while the remaining part runs on the host PC. Such a hardware-software co-simulation allows easy verification of the hardware behavior while also accelerating simulation speed.

As you can see, we used the Xilinx System Generator for DSP to create an image-preprocessing pipeline for an LDW system. While in this discussion we only revealed some of the details of one of its modules, namely the GNR 2-D FIR filter, the entire lane detection preprocessing function (shown in Figure 2) took

only 12 DSP48, 16 BRAM and 2,594 slices of an XA Spartan-3A DSP 3400 device, running at 128.24 MHz with an input data rate of 14.2 MSPS, 50 percent higher than what is needed by VGA image resolution. The whole algorithm design and FPGA implementation required a few weeks of work and did not necessitate the writing of any VHDL code.

We look forward to continuing the project by implementing the extraction and tracking of the lane models in the AccelDSP design tool and then integrating such stages within the System Generator for DSP model. For further detail you can contact any of us by e-mail. (The authors are grateful to professor Vittorio Murino of the computer science department at Verona University for his support and contributions.)

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