

Xilinx Tool & IP Updates

Xilinx is continually improving its products, IP and design tools as it strives to help designers work more effectively. Here we report on the most current updates to the flagship FPGA development environment, the ISE® Design Suite, as well as other design tools and IP. The latest service packs offer significant enhancements and new features. Keeping your installation of ISE up to date with these service packs will ensure the best results for your design.

Updates are available from the Xilinx Download Center at www.xilinx.com/download. For more information on the ISE Design Suite or to download free 60-day evaluations of any of the products, visit www.xilinx.com/ise. Also, see the Tools of Excellence section in this issue for news of IP, tools and development boards from Xilinx partners.

Logic Design Tools

ISE Foundation™ Software

Description: The industry's most complete programmable logic design solution

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: Besides adding support for the new Virtex®-5 TXT FPGA Platform as well as quality improvements, Service Pack 3 provides enhancements to the ISE Project Navigator, Constraints Editor, CORE Generator™ System, Floorplan Editor and implementation tools.

With Service Pack 3, the IBISWriter now provides updates to the IBIS models for the Virtex-5 family of FPGAs through XilinxUpdate.

ISE Simulator

Description: A complete, full-featured HDL simulator integrated with ISE Foundation

Latest version number: 10.1.3

Date of latest release: June 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: Support for the new Virtex-5 TXT FPGA Platform and quality improvements

ModelSIM Xilinx Edition III (MXE-III)

Description: A low-cost version of the industry's most popular simulation environment

Latest version number: 6.3c

Date of latest release: March 2008

Previous release: 6.2g

Revision highlights: No new updates since the release of the ISE Design Suite 10.1.

PlanAhead™

Description: A faster, more efficient FPGA design solution to help achieve your performance goals in less time

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: Support for the new Virtex-5 TXT FPGA Platform and quality improvements

ChipScope™ Pro and ChipScope Pro Serial I/O Toolkit

Description: Real-time debug and verification tools for Xilinx FPGAs

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: In addition to support for the new Virtex-5 TXT FPGA

Platform and quality improvements, Service Pack 3 also improves the scroll bar in the Waveform viewer Bus/Signal column to adjust scroll and justify text. This new feature makes it easier to view signals and buses with extremely long hierarchical names.

Support for the Virtex-5 TXT FPGA Platform is now available for all ChipScope Pro and ChipScope Pro Serial I/O Toolkit cores, including the IBERT core. In addition, Service Pack 3 also includes improvements to the ChipScope Pro Serial I/O Toolkit to determine the optimal Decision Feedback Equalizer settings for the Virtex-5 GTX RocketIO™ transceivers.

ISE WebPACK™

Description: A free solution for your Xilinx CPLD or medium-density FPGA design

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/webpack

Revision highlights: The improvements described above in the revision highlights for ISE Foundation apply to all devices supported in ISE WebPACK.

Embedded Design and DSP Tools

Platform Studio and EDK (Embedded Development Kit)

Description: An integrated development environment of embedded processing tools, MicroBlaze™ soft processor core, IP, software libraries and design generators

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: In addition to quality improvements, Service Pack 3 includes

support in the EDK's Base System Builder for the Virtex-5 FPGA ML510 Embedded Development Platform.

Service Pack 3 also includes new IP cores in Platform Studio. In System Flash v1.00a simplifies access to the on-board flash memory for the nonvolatile Spartan®-3AN family of FPGAs, while TFT Controller 1.00a provides easy control of the text display on FPGA development boards. In addition, Agilent trace capture tools support early versions of the MicroBlaze soft processing core. Upgraded trace capability includes capture of new MicroBlaze instructions such as those for MMU, PID, FPU and FSL.

System Generator for DSP Tool Kit

Description: Enables development of high-performance DSP systems using products from The MathWorks, Inc.

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: In addition to quality improvements, Service Pack 3 adds new support for the FFT 6.0 blockset in System Generator, providing up to 34 bits data and phase factor width. Other improvements support block floating-point scaling for streaming, pipelined and I/O architecture, and DSP48 abstraction for mathematical operators.

Accumulators, AddSub and counter blocks can now be implemented using either a DSP48 or the original LUT-based implementation, providing design portability across all supported Xilinx devices.

Thanks to enhanced printing support, users can now print directly from the WaveScope toolbar or file menu without having to perform manual screen captures. Finally, new IP version checking provides a warning if an IP core scheduled to be removed in a future version of System Generator for DSP is used.

AccelDSP™ Option to System Generator for DSP

Description: Enables a top-down MATLAB® language-based DSP design methodology

Latest version number: 10.1.3

Date of latest release: September 2008

Previous release: 10.1.2

Download the latest patch:

www.xilinx.com/download

Revision highlights: In addition to quality improvements, Service Pack 3 includes the “use_logiccore” directive, which tells AccelDSP to use an optimized LogiCORE™ for the specified operator in the design, allowing greater quality-of-results. Also, a new optional parameter called “enable” has been added to the “insertpipestage” directive. This allows you to specify whether or not an associated hierarchical directive is enabled or disabled.

A new parameter called “register_output,” which has been added to the “memmap” directive, allows you to specify whether or not the output of the memory is registered. And a new parameter called “enable,” now added to the “insertpipestage” directive, lets you specify whether or not an associated hierarchical directive is enabled or disabled.

In addition, new LogiCORE support is now available for Accumulator, Multiply Accumulator and Multiply Adder.

Xilinx IP Updates

Name of IP: ISE IP Update 10.1.3

Type of IP: All

Targeted application: Xilinx develops IP cores and partners with third-party IP providers to decrease customer time-to-market. The powerful combination of Xilinx FPGAs with IP cores provides functionality and performance similar to ASSPs, but with flexibility not possible with ASSPs.

Latest version number: 10.1.3

Date of latest release: September 2008

Access the latest version:

www.xilinx.com/download

Informational URL:

www.xilinx.com/ipcenter/coregen/updates_101_ip3.htm

Release Notes: www.xilinx.com/support/documentation/user_guides/xtp025.pdf

Installation Instructions:

www.xilinx.com/ipcenter/coregen/ip_update_install_instructions.htm

Listing of all IP in this release:

www.xilinx.com/ipcenter/coregen/101_3_datasheets.htm

Revision highlights: Xilinx intellectual property (IP) cores, including LogiCORE IP cores, are delivered through software updates available from the Xilinx Download Center. The latest versions of IP products have been tested and are delivered with the current IP releases.

In addition to quality improvements, Service Pack 3 ISE IP Update 10.1.3 provides new features, functionality and examples for many of the Xilinx LogiCORE IP cores. It includes optimized uplink and downlink baseband modules that contain complex functionality, including rate matching/dematching, assembly/reassembly, turbo codecs and CRC. These high-quality cores are production ready, enabling users to realize fast and efficient baseband designs in Xilinx FPGAs, while significantly reducing development effort. These cores are scalable from femto- to macrocell applications, and are designed to meet 3GPP LTE wireless specifications for both FDD and TDD variants.

Learn more about the 3GPP LTE UL Channel Decoder at www.xilinx.com/products/ipcenter/DO-DI-CHDEC-LTE.htm. Details of the 3GPP LTE DL Channel Encoder are available at <http://www.xilinx.com/products/ipcenter/DO-DI-CHENC-LTE.htm>.

Enhancements to existing IP cores:

A new low-power implementation option has been added to the Block Memory Generator. Also in this release are updates to other popular CORE Generator IP cores, including the Memory Interface Generator (MIG); PCI 32, PCI 64 and PCI-X; Content Addressable Memory (CAM), and FFT v6.0.

A number of cores now support the Virtex-5 TXT family of FPGAs. Among them are the Block Memory Generator, FIFO Generator, CAM, Virtex-5 RocketIO GTX Transceiver Wizard, Endpoint Block Plus Wrapper for PCI Express, 10 Gigabit Ethernet MAC, Virtex-5 Ethernet MAC Wrapper, XAUI, SPI-4.2 and FFT. 🌈