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Avalon Bulks up IP Offerings for Optical Transport

IP vendor Avalon Microelectronics (St. John's, Newfoundland, Canada) recently expanded its intellectual-property lineup and now offers several cores for 40G, 10G and 2.5G Sonet/SDH and OTN optical transport.

Avalon's IP is mainly targeted at FPGA implementations. "The number of IP blocks we offer is hard to quantify, because our IP is arranged around application spaces and needs," said CEO Wally Haas, who founded Avalon in 2004 after a stint at AMCC. "We have a full suite of IP for the 40G, 10G and 2.5G data rates."

The company offers framers, concatenated and channelized path processors, and packet-over-Sonet mappers to support SDH/Sonet applications. Its flagship product is an enhanced forward-error-correction (EFEC) core for 10G and 40G. "We have a core IP library that is tested and validated, and we have hardware platforms that we use to test these cores," said Haas. "We customize these cores to create solutions for our customers."

For example, he said, "a 10G transponder would take a 10G client SDH or 10GE, and that can be transported over 10G OTN with FEC or EFEC cores. That's one application where we combine a few pieces of IP to create a full product or to create a larger core, depending on our customer's needs."

Haas said the company's modular approach allows Avalon to take

that same IP and configure it for a 40G muxponder solution—create four 10G clients in Sonet or SDH, and aggregate those up to 40G with FEC or EFEC.

Avalon initially made its mark offering an SFI-5 core. "What that does is make FPGA- or serdes-based products compliant to the SFI-5 standard, which they normally aren't," said Haas. The company holds three patents on that IP, which Haas calls its "skew finder technology." This patented technology uses a reference transceiver to relate skew by any transmitting serdes to any other transmitting serdes, he said. "We've deployed that in Virtex®-II Pro, Virtex®-4 and Virtex®-5 FPGAs."

The SFI-5 core is a soft core that users download in conjunction with control software. The company also offers netlisted and RTL versions of its IP, as well as single-project, single-site and multiproject, multisite licensing.

Haas said that Avalon takes IP protection very seriously and has a full-time patent writer on staff. The company has thus far filed seven patents, he said. According to Haas, most IP licensing deals also require a small—usually very small—amount of integration services from Avalon. "We consider ourselves a product company," said Haas.

For more information, visit <http://www.avalonmicro.ca/about/mission/>.

Synopsys Prototyping Board Packs Virtex-5 LX330T; FXT Version Due

The latest ASIC prototyping board from Synplicity, newly acquired by Synopsys Inc. (Mountain View, Calif.), features the Virtex®-5 LX330T FPGA, along with 1 Gbyte of on-board DDR2 memory. "We've laid it out in a way that later in the year, we can also offer a derivative of this system with a Virtex®-5 FXT device. And we already have [customer] interest in that," said Juergen Jaeger, director of HAPS product marketing in the Synplicity business group at Synopsys.

Released at the Design Automation Conference in Anaheim, Calif., in June, the High-performance ASIC Prototyping System (HAPS) 51T "provides users with a platform for all kinds of applications that incorporate high-speed interfaces," Jaeger said. Along with the DDR2 memory, the board also includes 2M x 36-bit synchronous SRAM and 32M x 16-bit flash PROM.

Jaeger said Synplicity started shipping the HAPS-51T board in mid-May. "We got the first orders for the boards before we even started the design. We see a lot of interest in this board, especially

as an add-on to our FPGA motherboards to add a high-speed interface to the system," he said.

This is the first board to go beyond the company's HAPSTrack connectors, Jaeger said. "In order to leverage the 24 RocketIO™ GTP channels in the Virtex-5 LX330T, we made a new connector, which we call the MGb [multigigabit] HAPS connector. Each MGb brings eight RocketIO channels out from the FPGA directly."

Designers can plug several daughterboards directly into the HAPS-51T, Jaeger said, including USB, Ethernet, PCI Express and video processing. They can also plug riser cards into the system to add more sockets.

The system features three Vcco regions, which designers can individually set to 3.3, 2.5 or 1.8 volts. Designers can program the board configuration via JTAG, on-board flash PROM or SelectMAP, or they can buy an optional CompactFlash card from Synopsys.

For more details on the product, including gate counts, go to www.synopsys.com.