



## Xilinx Education Services Newsletter, December 2006

### Featured NewsFlash

On 15 December the Education Services section of the Xilinx Web site underwent a facelift. The revised Education Services pages now offer a more streamlined, course-centric approach to delivering training options to Xilinx customers across the globe. Visitors to the Xilinx site can expect.

- Fewer clicks due to a flatter site structure that brings the most important information to the top
- Direct access to authorized training provider contact details
- Easy navigation to curriculum paths
- Quick overview of all training-related content offered on Xilinx.com including Webcasts and events such as public forums and demonstrations.

[Visit the new Education Services Section of Xilinx.com Now!](#)

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### Instructor-Led Training News

Xilinx Education Services would like to announce the new updates for our instructor-led courses. Courses have been adapted to include the latest Xilinx FPGA architectures and labs that utilize the latest software flows.

#### [Designing with PlanAhead v8.2](#)

A new version of Designing with PlanAhead™ v8.2 is now available. All classes use the new version.

##### What's New in v8.2:

- All labs have been updated to use PlanAhead 8.2.1 and ISE™ 8.2.
- GUI enhancements, particularly regarding adjusting the sizes of View windows.
- Explore Ahead is now the primary interface between PlanAhead and ISE.
- The incremental design flow material has been removed from the course. This content will reappear in the v9.1 update.

[Visit here](#) for more information on PlanAhead

#### [Designing with Ethernet MAC Controllers v8.2](#)

A new course offering is now available from Xilinx Education Services called Designing with Ethernet MAC Controllers v8.2. This course is a comprehensive introduction to the EMAC solution that Xilinx has to offer.

##### Software

- This course uses ISE 8.2 SP1, IP Update #1, EDK 8.2 software

##### Hardware

- Virtex-4 is the target device and we use ML403 board
- Two out of six labs use ML403 board

##### Course Design

- This course is a 2-day course
- What is covered?
- Ethernet Basics, MAC Frames

- MAC Interfaces including MII, GMII, RMII, SGMII, XGMII, and XAUI
- Auto negotiations, VLAN, and Jumbo frames
- Hard TEMAC, EMAC, GEMAC, 10 GE MAC
- Simulation and analysis of various kinds of MAC frames
- Standalone and processor-interface based EMAC solutions

[Visit here](#) for more information on EMAC

### **Designing with Multi-Gigabit Serial I/O v8.2 — Under Development**

A new version of the Designing with Multi-Gigabit Serial I/O v8.2 is under development. The scheduled release date is January 2007.

#### **What's New in v8.2:**

- Virtex-5 LXT is the target device family.
- ISE v8.2i with the IP3 update is used for all labs

### **Live e-Learning News**

Live e-Learning (LEL) allows us to convert classroom based instructor-led courses into a series of lectures and labs that are delivered by a live Xilinx instructor online. As a student, you can attend from the comfort of your desk and obtain the same knowledge taught during the traditional course. Live e-Learning works by scheduling course modules sequentially over a one to two-week period, depending upon the subject. Shortly after registering for a Live e-learning class, you will receive an FTP address for your course workbook allowing you to follow along with the material delivered by the live instructor through a Centra interface and a phone. How do we conduct labs? Toolwire technology makes it possible for you to perform Xilinx labs in a virtual environment and receive hands-on experience with the Xilinx software tools while remaining online.

Sound interesting? Redeem your Training Credits for several Live e-Learnings that are upcoming in 2006! View the complete schedule and sign up today by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Live e-Learning" to register for any offering.

#### **Fundamentals of FPGA Design v8.2 LEL**

This course covers the ISE 8 software features, such as the Architecture Wizard and the Pin and Area Constraint Editor (PACE). Other topics include design planning, implementation options, and global timing constraints.

This course is scheduled to begin on January 8, 2007 with sessions taking place on January 8th, 9th, and 12th. The Monday, Tuesday and Friday sessions will run 9-11AM PDT.

#### **Designing for Performance v8.2 LEL**

This Live e-Learning teaches you how to fit your design into a smaller FPGA or a lower speed grade to reduce system costs. By mastering the tools and the design methodologies presented in this course, you can shorten your development time and lower development costs.

This course is scheduled to begin on January 15, 2007 with sessions taking place on January 15th, 16th, 19th, 22nd, 23rd, and 26th. The Monday, Tuesday and Friday sessions will run 9-11AM PDT.

#### **Advanced FPGA Implementation v8 LEL**

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE tool suite and includes labs that provide hands-on experience. Scheduled over a two-week period, this course comprises a series of six two-hour sessions (with sessions running on Monday, Tuesday, and Friday of each week).

This course is scheduled to begin on January 29, 2007 with sessions taking place on January 29th, 30th, February 2nd, 5th, 6th, and 9th. The Monday, Tuesday and Friday sessions will run 9-11AM PDT.

#### **Looking for a Particular Xilinx Course in a Live e-Learning Format?**

*Are you looking for a particular Xilinx course in a Live e-Learning format? If a course you desire to take is not listed above, contact a Xilinx registrar at: [registrar@xilinx.com](mailto:registrar@xilinx.com) or 1-(877) XLX-CLASS.*

### **Recorded e-Learning News**

Xilinx Education Services offers a series of Recorded e-Learnings that can help you get up to speed quickly on the powerful

capabilities of Xilinx technology. These recordings are currently available at no charge, over the internet anytime day or night, and can be taken anywhere there is an internet connection. View the complete set of modules available by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Recorded e-Learning" to register for any offering.

### **System Generator Getting Started Training REL**

A new recorded e-learning System Generator Getting Started Training REL is now available. System Generator enables the use of Simulink for designing Xilinx FPGAs. This recorded e-learning will provide a jump start for those who want to evaluate this flow.

**After completing this training, you will be able to:**

- Create a DSP design that includes memories and control using Simulink and implement that design into a Xilinx FPGA
- Design highly efficient FIR filters for the Xilinx device architectures
- Define fixed-point numeric precision abstractly using the Xilinx DSP blockset

**There are seven individual modules:**

- Module 1 - Introduction
- Module 2 - Design Creation Basics
- Module 3 - Signal Routing
- Module 4 - Implementing System Control
- Module 5 - Multi-Rate Systems
- Module 6 - Memories
- Module 7 - Filter Design

[Visit here](#) for more information System Generator

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