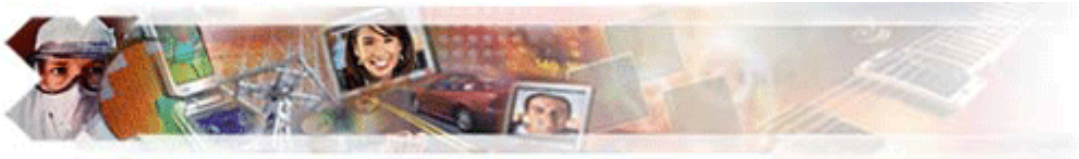

Xilinx Education Services Newsletter – June 2007

Xilinx Education Services: The source for Xilinx education

Brought to you by Xilinx, the leader in Programmable Logic technology — Xilinx Education Services is the source for Xilinx education. Our programs:

- Provide targeted, high-quality education products and services designed by experts in programmable logic design and delivered by Xilinx-qualified trainers
- Offer targeted courses at all levels of programmable logic design
- Create an engaging learning environment by blending lecture, hands-on labs, interactive discussions, tips, and best practices
- Deliver training when and where you need it by leveraging our global network of 32 Authorized Training Providers (ATP) and online learning systems. Classes are offered at over 110 locations around the world

In This Issue

Instructor-Led Training News

Instructor-led training offers the advantage of face-to-face learning from our team of expert trainers with first-hand knowledge of Programmable Logic products and technology. Their goal is to accelerate your success by enabling you to get the most out of the powerful capabilities of Xilinx products and technology. By attending an instructor-led course, you will become more competent and confident in the use of Programmable Logic Devices. These classes can be brought to you on-site, or you can attend them at over 110 public locations around the world.

To register, or learn more about all of the courses and curriculum paths Xilinx offers, visit www.xilinx.com/education.

The following classes will use the new ISE™ v9.1 software that is now available. All classes will use the new course workbook and design tools.

Advanced FPGA Implementation v9.1 — Register for a class near you

Attending the Advanced FPGA Implementation course will enable you to tackle the most sophisticated aspects of the ISE 9.1i tool suite and Xilinx hardware. After completing this training, you will have the necessary skills to:

- Create and edit timing constraints in the UCF file
- Utilize Tcl-based scripting to implement a design
- Analyze I/O interface timing and implement timing constraints and design modifications to meet System and Source Synchronous I/O interface timing
- and much more

Course Design

This is a 2-day course covering the following topics: Synplicity's Synplify and the Xilinx XST tools.

New in this course:

- Tcl Scripting replaces Command Line Implementation
- Advanced I/O Timing replaces Creating Your Own RPM
- SmartCompile™ Design Preservation Techniques replaces Divide and Conquer design techniques
- Revised Floorplanning Effective Layout

Software

This course uses ISE 9.1i SP2, Synplicity Synplify Pro 8.8, and Precision 2006.a.

Designing for Performance v9.1 — Register for a class near you

Attending the Designing for Performance class will help you create more efficient designs. By mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs. After completing this training, you will have the necessary skills to:

- Increase performance by duplicating registers and pipelining
- Write HDL code by using a style that is optimal for targeting Xilinx devices
- Describe different synthesis options and how they can improve performance
- Create and integrate cores into your design flow by using the CORE Generator™ software system
- Run behavioral simulation on an FPGA design that contains cores
- Pinpoint design bottlenecks by using the Timing Analyzer reports
- Apply advanced timing constraints to meet your performance goals
- Use advanced implementation options to increase design performance
- and much more

Course Design

This 2-day course will help you fit your design into a smaller FPGA or a lower speed grade for reducing system costs.

New in this course:

- The CORE Generator™ lab does not include the use of the Simulator or BRAM
- The Synthesis labs now support Synplicity v8.8 and Precision v2006a
- The Timing Closure Flow Diagram has been updated to use Xplorer and MPPR
- The Timing Analyzer, Constraints Editor, and Floorplan Editor are different from the previous version
- The Advanced Implementation Options lab requires three iterations of the design with the Implementation tools

Software

This course uses ISE 9.1i, Synplicity Synplify Pro, and Mentor Graphics Precision RTL.

Designing with PlanAhead v9.1 — Register for a class near you

Attending the Designing with PlanAhead™ course will teach you how to use Xilinx hierarchical floorplanning in order to improve your programmable logic design flow. The result is higher performance designs and a significant reduction in the number and the length of design iterations. After completing this training, you will have the necessary skills to:

- Analyze design statistics, connectivity, timing, and placement results
- Run the Design Rule Checker (DRC) and Weighted Average Simultaneous Switching Output (WASSO) analysis
- Partition and floorplan designs
- Run ExploreAhead to try multiple implementation strategies
- Import and analyze the implementation results to improve the floorplan
- Floorplan to improve performance and consistency
- Use block-based design and create and reuse module-level IP
- Use PinAhead to import, define, and assign I/O pins for the design
- and much more

Course Design

This 2-day course covers the following topics: synthesis and project tips, improving performance, experimenting with implementation options, incremental methodology, block-based IP design, and I/O pin assignment.

New in this course:

- All materials and labs are based on the PlanAhead™ v9.1.2 software
- The "Updating the Design Netlist" module has been removed. The lab exercise has been split up and incorporated into the "Getting Started" and "Block-Based Design" labs
- A new pin assignment module and lab have been added to highlight the new PinAhead environment
- The final "Floorplanning Strategies" module has been enhanced with some case studies of actual Virtex™-5 designs (from the Technical Sales Conference presentation)

Software

This course uses ISE 9.1i.

Fundamentals of FPGA Design v9.1 — Register for a class near you

Attending the Fundamentals of FPGA Design course will teach you how to use the ISE software tools to implement a design and gain a firm understanding of the Xilinx FPGA architectures. After completing this comprehensive training, you will have

the necessary skills to:

- Use Xilinx Project Navigator to implement an FPGA design
- Assign pin locations with the Floorplan Editor tool
- Create DCM instantiations with the Architecture Wizard
- Read reports to determine whether design goals were met
- Use the Constraints Editor to enter basic global timing constraints
- Locate and modify implementation options
- and much more

Course Design
In this 1-day course, you will use ISE software tools to implement a design and gain a firm understanding of the Xilinx FPGA architecture.

New in this course:

- Three recorded e-Learning modules are now required:
  - Basic FPGA Architecture: Slice and I/O Resources
  - Basic FPGA Architecture: Memory and Clocking Resources
  - Basic FPGA Architecture: Architecture Wizard and Floorplan Editor
- Timing Analyzer, Floorplan Editor, and Constraints Editor have a different look and functionality
- Floorplan Editor has an additional lab
- Implementation Options module now introduces the Xplorer function in more detail

Software
This course uses ISE 9.1i.

ISE Design Entry v9.1 — Register for a class near you
Attending the ISE Design Entry course will teach you about Xilinx project structure, process windows, various ISE software design flows, and Xilinx Synthesis Technology (XST). After completing this training, you will be able to:

- Create a new Project Navigator project in the ISE software
- List the design flows available in the ISE software
- Access and modify XST synthesis options
- Create a schematic design by using the Engineering Capture System (ECS) schematic entry tool
- Create a symbolic state machine by using the StateCAD tool
- Create testbenches and simulate a design by using the ISE Simulator
- and much more

Course Design
In this 1-day course, you will learn about project structures, process windows, various ISE software design flows, and Xilinx Synthesis Technology (XST).

New in this course:

- All materials and labs have been updated to support ISE 9.1
- GUI-related updates

Software
This course uses ISE 9.1i.

Live e-Learning News

Live e-Learning combines the excellence of our traditional instructor-led training with the benefits of learning from the comfort of your own desk. Live e-Learning saves time and money by delivering a series of lectures and labs online over the course of a one-to-two-week period, without sacrificing the skills development that only comes from directly working with an instructor, development tools, and demo boards. Live e-Learning is available in North America only.

Sound interesting? Redeem your Training Credits for an upcoming Live e-Learning class today by accessing them at https://xilinx.onsaba.net/xilinx. Select “Live e-Learning” to register for any offering.

The following Live e-Learning courses have been updated using v9.1 course materials.

Fundamentals of FPGA Design LEL:
This course covers the ISE 9.1i software features, such as the Architecture Wizard and the Floorplan Editor. Other topics include design planning, implementation options, and global timing constraints.
Please see the description in the Instructor-Led Training news above for more information on Fundamentals of FPGA Design.

Designing for Performance LEL:
This Live e-Learning teaches you how to fit your design into a smaller FPGA or a lower speed grade to reduce system costs. By mastering the tools and the design methodologies presented in this course, you can shorten your development time and lower development costs.
Please see the description in the Instructor-Led Training news above for more information on Designing for Performance.

Advanced FPGA Implementation LEL:
Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE tool suite and includes labs that provide hands-on experience. Scheduled over a two-week period, this course comprises a series of six two-hour sessions (with sessions running on Monday, Tuesday, and Friday of each week).
Please see the description in the Instructor-Led Training news above for more information on Advanced FPGA Implementation.

For a complete Live e-Learning course listing and to find out class dates, contact a Xilinx registrar at registrar@xilinx.com or 1-(877) XLX-CLASS.

Recorded e-Learning News

Recorded e-Learning will help you get up to speed quickly on the powerful capabilities of Xilinx technology. As a prerequisite to many of the Xilinx Curriculum paths, these courses ensure that you can take full advantage of the powerful Instructor-Led training or Live e-Learning courses. These recordings are available at no charge, over the Internet, anytime, day or night. Recorded e-Learning is offered in English only.
The following new Recorded e-Learnings are now available:

Architecture Wizard and Floorplanner Editor
After completing this training, you will be able to:
- List at least two uses of the Architecture Wizard
- Identify two features of the Floorplan Editor
- Create quality pin assignments for Xilinx FPGAs

Memory and Clocking Resources
After completing this training, you will be able to:
- List their dedicated resources
- List some of the differences between Spartan-3 and Virtex-4 FPGAs

Slice and I/O Resources
After completing this training, you will be able to:
- Describe the basic Slice resources available in Virtex-4 FPGAs
- Identify the basic I/O resources available in Virtex-4 FPGAs

Interactive Recorded e-Learning News

Xilinx Education Services offers the following self-paced interactive recorded e-Learning courses. These courses offer the most flexibility with optional audio and textual narration and interactive exercises to engage your participation and enhance your understanding of the presented material.

Fundamentals of FPGA Design
The Fundamentals of FPGA Design interactive recorded e-Learning course delivers high-value training at your own pace with the emphasis of keeping your work schedule and priorities intact. This course comprises seven recorded modules and five hands-on labs covering the ISE v9.1 software features, such as the Architecture Wizard and the Floorplan Editor.

Global Timing Constraints

This module is about 15 minutes in duration. After completing this training, you will be able to apply global trimming constraints to a simple synchronous design and use the Constraints Editor to specify global timing constraints.

View a list of available interactive recorded e-Learning and start learning today.

On-Demand Webcasts

Webcasts are 60 minutes, were recorded live and now made available on-demand. If the webcast you are looking for is not shown, the on-demand webcast has not yet been posted. Please check again in 24 hours. All on-demand webcasts require registration.

View a list of all available On-Demand Webcasts

Demos-on-Demand

Xilinx offers a wide variety of product demos and product specific presentations.

View all product demos and presentations here.