



Xilinx Education Services Newsletter – September 2007

Xilinx Education Services: The Source for Xilinx Education

Brought to you by Xilinx, the leader in Programmable Logic technology — Xilinx Education Services is the source for Xilinx education.

Our programs:

- Provide targeted, high-quality education products and services that are designed by experts in programmable logic design and delivered by qualified trainers
- Offer targeted courses at all levels of Programmable Logic design
- Create an engaging learning environment by blending lecture, hands-on labs, interactive discussions, tips, and best practices
- Deliver training when and where you need it by leveraging our global network of 22 Authorized Training Providers (ATP) and online learning systems

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Authorized Training Provider (ATP)

The Xilinx Authorized Training Provider Network delivers consistent, high-quality Xilinx training worldwide. To qualify as an ATP, training providers must be:

- Training experts and providers of Xilinx training products, with the ability to offer local classes in the native language
- Qualified by Xilinx to teach our courses to a high level of quality and customer satisfaction
- Skilled in guiding customers in the use of curriculum paths and training plans to ensure they get the most from their learning experience
- Flexible, using an open approach to address customer training requirements
- Paid in local currency or with training credits available through the [Xilinx Productivity Advantage](#) program

Instructor-Led Training News

Instructor-led training offers the advantage of face-to-face learning from our team of expert trainers with first-hand knowledge of Programmable Logic products and technology. Their goal is to accelerate your success by enabling you to get the most out of the powerful capabilities of Xilinx products and technology. By attending an instructor-led course, you will become more competent and confident in the use of Programmable Logic devices. These classes can be brought to you on-site, or you can attend them at over 110 public locations around the world.

To register, or learn more about all of the courses and curriculum paths Xilinx offers, visit www.xilinx.com/education.

The following classes will use the new ISE™ v9.1 software that is now available. All classes will use the new course workbook and design tools.

[Fundamentals of CPLD Design v9.1](#) — Register for a class near you

This comprehensive course provides you with an introduction to designing with Xilinx CPLDs by using the ISE series software tools. After completing this training, you will have the necessary skills to:

- Describe what products Xilinx offers and where the CoolRunner™-II CPLD fits into this offering
- Identify the basic architectural resources of the CoolRunner-II CPLD
- Describe the CPLD tool flow: design entry, synthesis, implementation, and programming
- Specify global timing constraints and pin assignments
- Access and implement basic and advanced CPLD software options via the ISE software

- And much more

Course Design

This is a 1-day course that balances lecture modules and practical hands-on labs.

New in this course:

- Updated software to ISE v9.1 SP3
- The first lab includes an exercise to download the design to the CoolRunner-II X-board

Software

This course uses ISE 9.1i SP3

[DSP Design Using System Generator v9.1](#) — Register for a class near you

Attending this course will allow you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. After completing this training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Recognize that hardware may be required for high-level abstraction
- Identify the high-level blocks available for filter design
- Perform hardware-in-the-loop and improve productivity
- Design a multiple clock-based System Generator system
- Employ various design techniques for improving system performance
- And much more

Course Design

Through hands-on exercises in this 2-day course, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

New in this course:

- Updated to ISE v9.1 software
- Addition of labs for Spartan™-3E Starter Boards

Software

This course uses ISE 9.1i SP2 + IP Update 1, Xilinx System Generator 9.1, and the MathWorks MATLAB® with Simulink® R2006b.

[Embedded Systems Development v9.1](#) — Register for a class near you

Attending the *Embedded Systems Development* course will bring experienced FPGA designers up to speed on developing embedded systems using the Embedded Development Kit (EDK). After completing this training, you will have the necessary skills to:

- Effectively develop, debug, and simulate an embedded system
- Identify tools used in the Embedded Development Kit
- Use the hardware, software, and debugging flows provided in the Embedded Development Kit
- Identify IP included in the Embedded Development Kit and where to get additional information
- Identify the hardware and software simulation environments
- Integrate custom IP into the Embedded Development Kit
- And much more

Course Design

This 2-day course covers the basic features and capabilities of the Xilinx MicroBlaze™ soft processor and the PowerPC® processor.

New in this course:

- Updated to ISE v9.1 software

Software

This course uses ISE 9.1 SP3, Mentor Graphics ModelSim PE 6.2f, and EDK 9.1 SP1.

[Advanced Features and Techniques of Embedded Systems Development v9.1](#) — Register for a class near you

Attending the *Advanced Features and Techniques of Embedded Systems Development* course will provide embedded systems developers with the necessary skills to develop complex embedded systems and enable them to improve their designs by using the tools available in the Embedded Development Kit (EDK). After completing this comprehensive training, you will have the necessary skills to:

- Assemble and architect a complete embedded system
- Identify the steps involved in integrating user IP in a system
- Use a Board Support Package (BSP) to target multiple operating systems
- Apply advanced debugging techniques
- Design a flash memory-based system and boot load from flash
- Apply various techniques to improve performance
- And much more

Course Design

This 2-day course builds on the skills gained in the *Embedded Systems Development* course.

New in this course:

- Updated to ISE v9.1 software

Software

This course uses ISE 9.1 SP3, Mentor Graphics ModelSim PE 6.2f, and EDK 9.1 SP1.

[Designing with Multi-Gigabit Serial I/O v9.1](#) — Register for a class near you

Attending the *Designing with Multi-Gigabit Serial I/O* course will teach you how to employ RocketIO™ GTP transceivers in your Virtex™-5 LXT FPGA design. After completing this training, you will be able to:

- Describe and utilize the ports and attributes of the RocketIO multi-gigabit transceiver (GTP) in the Virtex-5 LXT FPGA
- Effectively use the following features of the GTP:
 - Comma detection, CRC, clock correction, and channel bonding
 - 8B/10B encoding/decoding, programmable termination, and pre emphasis
- Use the GTP Wizard to instantiate GTP primitives in a design
- Access appropriate reference material for board design issues
- Power supply, oscillators, and trace design
- And much more

Course Design

Additional highlighted topics in this 2-day course include use of the Architecture Wizard and synthesis and implementation considerations.

New in this course:

- The target device family is Virtex-5 LXT
- The software has been updated to ISE v9.1 + SP2 + IP1 + ModelSim 6.2f
- The Aurora Reference Design lecture and lab have been removed
- The labs are based on the example design that is created by the GTP Wizard

Software

This course uses ISE 9.1i SP2 + IP Update 1 and Mentor Graphics ModelSim PE 6.2f.

[Introduction to Verilog v9.1](#) — Register for a class near you

This comprehensive course is a thorough introduction to the Verilog language. After completing this training, you will be able to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Run a timing simulation by using Xilinx Simprim libraries
- Create and manage designs by using the ISE software design environment
- And much more

Course Design:

In this 3-day course you will learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization.

New in this Course:

- Fixed errata information
- Added introductory File I/O presentation and lab:
 - Advanced Verilog Testbenches Presentation module
 - Lab 9: Using Verilog File I/O lab

Software:

This course uses ISE 9.1i SP2 + IP Update 1

Live e-Learning News

Live e-Learning combines the excellence of our traditional instructor-led training with the benefits of learning from the comfort of your own desk. Live e-Learning saves time and money by delivering a series of lectures and labs online over the course of a one- to two-week period, without sacrificing the skills development that only comes from directly working with an instructor, development tools, and demo boards. Live e-Learning is available in North America only.

Sound interesting? Redeem your Training Credits for an upcoming Live e-Learning class today by accessing them at <https://xilinx.onsaba.net/Saba/Web/Main>. Select “Live e-Learning” to register for any offering.

The following Live e-Learning courses have been updated using v9.1 course materials.

Fundamentals of FPGA Design LEL:

This course covers the ISE 9.1i software features, such as the Architecture Wizard and the Floorplan Editor. Other topics include design planning, implementation options, and global timing constraints.

Designing for Performance LEL:

This Live e-Learning teaches you how to fit your design into a smaller FPGA or a lower speed grade to reduce system costs. By mastering the tools and the design methodologies presented in this course, you can shorten your development time and lower development costs.

Advanced FPGA Implementation LEL:

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE tool suite and includes labs that provide hands-on experience.

For a complete Live e-Learning course listing and to find out class dates, contact a Xilinx registrar at registrar@xilinx.com or 1-(877) XLX-CLASS.

Recorded e-Learning News

Recorded e-Learning will help you get up to speed quickly on the powerful capabilities of Xilinx technology. As a prerequisite to many of the Xilinx Curriculum paths, these courses ensure that you can take full advantage of the powerful Instructor-Led training or Live e-Learning courses. These recordings are available at no charge, over the Internet, anytime, day or night.

Recorded e-Learning is offered in English only.

The following new Recorded e-Learning is now available:

[ChipScope Pro Software](#)

After completing this training, you will be able to:

- Describe the value of the ChipScope Pro analyzer
- Describe how the ChipScope Pro analyzer works
- List what cores are available
- Use the CORE Generator™ and Core Inserter software
- Plan for debug, as well as debug, with the ChipScope Pro analyzer

Interactive Recorded e-Learning News

Xilinx Education Services offers the following self-paced interactive recorded e-Learning courses. These courses offer the most flexibility with optional audio and textual narration and interactive exercises to engage your participation and enhance your understanding of the presented material.

[Fundamentals of FPGA Design](#)

The Fundamentals of FPGA Design interactive Recorded e-Learning (iREL) course delivers high-value training at your own pace with the emphasis of keeping your work schedule and priorities intact. This course comprises seven recorded modules and five hands-on labs covering the ISE v9.1 software features, such as the Architecture Wizard and the Floorplan Editor.

[Global Timing Constraints](#)

This module is about 15 minutes in duration. After completing this training, you will be able to apply global timing constraints to a simple synchronous design and use the Constraints Editor to specify global timing constraints.

[View a list of available interactive recorded e-Learning and start learning today.](#)

Additional Xilinx Product Information

If you would like to have the latest product information on Virtex, Spartan devices, CPLDs, Design tips, Development tools, and more, go to http://www.xilinx.com/push_email/newsletter/index.htm

On-Demand Webcasts

Xilinx on-demand Webcasts are recorded live and then made available on-demand. These broadcasts feature technical presentations, product demonstrations, and question-and-answer sessions presented by our expert silicon and software people on Xilinx technology, the industry, or both. For more information go to http://www.xilinx.com/events/webcasts_od.htm

Demos-on-Demand

Xilinx product demos are presented by our expert silicon and software people on detailed, video-based information in the areas of FPGA, CPLD, DSP, Embedded Design, and the Design Tools. For more information go to <http://www.demosondemand.com/clients/xilinx/001/page/index.asp>

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