



Featured Tidbits

[Designing with the Virtex-5 LX FPGA](#)

Classes will be offered as both Instructor-Led (ILT) in San Jose, CA, and as a Live e-Learning (LEL). The first scheduled ILT course is on July 6th, 2006. The first LEL is scheduled for June 20th, 2006, with 2 hour sessions taking place on June 20th and 22nd from 9-11 PDT.

Featured Webcasts

[Introducing Virtex-5 FPGA - The Ultimate System Integration Platform](#)

Learn how the latest Virtex™-5 FPGAs address design challenges in today's systems.

Learn how to meet higher performance and lower power design requirements.

Learn how to better integrate system functions with the latest FPGAs

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Instructor-Led Training News

Xilinx Education Services would like to announce the new updates for our instructor-led courses. Courses have been adapted to include the latest Xilinx FPGA architectures and labs that utilize the latest software flows.

Designing with the Virtex-5 LX FPGA

For those interested in learning how to effectively utilize Virtex-5 FPGA architectural resources, Xilinx Education Services announces a new course available. Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device. Note that the initial course material covers the Virtex-5 LX FPGA platform only. Future revisions will include additional platforms as they become available.

[Learn More and Register](#)

Classes will be offered as both Instructor-Led (ILT) in San Jose, CA, and as a Live e-Learning (LEL). The first scheduled ILT course is on July 6th, 2006. The first LEL is scheduled for June 20th, 2006, with 2 hour sessions taking place on June 20th and 22nd from 9-11 PDT.

Advanced VHDL (v8.1)

A revision has been made to the [Advanced VHDL](#) course.

What's New in v8.1?

- This is the first major revision since the release of ISE™ v6.1.
- Was updated to use ModelSim PE 6.0c in September, 2005.
- Labs and presentations updated to use ISE 8.1 (no service packs) and ModelSim PE 6.0c
- Virtex-4 is now the lead target device
- Errata Corrections
- Slide reduction
- Increased number of pen & paper exercises performed by students in "Knowledge Checks"
- Solidify and test knowledge prior to labs
- Add to the student's expertise and knowledge of advanced VHDL concepts
- Many of the exercises ask the students to write re-usable functions or procedures that are commonly needed for testing and synthesis
- Major rework of labs to reduce lab time and concentrate time and effort on the most prudent VHDL learning points
- Lab documents have more explanation of required coding steps. Includes pointing them to the correct location in the file and hints for writing the code. Additionally, we have added more information to help students identify in the simulation if the design is working correctly. This is in addition to providing/creating self-testing test benches.

Designing with PlanAhead (v8.1)

A revision has been made to the [Designing with PlanAhead](#) course. All courses with a start date on or after March 2, 2006 will use the new materials.

What's New in v8.1?

- Updated content to use PlanAhead™ (v8.1i) and ISE (v8.1i)
- New ExploreAhead™ feature allows users to setup and run multiple implementations using different software options

Embedded Systems Design (v8.1)

A revision has been made to the [Embedded Systems Design](#) course.

What's New in v8.1?

- Labs and presentations updated to use ISE (v8.1) SP1 and EDK (v8.1)
- Modified four labs, now targeting hardware board
- New lab covering SDK-based Debugging

Advanced Features and Techniques of Embedded Systems Development (v8.1)

A revision has been made to the [Advanced Features and Techniques of Embedded Systems Development](#) course.

What's New in v8.1?

- Labs and presentations updated to use ISE (v8.1) SP1 and EDK (v8.1)
- Lab covering SDK-based Profiling

Additionally Look for ISE (v8.2i) Updates to the Following Courses:

- [Fundamentals of FPGA Design](#) (v8.2)
- [Designing for Performance](#) (v8.2)

For more information, or to enroll in a Xilinx course, browse to: <https://xilinx.onsaba.net/xilinx>

Live e-Learning News

Live e-Learning allows us to convert classroom based instructor-led courses into a series of lectures and labs that are delivered by a live Xilinx instructor online. As a student, you can attend from the comfort of your desk and obtain the same knowledge taught during the traditional course. Live e-Learning works by scheduling course modules sequentially over a one to two-week period, depending upon the subject. Shortly after registering for a Live e-learning class, you will receive an FTP address for your course workbook allowing you to follow along with the material delivered by the live instructor through a Central interface and a phone. How do we conduct labs? Toolwire technology makes it possible for you to perform Xilinx labs in a virtual environment and receive hands-on experience with the Xilinx software tools while remaining online.

Sound interesting? Redeem your Training Credits for several Live e-Learnings that are upcoming in 2006! View the complete schedule and sign up today by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Live e-Learning" to register for any offering.

Designing with the Virtex-5 LX FPGA LEL

For those interested in learning how to effectively utilize Virtex-5 LX FPGA architectural resources, Xilinx Education Services announces a new course available. Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device. Note that the initial course material covers the Virtex-5 LX FPGA platform only. Future revisions will include additional platforms as they become available. This course is scheduled to begin on:

- 6/20/06, with sessions taking place on June 20th, 22nd.
 - 8/1/06, with sessions taking place on August 1st, 3rd.
- The Tuesday, Thursday sessions will run from 9-11 AM PDT.

Advanced FPGA Implementation LEL

This Live e-Learning details the most sophisticated aspects of the ISE tool suite with labs providing hands-on experience. This course requires *Fundamentals of FPGA Design* and *Designing for Performance* as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended, as is at least six months of design experience with Xilinx tools and FPGAs. This course is scheduled to begin on:

- 7/10/06, with sessions taking place on July 10th, 11th, 14th, 17th, 18th, 21st.
- The Monday, Tuesday, and Friday sessions will run from 9-11 AM PDT.

Introduction to Verilog LEL

This comprehensive 9-session course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations. This course is scheduled to begin on:

- 8/7/06, with sessions taking place on August 7th, 10th, 11th, 14th, 17th, 18th, 21st, 24th, 25th.
- The Monday, Thursday, and Friday sessions will run from 9-11 AM PDT.

Designing with the Virtex-4 Family LEL

Designing with the Virtex-4 Family Live e-Learning delivers high-value training to you remotely via the Internet, with the emphasis on keeping your work schedule and priorities intact. Scheduled over a two-week period, this course comprises a series of six 2-hour sessions. Interested in learning how to utilize Virtex-4 FPGA architectural resources effectively? This course focuses on understanding and utilizing several of the new and enhanced resources found in our newest device. Topics covered include an overview of the Virtex-4 FPGA; the Digital Clock Manager (DCM) and Phase-Matched Clock Divider (PMCD); global and regional clocking techniques; memory and FIFO; and source-synchronous resources. A combination of modules and labs allow for practical hands-on application of the principles taught in this course. This course is scheduled to begin on:

- 9/11/06, with sessions taking place on September 11th, 12th, 15th, 18th, 19th, 22nd.
- The Monday, Tuesday, and Friday sessions will run from 9-11 AM PDT.

Are you looking for a particular Xilinx course in a Live e-Learning format? If a course you desire to take is not listed above, contact a Xilinx registrar at: registrar@xilinx.com or 1-(877) XLX-CLASS.

Recorded e-Learning News

Xilinx Education Services offers a series of Recorded e-Learnings that can help you get up to speed quickly on the powerful capabilities of Xilinx technology. These recordings are currently available at no charge, over the internet anytime day or night, and can be taken anywhere there is an internet connection. View the complete set of modules available by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Recorded e-Learning" to register for any offering.

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