



Xilinx Education Newsletter - September 2006

Featured NewsFlash

[Several courses have been updated and adapted to include the latest FPGA architectures and software versions.](#)

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Instructor-Led Training News

Xilinx Education Services would like to announce the new updates for our instructor-led courses. Courses have been adapted to include the latest Xilinx FPGA architectures and labs that utilize the latest software flows.

Fundamental of FPGA Design v8.2

A revision has been made to the [Fundamentals of FPGA Design](#) course. All courses will use the new materials. Software has been updated to version 8.2

Use the ISE™ software tools to implement a design and to gain a firm understanding of the Xilinx FPGA architecture. Learn the best design practices from the pros and understand the subtleties of the Xilinx design flow.

This course covers ISE 8.2i software features, such as the Architecture Wizard and the Pin and Area Constraint Editor (PACE). Other topics include design planning, implementation options, and global timing constraints. For more emphasis on improving overall design performance, take the follow-up course [Designing for Performance](#), which builds on the basic principles covered in this course.

Designing for Performance v8.2

A revision has been made to the [Designing for Performance course](#). All courses will use the new materials. Software has been updated to version 8.2

Attending the Designing for Performance class will help you create more efficient designs. This course can help you fit your design in a smaller FPGA or lower speed grade for reducing system costs. In addition, by mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Designing with the Virtex-5 LX FPGA

For those interested in learning how to effectively utilize Virtex-5 FPGA architectural resources, Xilinx Education Services announces a new course available. Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device. Note that the initial course material covers the Virtex-5 LX FPGA platform only. Future revisions will include additional platforms as they become available.

Classes will be offered as both Instructor-Led (ILT) in San Jose, CA and as a Live e-Learning (LEL). The one day 4 hour ILT course will be on October 11th from 9-1:00 PDT.

Designing with Ethernet MAC Controllers v8.1 - Course Under Development:

A new Designing with Ethernet MAC Controllers course is currently under development by Xilinx Education Services. The 2 day course will help attendees understand Ethernet protocol and utilize the Xilinx solution for the Ethernet connectivity. Attendees will also get acquainted with various solutions Xilinx offers for Ethernet connectivity, learn the basics of Ethernet standard, protocol, and OSI model, utilize some of the solutions that Xilinx provides through hands-on laboratory exercises, gain knowledge of hardware design considerations and software development requirements.

Engineers who would like to come up to speed on utilizing the Ethernet connectivity solution that Xilinx offers both in the form of soft cores and hard IP should attend this course

After completing this training, student will be able to:

- Utilize various Ethernet cores either in a standalone mode or as a peripheral in a processor-based design
- Determine appropriate core to use
- Develop software to drive the core and achieve desired functionality
- Integrate hard and soft IP into the EDK

Look for the release of this course in September 2006.

For more information please go to <http://www.xilinx.com/education>.

Live e-Learning News

Live e-Learning allows us to convert classroom based instructor-led courses into a series of lectures and labs that are delivered by a live Xilinx instructor online. As a student, you can attend from the comfort of your desk and obtain the same knowledge taught during the traditional course. Live e-Learning works by scheduling course modules sequentially over a one to two-week period, depending upon the subject. Shortly after registering for a Live e-learning class, you will receive an FTP address for your course workbook allowing you to follow along with the material delivered by the live instructor through a Central interface and a phone. How do we conduct labs? Toolwire technology makes it possible for you to perform Xilinx labs in a virtual environment and receive hands-on experience with the Xilinx software tools while remaining online.

Sound interesting? Redeem your Training Credits for several Live e-Learnings that are upcoming in 2006! View the complete schedule and sign up today by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Live e-Learning" to register for any offering.

Advanced FPGA Implementation v8 LEL:

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE tool suite and includes labs that provide hands-on experience. Scheduled over a two-week period, this course comprises a series of six two-hour sessions (with sessions running on Monday, Tuesday, and Friday of each week).

This course is scheduled to begin on September 11th, 2006, with sessions taking place on September 11th, 12th, 15th, 18th, 19th, 22nd. The Monday, Tuesday and Friday sessions will run 9-11AM PDT.

Fundamentals of FPGA Design v8.2 LEL:

This course covers the ISE 8 software features, such as the Architecture Wizard and the Pin and Area Constraint Editor (PACE). Other topics include design planning, implementation options, and global timing constraints.

This course is scheduled to begin on October 2, 2006, with sessions taking place on October 2nd, 3rd, and 6th. The Monday, Tuesday and Friday sessions will run 9-11AM

Designing for Performance v8.2 LEL:

This Live e-Learning course teaches you how to fit your design into a smaller FPGA or a lower speed grade to reduce system costs. By mastering the tools and the design methodologies presented in this course, you can shorten your development time and lower development costs.

This course is scheduled to begin on October 9, 2006, with sessions taking place on October 9th, 10th, 13th, 16th, 17th and 19th. The Monday, Tuesday and Friday sessions will run 9-11AM PDT.

Designing with the Virtex-5 LX Platform FPGA v8.2 LEL:

Interested in learning how to effectively utilize Virtex-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device. Note that the initial course material covers the Virtex-5 LX FPGA platform only. Future revisions will include additional platforms as they become available.

This course is scheduled to begin on October 17, 2006, with sessions taking place on October 17th and 19th. The Tuesday and Thursday sessions will run 9-11AM PDT.

Are you looking for a particular Xilinx course in a Live e-Learning format? If a course you desire to take is not listed above, contact a Xilinx registrar at: registrar@xilinx.com or 1-(877) XLX-CLASS.

Recorded e-Learning News

Xilinx Education Services offers a series of Recorded e-Learnings that can help you get up to speed quickly on the powerful capabilities of Xilinx technology. These recordings are currently available at no charge, over the internet anytime day or night, and can be taken anywhere there is an internet connection. View the complete set of modules available by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Recorded e-Learning" to register for any offering.

Fundamentals of FPGA Design interactive Recorded e-Learning (iREL)

The Fundamentals of FPGA Design interactive recorded e-Learning course is offered in North America only. This training offers the most flexibility with optional audio and textual narration and interactive exercises to engage your participation and enhance your understanding of the presented material. The course comprises seven recorded modules and four hands-on labs covering the ISE™ 8.1 software features, such as the Architecture Wizard and the Pin and Area Constraint Editor (PACE). Other topics include design planning, implementation options, and global timing constraints. This e-Learning requires the free Flash Player and includes optional narration, please adjust your speakers accordingly!

AccelDSP Jump Start Modules REL:

The AccelDSP Synthesis Tool accelerates the migration of MATLAB algorithms into Xilinx FPGAs. This recorded e-learning training will provide a jump start for those who want to evaluate this flow. There are five individual modules.

After completing this training, you will be able to:

- Modify a MATLAB script for a DSP algorithm so that it can be synthesized using the AccelDSP Synthesis Tool
- Identify the concepts of quantization as well as specify, monitor, and control bit growth in a MATLAB design
- Apply MATLAB coding style changes and AccelDSP directives to optimize a design for performance and efficiency

For more information go to <http://www.xilinx.com/support/training/rel/acceldsp.htm>

Sign up today by accessing them at <https://xilinx.onsaba.net/xilinx>. Select "Recorded e-Learning."

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