



## Xilinx Platform Newsletter, August 2007

### Top Story

#### Xilinx Serial Connectivity Seminars 2007

Coming soon to a city near you: a FREE all-day event sponsored by Xilinx, with Agilent Technologies, Jungo, Linear Technology, Mentor Graphics, and Nu Horizons Electronics.

- o Learn design techniques from industry experts
- o High-speed serial design and verification
- o PCI Express®, 1G & 10G Ethernet standards
- o FPGA implementation, protocol testers, signal integrity tools, device drivers, and more

Register now to win an iPod at [www.xilinx.com/serialseminar](http://www.xilinx.com/serialseminar)

### In This Issue

- [Quick Update](#)
- [Development Tools](#)
- [Design Tips](#)
- [Education](#)
- [Partner Spotlight](#)
- [In the Press](#)
- [We Want to Hear From you](#)
- [Have the Latest Virtex Information Delivered to Your Desktop](#)

### Quick Links

- [Xilinx Home](#)
- [Xilinx Virtex™ Series FPGAs](#)
- [Xilinx Spartan™-3 Generation FPGAs](#)
- [Xilinx CPLDs](#)
- [Xilinx Design Tools](#)
- [Xilinx IP Center](#)
- [Xilinx Boards and Kits](#)
- [Xilinx Services & Support](#)
- [Xilinx Online Store](#)
- [Xilinx Documentation](#)
- [Find Your Local Sales Office](#)



### Quick Update

#### [Virtex-5 FPGAs Provide Early Path to DDR3 SDRAM Adoption](#)

Achieving 800 Mbps DDR3 interfaces requires precise control over I/O timing. Read about successful Virtex-5 [interoperability tests](#) performed with DDR3 SDRAM devices from leading manufacturers.

#### **DDR2-400 Support For Spartan-3 Generation FPGAs**

[Download](#) the free, hardware-verified, 400 Mbps DDR2 SDRAM interface reference design for low-cost Spartan-3A and Spartan-3AN FPGAs, including graphic demo files.

#### **On-demand Webcast Seminars:**

- [Accelerate Delivery of Built-in Ethernet Solutions Using Xilinx FPGAs and Gigabit Ethernet Development Kit](#)
- [Discover How to Design With and Take Advantage of the PCI Express Hard Block in the Virtex-5 FPGA](#)
- [Cost Effective Digital Radio Processing Solutions Using New Spartan-DSP and Virtex-5 SXT](#)

### Development Tools

#### **ISE WebPACK 9.2i Expands Virtex-5 Support**

Available as a free download, ISE™ WebPACK™ 9.2i provides the tools, features, and easy-to-use design environment of the ISE Foundation™ design suite. This latest release adds support for Virtex-5 LX30T, LX50, and LX50T devices.

— [Download FREE ISE WebPACK 9.2i Today!](#)

### Design Tips

## [Technical Paper: Security Solutions Using Spartan-3 Generation FPGAs](#)

Security has become a critical issue in our global society, and is rapidly becoming indispensable in the electronics industry. This white paper identifies top design security threats, explores basic levels of security, and describes how new, low-cost Spartan-3A, Spartan-3AN, and Spartan-3A DSP FPGAs from Xilinx can help protect products and profits.

## [Create Memory Interface Designs Faster with Xilinx Solutions](#)

Xilinx simplifies DDR and DDR2 memory interface design with hardware-verified reference designs, easy-to-use software tools, and complete development kits

## [Making the Most of MOST Control Messaging](#)

At only 2,600 slices, the Xilinx MOST® (Media Oriented Systems Transport) network interface controller (NIC) occupies roughly half of a Spartan-3E 500 device, which leaves plenty of room for the microprocessor and other peripherals.

## Education

---

### **XES: Xilinx Education Services**

Receive targeted, high-quality education designed by experts in programmable logic design and delivered by Xilinx-qualified trainers. XES delivers training when and where you need it by leveraging our global network of 22 Authorized Training Providers (ATP) and online learning systems.

### **This Month's Featured Courses:**

- [Designing a LogiCORE™-based PCI Express System](#)

Learn how to build PCI Express interface designs faster and more easily when using IP from Xilinx.

- [Designing with PlanAhead™](#)

This course focuses on how you can increase design performance and achieve repeatable results with the PlanAhead software tool.

- [Introduction to AccelDSP™](#)

Learn how to synthesize an algorithm written in MATLAB® into a design optimized for a Xilinx FPGA. We cover how to use the floating-to-fixed point and design exploration features of the AccelDSP Synthesis Tool to achieve maximum results ... and much more.

## Partner Spotlight

---

### [Automated MGT Serial Link Tuning Ensures Design Margins](#)

Streamline the serial link tuning process using Agilent's Serial Link Optimizer tool with Xilinx IBERT measurement cores. An internal bit error ratio tester (IBERT) measurement core from Xilinx can view serial signals at an internal receiver point. Used in conjunction with the Agilent Serial Link Optimizer, you can have both a graphical view of the BER across the unit interval and automatically adjust pre-emphasis and equalization settings to optimize the channel.

### [Efficient DSP Algorithm Development for FPGA and ASIC Technologies](#)

This white paper discusses the challenges and requirements of creating portable algorithmic IP for FPGAs and ASICs and illustrates how an ESL synthesis methodology using Synplicity's Synplify DSP tool can significantly reduce the time and effort to implement either technology.

### [High-performance, High-capacity FPGA Platforms for ASIC Prototyping and Emulation.](#)

The Synplicity HAPS modular ASIC prototyping system offers high performance, configurability, and over 30 daughter cards. The HAPS-54 Virtex-5 motherboard features an 8 million gate capacity.

### [HiGig IP for Virtex-5 FPGAs](#)

GDA Technologies offers a 10G Ethernet MAC core that implements the Broadcom proprietary HiGig Protocol.

## In the Press

---

## **Customers Building Products with Virtex FPGAs**

### **Samsung Picks Xilinx Processors For Digital Video Surveillance System**

Samsung Electronics will use the Xilinx Spartan-3E FPGA and MicroBlaze™ soft processor in its latest digital video surveillance system, in which the components will play a vital role in both the digital video recorder (DVR) and dome camera.

### **MiniFX FPGA Board Processes Real-time Streaming Data**

Embedded Systems Design Inc. (ESD) has released the StreamBlade MiniFX, a 3.5 x 3.0-inch FPGA-based board, for processing real-time streaming data. Applications include telecommunications protocol processing, software-defined radio (SDR), and real-time streaming data for video and voice processing, generation, recording, and playback. The MiniFX allows developers to take full advantage of its configured Xilinx Virtex-4 FPGA available with a FX20, FX40, or FX60.

## **Partner Solutions for Virtex Design**

### **Compact SOM Logic Module Speeds Designs To Market**

With a modular architecture that facilitates the simple integration of user logic and custom peripheral sets, the LM125 compact logic module from Advanced Knowledge Associates lets systems designers get to market quickly. The system-on-module (SOM) device is based on a high-density Spartan IIE FPGA fabric and employs a µBlaze soft CPU core from Xilinx.

### **Silicon Interfaces Announces Release of New SI85SCC30-A Serial Communication Controller IP**

Silicon Interfaces, Ltd. has announced the availability of the SI85SCC30-A Serial Communication Controller IP, a versatile full-duplex, dual-channel multi-protocol data communication peripheral, with triple-buffered receiver and double buffered transmitter. Targeted at Xilinx Virtex-4 FPGAs, this SCC is a VHDL-based soft IP.

## **Virtex Design Solutions from Xilinx**

### **First Production FPGAs to Demo Interoperability with DDR3 SDRAM Technology**

Xilinx has announced that its Virtex-5 FPGA devices are interoperable with 800 Mbps DDR3 SDRAM devices from leading memory suppliers. Hardware-proven interoperability with Virtex-5 devices provides customers with an early path to adopt DDR3 SDRAM technology with the industry's only high-performance 65-nm FPGA family shipping in production.

### **FPGA Software Simplifies I/O Assignment**

PinAhead technology provides the ability to assign interface I/O groups to I/O pins simply by dragging into a graphical representation of the FPGA - Xilinx has released a new version of its PlanAhead hierarchical design and analysis design tool featuring the expanded functionality of Xilinx PinAhead technology.

### **Greater Power Efficiency for Xilinx High-performance Spartan-3A DSP FPGAs**

Xilinx has announced the addition of power efficient Spartan-3A DSP devices to its XtremeDSP™ portfolio of solutions for signal processing applications. The new devices, which are in production today, deliver high-performance DSP capabilities in a low-power FPGA for applications such as tactical radios for military communications, wireless access points and portable medical equipment.

---

© Copyright 1994-2007 Xilinx, Inc. All Rights Reserved

This email was sent to: %%emailaddr%%

This email was sent by: %%Member\_Busname%%  
%%Member\_Addr%%  
%%Member\_City%%, %%Member\_State%%, %%Member\_PostalCode%%  
%%Member\_Country%%

Xilinx does not rent, sell or lease customer information. We respect your right to privacy - [view](#) our policy.

You are currently subscribed to receive Xilinx email communications.  
Go [here](#) to view/modify your preferences.

Go [here](#) if you no longer wish to receive Xilinx email.

If you have difficulties or questions about this process, please contact: [xilinxmail@xilinx.com](mailto:xilinxmail@xilinx.com)