



XAPP1073 (v1.0) May 17, 2010

NSEU Mitigation in Avionics Applications

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Summary

Neutron-induced single event upset (NSEU) is a known phenomenon in the memory structures of modern ICs used in terrestrial applications. With current and next-generation aircraft operating at altitudes of 40,000 feet and higher, the increased atmospheric neutron flux raises the likelihood of this phenomenon by several orders of magnitude with the potential to impact flight safety. The decreasing feature size of memory structures combined with the growth in memory size means that system susceptibility to NSEUs is growing. SRAM-based FPGAs pose a unique challenge for avionics manufacturers because an FPGA's functionality depends on the integrity of its configuration memory. It is vital for FPGA designers to achieve NSEU hardness for critical avionics systems through a combination of soft and hard mitigation techniques.

This application note provides background on NSEUs in SRAM-based FPGAs, mitigation techniques (with a focus on configuration memory) suggested by Xilinx, and an overview of calculating projected failures-in-time (FIT) rates⁽¹⁾ at altitude.

Introduction

Cosmic Rays and Air Showers

Cosmic rays originate in outer space, travel at nearly the speed of light, and strike Earth from all directions. Cosmic rays are the nuclei of atoms, ranging from the lightest to the heaviest elements in the periodic table.

Neutrons are generated in the atmosphere by high-energy cosmic ray particles through direct nuclear spallation reactions with the atoms in the atmosphere, often referred to as an air shower. Neutrons with energy greater than 10 MeV carry sufficient energy to cause single-event effects in SRAM-based FPGAs.

Air pressure also plays a significant role in causing neutron-generating reactions and in transporting neutrons to ground level. An intense neutron environment exists at higher altitudes in the atmosphere, 10 km to 40 km and more above the surface. In addition, Earth's magnetic field causes the flux to vary from the equator to the poles, with the equator having the least flux and the poles having the greatest flux. The magnetic field of the sun as it varies during the sunspot cycle also influences the flux of cosmic rays on earth by roughly 20%.

Long-haul aircraft flying at altitudes at or near 40,000 feet along flight paths above 60° latitude experience the greatest neutron flux of all flights—roughly 500 times that of a ground-based observer in New York City. See [Figure 1](#). See also [Derating Rosetta Results for Altitude and Latitude, page 10](#).

1. *FIT rate* is defined as the number of failures that can be expected in 10⁹ device hours.

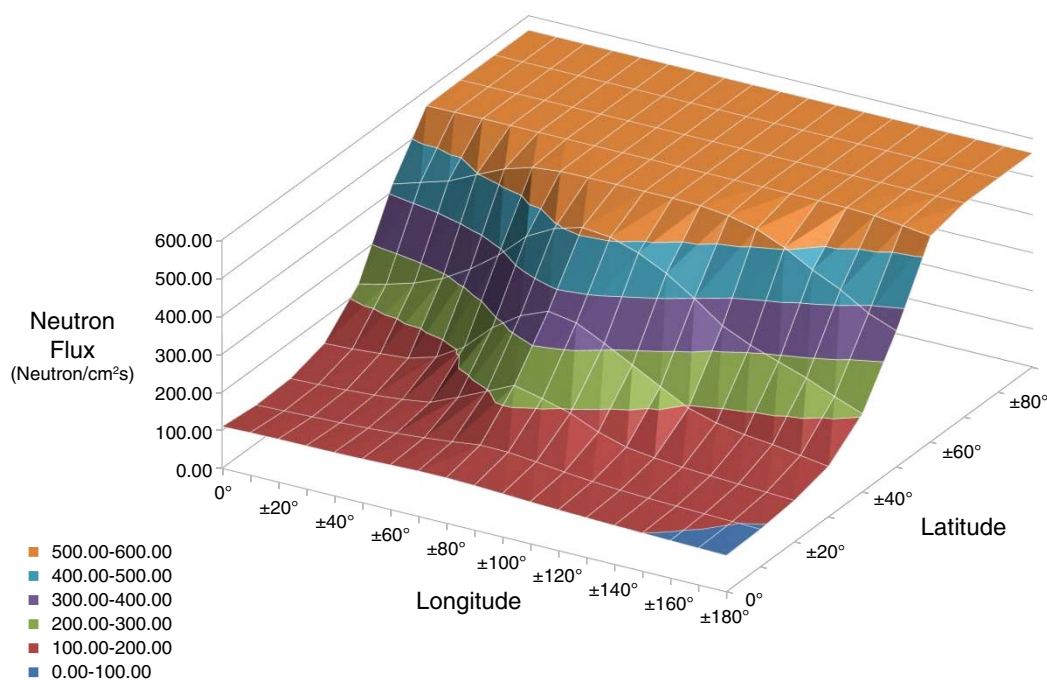


Figure 1: Neutron Flux at 40,000 Feet [Ref 1]

Neutron-Induced Single Event Upsets

When a high-energy neutron passes through the silicon substrate of a device, charged particles are created as the result of collisions. If the charge of these particles is sufficient, then they can change the state of a static memory element. These changes of state are referred to as NSEUs. See Figure 2.

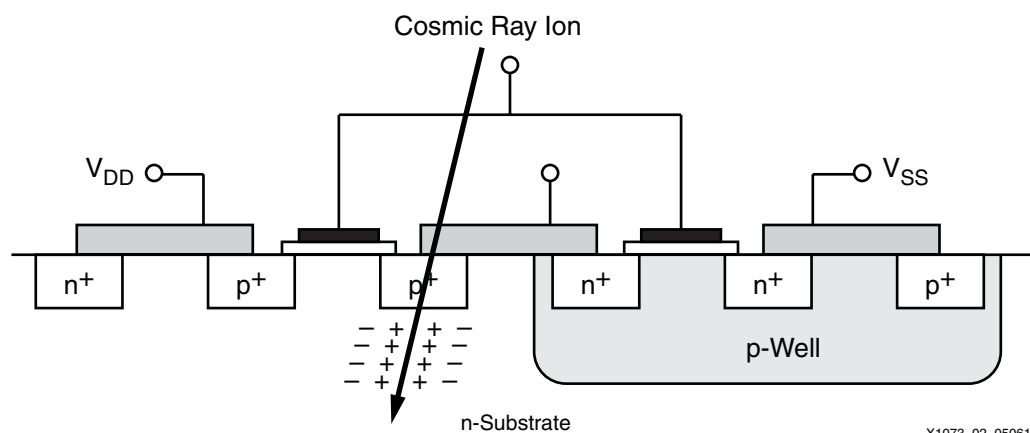


Figure 2: NSEUs in an FPGA

The system experiences memory device NSEUs as changes in data bits. With an SRAM-FPGA, not only do NSEUs occur in the device memory but in the configuration memory as well, potentially creating a change in the FPGA's programmed logic.

NSEUs are temporary (soft) in nature and are corrected with the next change in state of the affected memory element. There are no known impacts to long-term device reliability due to NSEUs.

Note: In addition to the neutron flux, there is also a flux of protons that, depending upon altitude, can be as much as 35% of the neutron flux. Since protons can also cause upsets, this additional flux should be included in any FIT-rate calculation. The exact derating factor that should be used is often set by the aircraft manufacturer or its prime contractors.

Real-World Impact

While much of the discussion regarding NSEUs seems theoretical, focusing upon the probability of an event or failures-in-time (FIT) rates, there can be a real impact on flight safety. On October 7, 2008, a Qantas A330 en route from Singapore to Perth suddenly pitched violently downward twice in rapid succession, diving 650 feet and then 400 feet in altitude, seriously injuring one flight attendant and eleven passengers. The Australian Transport Safety Bureau (ATSB) is investigating the possibility of the errors in the Air Data Inertial Reference Unit (ADIRU) having occurred as the result of NSEUs. [\[Ref 2\]](#)

Clearly, NSEUs are a real-world concern, and designs using FPGAs in avionics systems should employ mitigation schemes where necessary.

NSEU and DO-254

RTCA/DO-254 and its counterpart in Europe, EUROCAE/ED-80, are the guidelines for the design of complex electronic hardware (CEH) for use in avionics systems. FAA advisory circular AC 20-152 made DO-254 an official requirement for suppliers of civil aviation avionics systems. DO-254 is a collection of best industry practices for design assurance of airborne electronic hardware. These guidelines advocate a top-down approach for design and verification of safety-critical electronics and other avionics systems and represent the consensus of the aviation community.

The FAA has defined a number of levels regarding the safety and criticality of an avionics system. For example, engineers designing to level A or B face a much more rigorous test, verification, and documentation process than for levels C, D, or E. All flight hardware needs to be classified as having one of these failure levels. [\[Ref 3\]](#)

As a result, level A or B systems require that mitigation techniques be applied, while lower-level systems—for example, in-flight entertainment systems—might be able to live with the rare occurrence of an NSEU without impacting performance or safety. Engineers need to analyze the requirement of mitigation for each system versus the overhead of a specific mitigation technique.

Areas Requiring Mitigation in Virtex-5 and Virtex-6 FPGAs

When considering NSEU mitigation, one must look at the different types of static memory storage within an FPGA. There are four components that comprise the memory content of Xilinx FPGAs:

- **Flip-flops** – the flip-flops contained in the configurable logic block (CLB) for user logic
- **LUT RAM** – distributed register files/RAM built out of the LUTs in the CLB for user logic
- **Block memory** – the embedded memory blocks for user logic
- **Configuration memory** – the memory used to store configuration (routing, logic structure, etc.) for the FPGA

Each of these memory areas requires different mitigation strategies. NSEUs in two of these areas (flip-flops and block memory) are a phenomenon common to all programmable technologies, however, this application note's main focus is on mitigating configuration memory NSEUs.

CLB Flip-Flops

Accelerated SEU testing predicts the FIT rate for CLB flip-flops to be as low as one to two per megabit, indicating that the data contained in these flip-flops is the least likely in the FPGA to suffer an SEU. [\[Ref 4\]](#) Given this low value and the relatively low number of flip-flops in a device

(as compared to other areas of the FPGA), flip-flops can be normally omitted from risk calculations. For example, the Xilinx® Virtex®-5 XC5VLX50T FPGA has approximately 0.03 Mb of flip-flops, which means a maximum device flip-flop FIT of 0.06 at sea level. This translates to a mean time between failures (MTBF) of nearly 2 million years—even if all flip-flops in the device are used.

However, any mission-critical areas of the user design can be protected with standard mitigation techniques—for example, by employing design redundancy techniques such as triple modular redundancy (TMR).

Distributed or LUT RAM

Virtex-5 and Virtex-6 device CLBs are composed of SLICEL and SLICEM slices. The LUTs in SLICEMs can implement a synchronous RAM (referred to as distributed RAM) or a 32-bit shift register without using the flip-flops available in the slice. [Ref 5][Ref 6]

When a design uses the LUTs in a SLICEM for distributed memory functions (either as RAM or a shift register), the write controls associated with those LUTs are passed from the FPGA configuration interface to the user design. During normal device operation, the contents of the LUT RAM are changed from their initial values contained in configuration memory. Therefore, any SEU correction causes the user content of the LUT RAM to be overwritten with the initial content from the configuration memory.

To prevent the user content of distributed RAM from being overwritten, the GLUTMASK configuration option must be set. As a result, an SEU to these bits cannot be corrected via a configuration memory mitigation scheme; rather, it must be mitigated in the user design.

Users should be aware of this distinction, either implementing data error and correction schemes for distributed RAM used in the design, or avoiding the use of these functions.

Embedded Block RAM

Both Virtex-5 and Virtex-6 devices include large amounts of bulk RAM for use as 36 Kb dual-port RAM, known as block RAMs. Each 36 Kb block RAM contains two independently controlled 18 Kb RAMs. Block RAMs are placed in columns, and the total number of block RAM memories depends on the size of the device.

As with all static RAM structures, block RAMs are susceptible to NSEUs. Due to the operation speed requirement for these RAM cells, they are more susceptible to upset when compared to configuration memory and CLB flip-flops. In fact, testing indicates that the block RAM cells are roughly five times more susceptible to upset than the configuration memory (see [The Rosetta Experiment, page 10](#)).

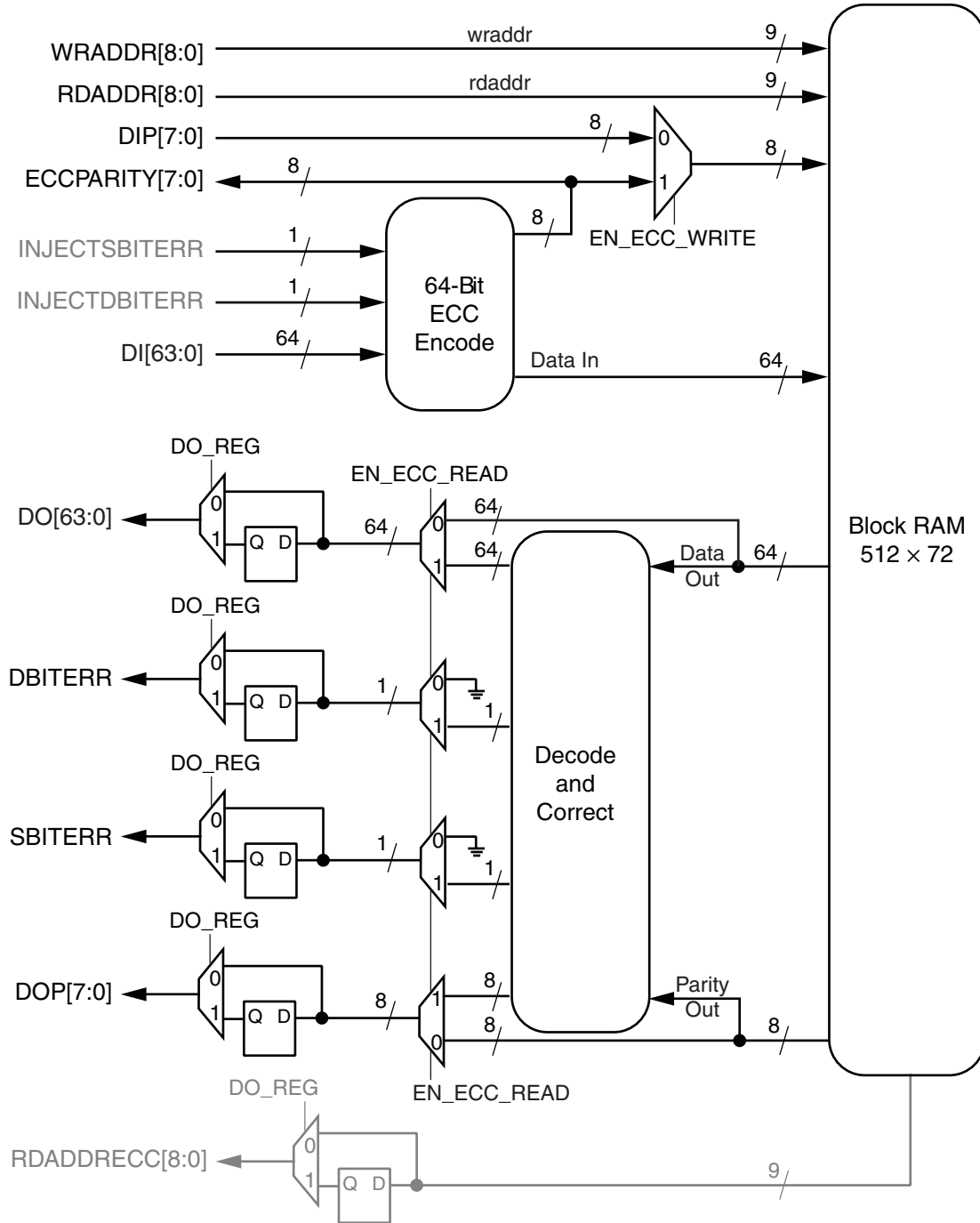
Fortunately, each Virtex-5 and Virtex-6 block RAM is equipped with built-in error correction code (ECC) functionality, which operates transparently to the user. This ECC configuration option is available with a 36 Kb block RAM in simple dual-port mode (x72) or a 36 Kb FIFO primitive (x72).

Note: Built-in ECC support is available only with the RAMB36E1 and FIFO36E1 primitives for Virtex-6 FPGA designs and the RAMB36SDP and FIFO36_72 primitives for Virtex-5 FPGA designs.

A block RAM in simple dual-port mode can be configured as a single 512 x 64 RAM, enabling the use of the built-in Hamming code error correction with the extra eight bits in the 72-bit-wide RAM used for ECC storage.

Eight protection bits (ECCPARITY) are generated during each write operation and stored with the 64-bit data in the memory. These ECCPARITY bits are used during each read operation to correct any single-bit error or to detect (but not correct) any double-bit error. The ECCPARITY bits are written to the memory and output to the FPGA fabric at each rising edge of WRCLK. There are no optional output registers available for the ECCPARITY output bits.

During each read operation, 72 bits of data (64 bits of data and an 8-bit parity word) are read from the memory and fed into the ECC decoder. The ECC decoder generates two status outputs, SBITERR and DBITERR, that are used to indicate the three possible read results: no error, single-bit error corrected, or double-bit error detected. In the standard ECC mode, the read operation does not correct the error in the memory array, it only presents corrected data on DO. The Virtex-5/Virtex-6 FPGA ECC operation is illustrated in Figure 3.



Features specific to Virtex-6 FPGAs are shown in gray

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Figure 3: Top-Level View of Virtex-5/Virtex-6 FPGA Block RAM ECC

Configuration Memory

Virtex-5 and Virtex-6 devices are configured by loading application-specific configuration data—the bitstream—into internal memory via the configuration interface. This data contains bits that set the configuration for each LUT and flip-flop, as well as all routing connections, the configurations for embedded elements, and so forth.

These cells are robust in nature, as they are expected to remain static—as opposed to the block RAM memory cells, which are designed for speed. As a result, an individual configuration cell is less susceptible to NSEU than the block RAM cells. However, the configuration memory represents the largest amount of static RAM in a Virtex-5 or Virtex-6 FPGA—typically four to six times the number of block RAM bits.

Table 1: Static Memory Content of Virtex-5/Virtex-6 FPGAs

Device	Total Number of Configuration Bits (Less Block RAM)	Slices	CLB Flip-Flops	Max Distributed RAM (Kb)	Block RAM	
					Blocks	Max (Kb)
Virtex-5 FPGAs:						
XC5VLX30	7,030,528	4,800	19,200	320	32	1,152
XC5VLX50	10,541,440	7,200	28,800	480	48	1,728
XC5VLX85	17,815,168	12,960	51,840	840	96	3,456
XC5VLX110	23,750,656	17,280	69,120	1,120	128	4,608
XC5VLX155	32,987,136	24,320	97,280	1,640	192	6,912
XC5VLX220	45,078,528	34,560	138,240	2,280	192	6,912
XC5VLX330	67,613,440	51,840	207,360	3,420	288	10,368
XC5VLX20T	6,251,200	3,120	12,480	210	26	936
XC5VLX30T	9,371,136	4,800	19,200	320	36	1,296
XC5VLX50T	14,052,352	7,200	28,800	480	60	2,160
XC5VLX85T	23,341,312	12,960	51,840	840	108	3,888
XC5VLX110T	31,118,848	17,280	69,120	1,120	148	5,328
XC5VLX155T	43,042,304	24,320	97,280	1,640	212	7,632
XC5VLX220T	55,133,696	34,560	138,240	2,280	212	7,632
XC5VLX330T	82,696,192	51,840	207,360	3,420	324	11,664
XC5VSX35T	9,318,656	5,440	21,760	520	84	3,024
XC5VSX50T	13,973,632	8,160	32,640	780	132	4,752
XC5VSX95T	24,968,192	14,720	58,880	1,520	244	8,784
XC5VSX240T	57,442,816	37,440	149,760	4,200	516	18,576
XC5VFX30T	9,318,656	23,200	92,800	1,500	228	8,208
XC5VFX70T	18,964,480	37,440	149,760	2,400	324	11,664
XC5VFX100T	27,298,304	5,120	20,480	380	68	2,448
XC5VFX130T	34,120,704	11,200	44,800	820	148	5,328
XC5VFX200T	48,689,152	16,000	64,000	1,240	228	8,208
XC5VTX150T	43,278,464	20,480	81,920	1,580	298	10,728
XC5VTX240T	65,755,648	30,720	122,880	2,280	456	16,416
Virtex-6 FPGAs:						
XC6VLX75T	19,859,904	11,640	93,120	1,045	156	5,616
XC6VLX130T	33,086,880	20,000	160,000	1,740	264	9,504

Table 1: Static Memory Content of Virtex-5/Virtex-6 FPGAs (Cont'd)

Device	Total Number of Configuration Bits (Less Block RAM)	Slices	CLB Flip-Flops	Max Distributed RAM (Kb)	Block RAM	
					Blocks	Max (Kb)
XC6VLX195T	48,042,720	31,200	249,600	3,140	344	12,384
XC6VLX240T	57,651,264	37,680	301,440	3,770	416	14,976
XC6VLX365T	80,466,048	56,880	455,040	4,130	416	14,976
XC6VLX550T	120,699,072	85,920	687,360	6,200	632	22,752
XC6VLX760	159,516,864	118,560	948,480	8,280	720	25,920
XC6VSX315T	76,966,848	49,200	393,600	5,090	704	25,344
XC6VSX475T	115,450,272	74,400	595,200	7,640	1,064	38,304
XC6VHX250T	59,766,336	39,360	314,880	3,040	504	18,144
XC6VHX255T	59,766,336	39,600	316,800	3,050	516	18,576
XC6VHX380T	89,649,504	59,760	478,080	4,570	768	27,648
XC6VHX565T	125,574,624	88,560	708,480	6,370	912	32,832

The sheer volume of memory bits in the configuration memory could cause concern from an SEU perspective. However, despite the large size, only a fraction of the configuration bits affect any given design. Less than 20%, and typically less than 10%, of the configuration cells have any significance to a design, reducing the total impact of SEUs.

A large number of unused configuration cells are also within the area of an otherwise used resource. For example, the programmable interconnect has many possibilities, but only a few of those apply to a particular design. Consequently, an SEU that causes the connection of an unused segment of interconnect to another unused segment has no effect on a given design. Even if an SEU were to connect an unused segment to a used segment, it is unlikely to have any impact on the user design.

Based on Xilinx white paper *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* [Ref 4], a Virtex-5 device shows a nominal 151 FIT/Mb at sea level for the configuration cells with a 95% confidence range of 101–215 FIT/Mb. For example, the XC5VLX50 device has 10,541,440 bits, or approximately 10.05 Mb of configuration cells, and therefore a nominal susceptibility of 1,518 FIT or an MTBF of 75.2 years. The device configuration FIT has a 95% confidence range of 1,015 to 1,442 or an MTBF of 52.8 to 112 years at sea level.

Based on the assumed worst-case derating factor for commercial aviation derived in [Derating Rosetta Results for Altitude and Latitude](#) of 561.7, the 95% confidence range for the XC5VLX50 yields an MTBF of 1.23 to 2.61 months.

However, this calculation is overly pessimistic. Given that less than one-fifth of the configuration bits are actually used in a given design, the above rates are improved by a factor of five. This number further improves when the design occupies less than 100% of the resources.

While not in any way seeking to trivialize the NSEU issue, even the unmitigated MTBF exceeds the average length of a commercial flight by orders of magnitude, given that flight times are less than 24 hours in length and that the clock on configuration NSEUs resets with each power cycling. However, with thousands of flights per day and multiple devices being used in a typical system, mitigation strategies for resolving configuration memory NSEUs *are* required for flight-critical applications.

Note: These calculations assume that the SEU results in a single-bit change. In fact, the Rosetta experiment demonstrates multi-bit upsets (MBUs) due to a single ionizing particle is rare. In lower geometries, there is a potential for increased MBU rates.

Configuration Memory Mitigation Techniques

A number of configuration memory mitigation techniques are available to the user, allowing the designer to scale the amount of mitigation required by the application.

Built-In Configuration SEU Detection

Virtex-5 devices introduced a new device functionality that performs continuous background readback of configuration data in a user design. This feature can be used in conjunction with the FRAME ECC feature for advanced operations such as SEU corrections. Once enabled, the configuration dedicated logic reads back continuously in the background to check the CRC of the configuration memory content. After the CRC indicates an error, then the FRAME_ECC is used to determine if a (correctable) single-bit error or an (uncorrectable) multi-bit error has occurred.

For Virtex-5 devices, the first round of readback CRC value is latched as the golden value for later comparison. The subsequent rounds of readback CRC values are compared against the golden value. When a CRC mismatch is found, a CRC error is asserted. The error flag remains asserted until the next comparison if the error was not corrected. If no new golden CRC is calculated, then the error flag remains asserted. When the user logic accesses the configuration logic through an ICAP command, JTAG, or a SelectMAP persist, the readback CRC error automatically stops without affecting the user configuration access, and the error flag is cleared. When the user finishes accessing the configuration logic, readback CRC automatically resumes.

For Virtex-6 devices, the built-in CRC readback function can detect single-bit and double-bit errors. The Virtex-6 FPGA CRC readback process operates in a similar manner to that of the Virtex-5 FPGA, except that in the first round of readback, the ECC syndrome bits are calculated by the hardware itself, i.e., calibrated. In the second round of readback, the CRC value is latched as the golden value for later comparison. The subsequent rounds of readback CRC value are compared against the golden value. Any single-bit errors are corrected automatically.

These dynamically changeable memory locations within the configuration memory are masked during background CRC readback:

- Distributed memory functions
- Dynamic reconfiguration port (DRP) memories
- Block RAM content, skipped to avoid interfering with user functions (block RAM is covered by its own ECC circuit during operation)

See the *Virtex-5 FPGA Configuration User Guide* [Ref 7] and the *Virtex-6 FPGA User Guide* [Ref 8] for more details on CRC readback.

Although a configuration upset is detected and reported, only the behavior of the design and system can deduce if the SEU has any effect on device operation. As described earlier, an SEU has no effect in the majority of cases; however, when an SEU does impact the application, the potential exists for undesirable application behavior from the time the SEU occurs until it is detected and corrected.

A logical error caused by an SEU could also result in prolonged corruption of informational data. This might be tolerable if the repair is made quickly and has no lasting effects. However, a logical error that adversely affects the control paths or operating states of a design can have lasting effects, and precautionary logic might be required in this situation. One potential solution is to issue a reset to all critical circuits upon detection of an error and then remove the reset after the error has been corrected.

SEU Correction For Virtex-5 FPGAs

SEU Strategies for Virtex-5 Devices [Ref 1] describes a number of SEU correction schemes for Virtex-5 FPGAs. The one technique that best replicates the built-in SEU correction capability of Virtex-6 FPGAs is the running repairs strategy. In this strategy, the built-in readback CRC feature of a Virtex-5 device is first used to detect changes to the configuration cells. Having detected an error, it must then be located. The exact location can be determined using the configuration error correcting codes (ECC) and the embedded calculator circuit to identify the location of a single-bit error in the frame read.

In principle, the correction is straightforward. The corrupted frame is read into a buffer, the single-bit error is isolated by interpreting the ECC value, and it is then corrected. The correction simply inverts the bit to reverse the inversion caused by the SEU. Finally, the corrected frame is written back into the configuration cells.

After an error is corrected, the readback CRC circuit restarts and confirms that the error is repaired after one complete scan of the device. Although the ECC bits enable the correction of any single-bit error, it is not possible to correct multiple-bit errors within the same configuration frame (1,312 bits). In the unlikely event two errors occur in the same frame, the error condition persists, and the system must determine a suitable course of action.

To assist users, Xilinx provides an SEU controller macro to perform all the necessary steps of correcting SEUs. See *SEU Strategies for Virtex-5 Devices* [Ref 1] for complete details.

For Virtex-6 FPGAs

If correction is enabled, then the readback CRC logic performs correction on single-bit errors. During readback, the syndrome bits are calculated for every frame. If a single-bit error is detected, the readback is stopped immediately. The frame in error is read back again, and, using the syndrome information, the bit in error is fixed and written back to the frame. If the CRC logic is set to correct and continue, then the readback logic starts over from the first address. If set to correct and halt, the readback logic stops after correction. See the *Virtex-6 FPGA User Guide* [Ref 8] for further details.

Brute-Force SEU Correction

SEU Strategies for Virtex-5 Devices [Ref 1] discusses two additional SEU correction schemes that can be applicable to avionics systems: [Scheduled Maintenance](#) and [Emergency Maintenance](#).

Scheduled Maintenance

The scheduled (or preventive) maintenance strategy exploits every available opportunity to reconfigure the device during normal operation and reconfigure whenever it is not playing an active role in the system. No attempt is made to determine if an SEU has occurred; the reconfiguration simply repairs any corruption, if it exists. Ideally, an MTBF is calculated for the application and reconfiguration scheduled well within that time.

While this method might not be sufficient for avionics applications, it can be used in conjunction with a methodology that detects and corrects SEUs to reset the clock for an MTBF event, further enhancing system reliability. For example, systems can be reset while on the ground prior to flight and, given the redundant nature of avionics systems, under controlled conditions during flight.

Emergency Maintenance

The emergency maintenance strategy involves forcing a reconfiguration upon detection of an SEU, rather than attempting to identify and correct the error. While this might be seen as a safe approach, it does require additional planning to ensure a graceful reboot.

Critical Bits Technology

Currently in development, *critical bits technology* takes advantage of the fact that less than 20% of the configuration memory bits are essential or critical to the functionality of a design. This technology operates in conjunction with the built-in configuration SEU detection scheme for Virtex-5 and Virtex-6 FPGAs and the SEU correction capabilities of either the Virtex-5 FPGA SEU controller macro or the Virtex-6 FPGA SEU correction mechanism.

With critical bits technology, any detected SEU is corrected and the user design notified of the event along with its location and whether the affected bit is critical to the user design or not. Based upon this information, the user design can undertake any desired additional mitigation—for example, a full reconfiguration.

The Rosetta Experiment

The Rosetta experiment is an ongoing project at Xilinx that collects real measurements of SEUs and applies the knowledge gained when engineering each new product. Each Rosetta experiment consists of multiple sets of 100 of the largest Xilinx FPGAs, using differing technologies, located at ten different altitudes.

The test data for Virtex-5 FPGA families confirms that these devices have significantly lower susceptibility to SEUs than their predecessors. Details of the Rosetta experiment are available. [\[Ref 4\]](#)

Derating Rosetta Results for Altitude and Latitude

Although the Rosetta experiment tested devices at 10 different altitudes, the focus was on terrestrial applications. The test data can be used by derating the results for altitude and longitude. [Table 2](#) lists the derating factors from the reference by latitude and longitude at 40,000 feet. Per JEDEC Standard No. 89A (JESD89A) [\[Ref 9\]](#), the reference of 1.000 is set at sea level at the latitude and longitude of New York City.

Using two long-haul flights as representative examples (BA284 between San Francisco and London on April 11, 2010 and UL862 between Hong Kong and San Francisco on April 18, 2010), the first flight reached a latitude of 65° and the second flight reached an altitude of 39,000 feet. [\[Ref 10\]](#) Clearly, based on these examples, a worst-case derating factor of 561.70 should be used for commercial avionics applications.

Table 2: Derating Factors by Latitude and Longitude at 40,000 Feet [\[Ref 11\]](#)

Longitude	Latitude									
	0°	10°	20°	30°	40°	50°	60°	70°	80°	90°
0°	109.49	100.62	104.37	131.57	222.10	419.22	559.93	561.70	561.70	561.70
10°	111.59	103.09	107.01	134.72	239.35	441.25	560.73	561.70	561.70	561.70
20°	112.66	105.50	110.34	140.69	260.48	463.07	561.50	561.70	561.70	561.70
30°	112.96	108.10	114.96	146.52	290.39	497.65	561.69	561.70	561.70	561.70
40°	113.35	111.59	121.59	167.52	333.40	530.70	561.70	561.70	561.70	561.70
50°	114.66	116.30	132.08	211.90	387.28	552.59	561.70	561.70	561.70	561.70
60°	116.82	122.50	163.33	280.60	454.95	560.16	561.70	561.70	561.70	561.70
70°	118.84	130.16	196.71	329.90	493.72	561.48	561.70	561.70	561.70	561.70
80°	119.06	139.55	230.46	360.00	514.32	561.67	561.67	561.70	561.70	561.70
90°	116.93	138.42	213.65	347.28	506.89	561.63	561.70	561.70	561.70	561.70
100°	113.35	131.18	193.2	311.59	483.35	561.50	561.70	561.70	561.70	561.70
110°	109.77	122.38	162.04	272.62	447.68	560.04	561.70	561.70	561.70	561.70
120°	106.75	115.68	140.12	233.48	399.60	551.89	561.70	561.70	561.70	561.70
130°	104.20	110.91	130.16	195.44	346.05	534.99	561.70	561.70	561.70	561.70
140°	102.01	107.74	123.64	174.36	313.20	503.85	561.67	561.70	561.70	561.70

Table 2: Derating Factors by Latitude and Longitude at 40,000 Feet (Cont'd) [Ref 11]

Longitude	Latitude									
	0°	10°	20°	30°	40°	50°	60°	70°	80°	90°
150°	100.05	105.15	119.06	161.49	287.54	463.07	561.27	561.70	561.70	561.70
160°	98.24	102.84	115.37	153.78	262.51	429.35	558.02	561.70	561.70	561.70
170°	96.56	100.54	111.88	142.74	232.13	385.15	549.99	561.70	561.70	561.70
180°	95.00	98.16	108.20	131.82	204.62	356.77	540.63	561.70	561.70	561.70

Conclusion

While NSEUs are a known issue in avionics applications, and SRAM-based FPGAs have an additional susceptibility over other programmable technologies due to the volatility of their configuration memories, Xilinx has developed a number of mitigation techniques and structures. These techniques and structures range from SRAM cells designed to logic design rules (not to memory design rules), built-in ECC structures in block RAM to SEU detection, and correction structures built into hardware. All memory elements are susceptible to NSEUs, but with proper mitigation techniques, SRAM-based FPGAs provide avionics designers with a much wider range of possible solutions.

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Related Information

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http://www.xilinx.com/support/documentation/user_guides/ug363.pdf
2. UG116, *Device Reliability Report*
http://www.xilinx.com/support/documentation/user_guides/ug116.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/17/10	1.0	Initial Xilinx release.

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