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Implementing Xilinx Flip-Chip BGA Packages

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Summary

Xilinx flip-chip BGA packages are offered for Xilinx high-performance FPGA products. Unlike wire-bond packaging in which the die is attached to the substrate face up and the connection is made by using wire, the solder bumped die in flip-chip BGA is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

In this application note, guidelines on board design rules as well as board assembly parameters, rework process, and thermal management will be discussed. Note that the reflow and rework guidelines contained in this application note are applicable to eutectic packages only. For reflow and rework guidelines on Pb-free packages, refer to *Implementation and Solder Reflow Guidelines for Pb-Free Packages* (XAPP427) [Ref 1].

Introduction

Xilinx flip-chip packages are assembled on high-density, multi-layer organic laminate substrates. These packages are used exclusively in high performance products and hence it is critical that the users know how to manage the implementation of flip-chip BGA packages to prevent costly replacements.

Package Construction

Figure 1, Figure 2, Figure 3, and Figure 4 show cross-sectional views (through the center of the die) of the package construction. Note that two types of lids are used to assemble flip-chip BGA packages, forged lids (see Figure 1) and stamped lids (see Figure 2). Two variations of packages without lids are also used, bare-die packages (see Figure 3) and lidless packages that incorporate a stiffener ring (see Figure 4).

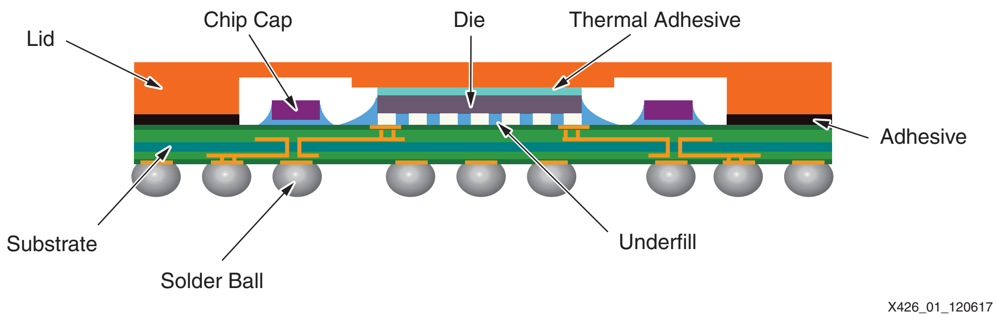

Figure 1: **Package Construction with Forged Lid**

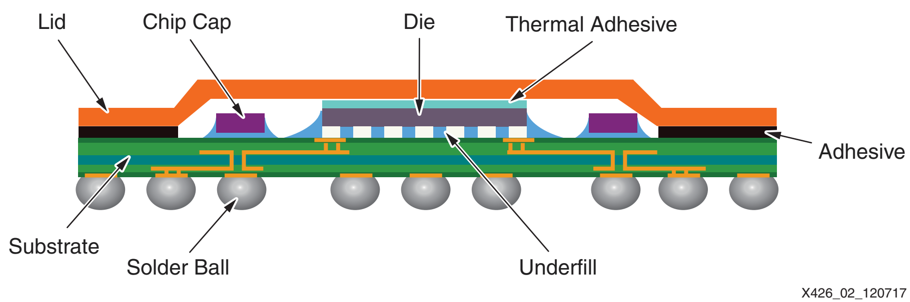

Figure 2: **Package Construction with Stamped Lid**

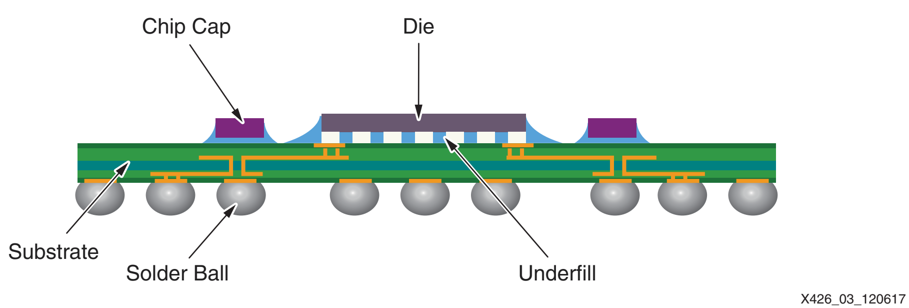

Figure 3: **Bare-Die Package Construction**

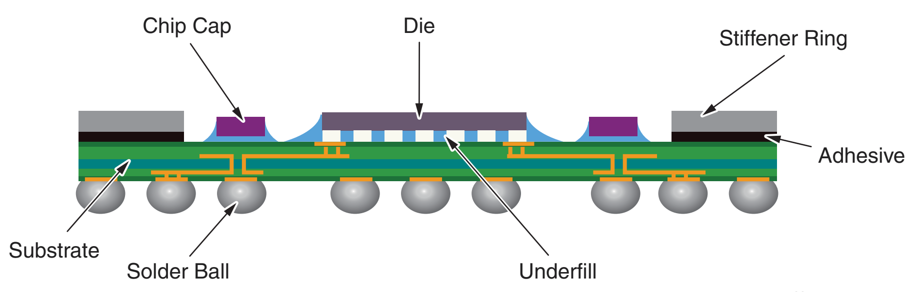

Figure 4: **Lidless Package Construction**

Xilinx flip-chip packages are not hermetically sealed and have vent holes between the edge of the package substrate and lid (see Figure 5). Vent holes are areas in the package substrate where no adhesive epoxy is dispensed. The vent holes leave a small gap between the lid and package substrate. These vent holes are kept by design between the heat spreader (lid) and the package substrate to allow for outgassing and moisture evaporation.

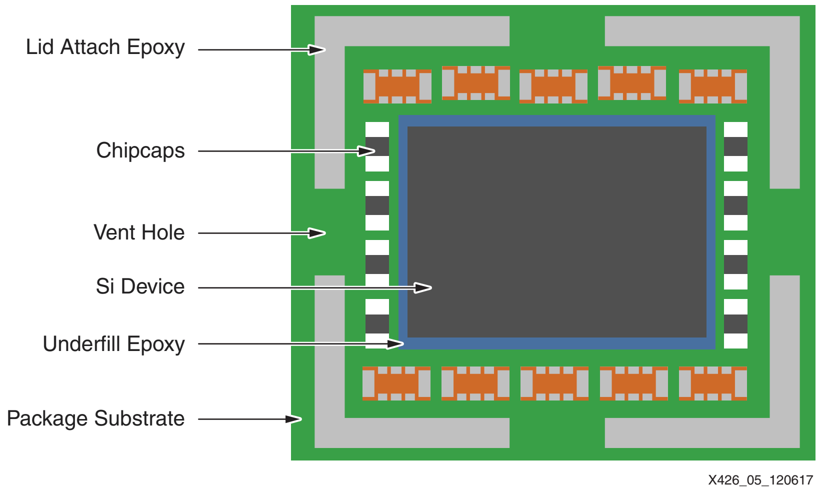

Figure 5: **Example of Vent Holes and Chip Capacitors (Package Dependent)**

Recommended PCB Reliability Guidelines

Xilinx flip-chip packages are not hermetically sealed and exposure/incomplete removal of cleaning solvents/ chemicals or excessive moisture during board assembly could pose serious package reliability concerns. The small vent holes are kept by design between the heat spreader (lid) and the package substrate to allow for outgassing and moisture evaporation. Solvents or other corrosive chemicals could seep through these vents and corrode the organic materials and components inside the package and hence are strongly discouraged during board assembly of Xilinx flip-chip BGA packages.

Recommended PCB Design Rules

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure 6 and summarized in Table 1 for 0.5, 0.8, 1.0, and 1.27 mm pitch packages. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 6. An example of an NSMD PCB pad solder joint is shown in Figure 7. It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

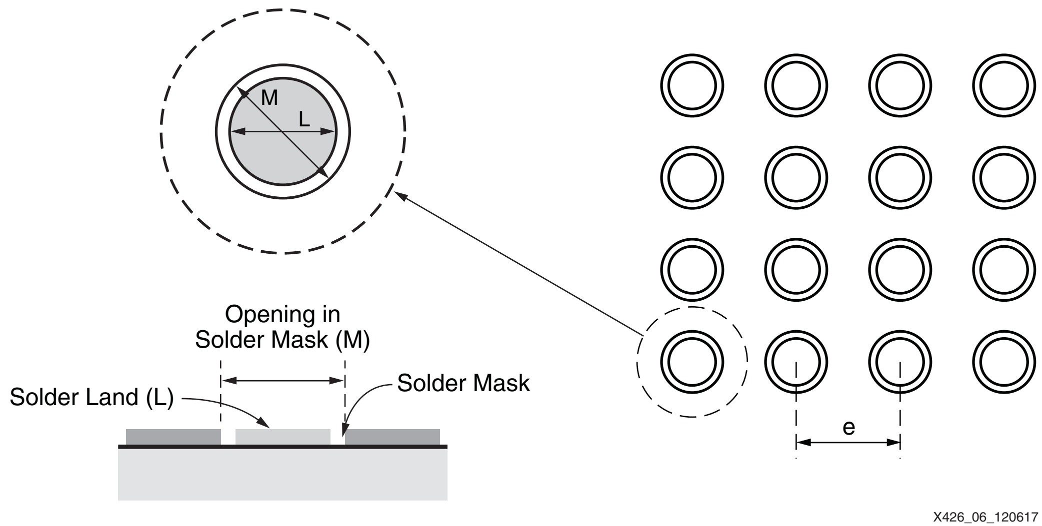

Figure 6: **Suggested Board Layout of Soldered Pads for BGA**

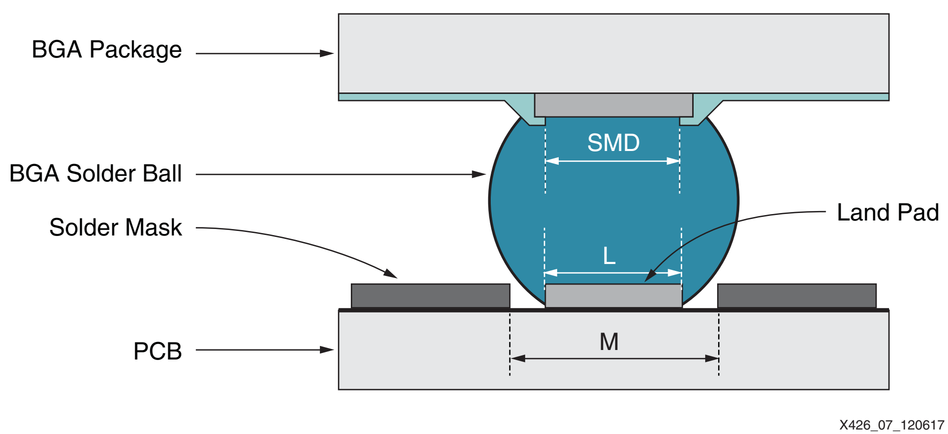

Figure 7: **Example of an NSMD PCB Pad Solder Joint**

Table 1: **BGA Package Design Rules**

Design Rule	0.5 mm Pitch	0.8 mm Pitch	1.0 mm Pitch	1.0 mm Pitch (FG Packages)	1.0 mm Pitch (FT Packages)	1.27 mm Pitch
	Dimensions in mm (mils)					
Package land pad opening (SMD)	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)	0.61 mm (24.0 mils)
Maximum PCB solder land (L) diameter	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)	0.56 mm (22.0 mils)
Opening in PCB solder mask (M) diameter	0.375 mm (14.76 mils)	0.50 mm (19.7 mils)	0.63 mm (24.8 mils)	0.60 mm (23.6 mils)	0.50 mm (19.7 mils)	0.66 mm (26.0 mils)
Solder ball land pitch (e)	0.50 mm (19.7 mils)	0.80 mm (31.5 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)	1.27 mm (50.0 mils)

Notes:

1. Controlling dimension in mm.

Assembling Flip-Chip BGAs

The Xilinx flip-chip BGAs conform to JEDEC body sizes and footprint standards. These packages follow the EIA moisture level classification for plastic surface mount components (PSMC). Standard surface mount assembly process should be used with consideration for the slightly higher thermal mass for these packages.

Like other SMT components, flip-chip BGA assembly involves the process of screen printing, solder reflow, and post reflow washing. The following will serve as a guideline on how to assemble flip-chip BGAs onto PCBs.

Screen Printing Machine Parameters

Below is an example of the parameters that were used for the screen printing process. Note that these may not be optimized parameters. Optimized parameters may depend on your applications and setup.

- Equipment: MPM Ultraprint 2000
- Squeegee Type: Metal
- Squeegee Angle: 45°
- Squeegee Pressure: 24 lbs/sq. in.
- Squeegee Speed: 0.7 in/sec
- Print Cycle: One pass
- Stencil Snap Off: 0.10 inches
- Stencil Lift Off Speed: Slow

Screen Printing Process Parameters

- Solder Paste: Alpha Metals WS609 (Water Soluble)
- Stencil Aperture: 0.0177 inches Diameter
- Stencil Thickness: 0.006 inches
- Aperture Creation: Laser cut

It is highly recommended to use either a no-clean solder paste or a water soluble solder paste. If cleaning is required, then a water soluble solder paste should be used.

Reflow Profiling

An optimized profile is paramount in achieving successful reflow results. A good starting point is to refer to the solder paste manufacturer's suggested reflow profile. However, solder paste manufacturers only supply the basic time/temperature duration information. To get an optimized reflow, components and board characteristics should dictate the maximum temperature and proper ramp rate.

Profiles should be established for all new board designs using thermocouples at multiple locations on the component (top, bottom, and corners — see Figure 11 in the Appendix). In addition, if there are mixture of devices on the board, then the profile should be checked at different locations on the board to ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that may damage the smaller, heat sensitive components. The minimum reflow temperature is the ideal thermal level at which the solder balls can be wet to form the solder joints.

The solder paste manufacturers usually provide this information and it is typically 15-20°C above the solder's melting point. For eutectic (Sn63Pb37) solder, it is around 205-215°C and for Pb-free solder, it is around 230°C to 245°C.

It is critical to keep the temperature gradient across the board as minimal as possible (maintain less than 10°C) to prevent warpage of the components and the board. This is accomplished by using a slower rate in the warm-up and preheating stages. A heating rate of less than 1°C/sec during the initial stage, in combination with a heating rate of not more than 3°C/sec throughout the rest of the profile is recommended.

Aside from the board, it is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cool down phase. In fact, cooling is a crucial part of the reflow process and must be optimized accordingly. While a slow cooling rate may result in high assembly yields, it could lead to formation of thick intermetallic layers with large grain size; thereby, reducing the solder joint strength. On the other hand, faster cooling rate leads to smaller solder joint grain size and hence resulting in higher solder joint fatigue resistance. However, overly aggressive cooling on stiff packages with large thermal mass such as flip-chip BGAs may lead to cracking or package warpage, caused by the differential cooling effects between the top surface and bottom side of the component and between the component and the PCB materials.

The key is to have an optimized cooling with minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder joint area should be as minimal as possible, preferably below 7°C during the critical region of the cool down phase of the reflow process. This critical region occurs at the phase in which the balls are not completely solidified to the board yet, usually between the 180°C and down to 160°C range. The best solution may be to divide the cooling section into multiple zones, with each zone operating at different temperatures to efficiently cool the parts. For a graphical representation of the typical reflow conditions for BGA, see Figure 12 in the appendix.

Post Reflow Cleaning/Washing

Most major PCB assembly subcontractors today have successfully developed the no-clean process in which post assembly washing is not required. That would be an ideal process. If cleaning is required as part of the process, then it is recommended to use a water soluble paste and then wash with deionized water in a washer, such as a Westek Triton IV at 140°F-145°F.

Cleaning solutions or solvents are not recommended as some cleaning solutions may contain chemicals that could corrode the heat spreader adhesive, thermal interface material, or the components inside the package.

Post Reflow Baking

Dry bake after cleaning processes are highly recommended to avoid fluid accumulation. Typical conditions used are 125°C for 4–6 hours. These are guidelines only and best manufacturing practices should always be used.

Reworking Flip-Chip BGAs

Devices packaged in a flip-chip BGA package are typically high performance and high priced devices and it is essential that proper procedures are followed for successful rework.

Prebaking

As the printed circuit board and the BGA packages are quite moisture sensitive, one should always bake the PCBs and the BGA devices prior to any rework operations. The recommended temperature and duration is 125°C for at least four hours.

BGA Removal

An accurate thermal profile needs to be established for the component removal process. This will determine the exposure duration and the maximum component/board temperatures.The profile should be adapted to each board and component to be removed. Although the typical profile should provide a peak temperature between 205 to 215°C or 230°C to 245°C for Pb-free (at the solder joint), for a maximum of 75 seconds, it is best, however, to consult with equipment manufacturer for the recommended profile.

Research has also indicated that a short delta T and a short dwell time above 183°C are preferred to minimize intermetallic growth and control board warpage. Also of importance is a need to assure that the component and the board are not overheated, and that all balls are reflowed on the specific component being removed. In general, preheat the entire board to a minimum of 85°C to avoid large temperature differentials and potential board warpage.

In terms of the equipment and tools available, automatic hot gas rework systems with vacuum suction are recommended. The nozzle should be designed such that most of the heat is applied at the solder joint area and not on the package. Excess heat can cause the lid attach epoxy to soften, which can cause the lid to come off. Apply heat from the topside using the rework profile developed (ramp the temperature for 45-60 seconds with a maximum temperature between 205-215°C for eutectic and 230°C to 245°C for Pb-free). When the solder balls are fully liquidus, remove the component using a vacuum tip. Do not attempt to remove partially reflowed component from a board by prying it off, as this would likely damage the component and can cause the lid to come off.

Note: To avoid package delamination, the temperature at the top of the package must not exceed 225ºC (240ºC to 260ºC for Pb-free flip-chip BGA packages, depending on package size).

Site Preparation

The excess solder that remains on the board can be removed using a vacuum desoldering system or a soldering iron with a solder wick. Special care must be taken to avoid damaging the solder mask material and the solder pads. As a final step, alcohol may be used with a brush to clean the rework area. Allow the board to dry and inspect to ensure a clean solderable surface. The specific steps used here may be different from board to board and from company to company. As a minimum, the removal of the excess solder is an essential requirement.

Solder Paste Application

There are several options available to apply the solder paste to the component site. The BGA package itself may be screened with paste prior to placement. In addition, the site may receive solder paste with a dispensing method. Finally the application of flux to a prepared pre-tinned site can produce acceptable results in most situations.

BGA Placement and Reflow

The next step is to replace the component on the board. The replacement component should be baked prior to assembly if the component has been exposed to the environment for more than the allotted time. Place the component on the site, observing all the alignment precautions. Reflow the balls using hot air in a manner similar to the removal process. Again observe total board temperature to avoid any thermal gradients that can result in board warpage. It is recommended to heat the PCB from the underside to a given temperature (depending on the board size and properties), preferably in the 80°C-145°C range.

Heating the underside of the board can help to minimize the temperature gradient on the board.

Additionally, larger BGA components such as flip-chip BGAs are quite sensitive to heat and therefore extra precautions are necessary. It is critical to minimize the temperature gradient on the part. High temperature gradient will create thermal shock that leads to package warpage. The temperature delta between the following locations should be 7°C or less: the solder balls on the corners, the solder balls at the center of the package, and the top surface side of the package. To achieve minimal temperature gradient, a slower ramp up rate (0.5°C/sec) and a lower peak reflow temperature (200°C as measured at the solder balls) is recommended.

Additionally, cooling should be optimized to minimize the temperature differential as described under Reflow Profiling, page 6.

BGA Reballing

Xilinx does not recommend reballing. Xilinx does not guarantee structural integrity or functionality of devices that have been reballed. If reballing is necessary, no more than three reflow cycles are recommended.

Conformal Coating

Xilinx has no experience or reliability data on flip-chip BGA packages on board after exposure to conformal coating. It is recommended that the end-user should characterize the board level reliability performance of Xilinx packages before production use.

Post Assembly Handling

When assembling mechanical connectors or fixtures to the PCB, be careful not to create excessive bowing or flexing on the PCB as this might weaken or cause damage to the solder joint interfaces.

Thermal Management

All the packages can use thermal enhancements, which can range from simple airflow to schemes that can include passive as well as active heat sinks. This is particularly true for the high performance flip-chip packages where system designers have the option to further enhance the packages to handle in excess of 20 watts with arrangements that take system physical constraints into consideration.

The accompanying flip-chip thermal management chart shown in Figure 8 illustrates incremental power management schemes that can be implemented on a flip-chip package. Similar concepts can apply to other package types.

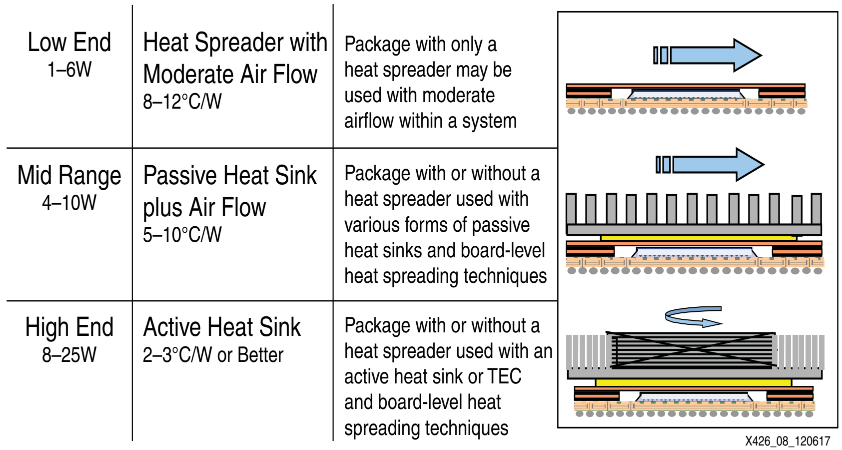

Figure 8: **Thermal Management Options for Flip-Chip BGA Packages**

For moderate power dissipation (less than 6 watts), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers can offer quick thermal solutions in these packages.

The use of lightweight finned external passive heat sinks can be effective for dissipating up to 10 watts in the bigger packages. The more efficient external heat sinks tend to be tall and heavy. To help prevent component joints from forming heat sink induced stress cracks, the use of spring loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heat sink is considered. The diagonals of some of these heat sinks may be designed with extensions to allow direct connection to the board.

All flip-chip packages offered are thermally enhanced BGAs with the die facing down. They are offered with or without exposed metal heat spreaders at the top. These are considered high-end thermal packages and they lend themselves to the application of external heat sinks (passive or active) for further heat removal efficiency. Again precaution should be taken to prevent component damage when a bulky heat sink is attached.

Active heat sinks may include simple heat sinks incorporating a mini fan or even Peltier Thermoelectric Coolers (TECs) with a fan to carry away any heat generated. Any consideration to apply TEC in heat management should require consultation with experts in using the device because these devices can be reversed and cause damage to components. Condensation can also be an issue.

Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. As much as 80% of the heat generated can go through the BGA balls and thus the board. Board designs may be implemented to take advantage of the board’s ability to spread heat. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on it.

Removing Heat Sink Phase Change Material

When removing or reworking heat sinks, the phase-change material residue must be removed from the surface of the die. Laird Technologies, Inc. provides the following guidance for complete removal of the phase-change material from the component.

Instructions for Removal of Phase Change Material

1. Separate the Components
2. Scrape Away Thick Residue
3. Clean Remaining Residue with Solvent
4. Working with Laird Material

Separate the Components

At room temperature, if possible use a back and forth twisting motion to break the bond between the phase-change thermal interface material and mated components (i.e., heat sink and FPGA). See Figure 9.

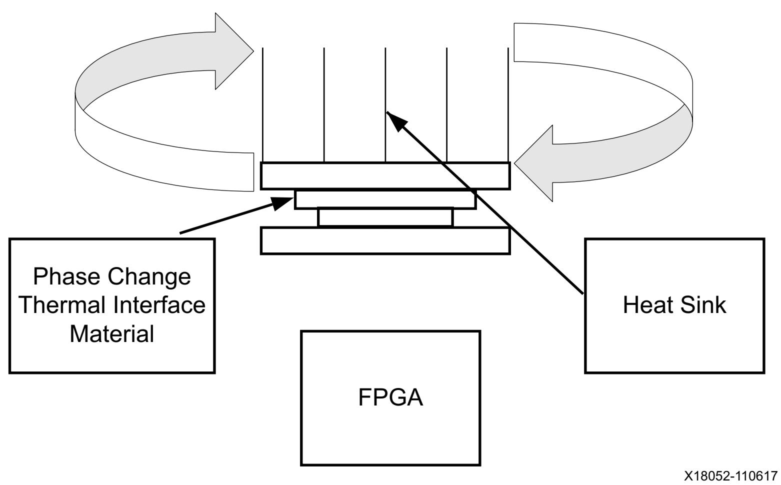

Figure 9: **Breaking the Bond between Thermal Interface Materials and Mated Components**

For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, situations where minimal movement is available, or if using fragile components, heat the component (preferred) or heat sink to about 40°C–60°C before removal.

The guideline is 40°C–60°C, however, you might find that for your application, heating to 35°C is adequate. You might prefer to heat to 70°C which makes the phase-change thermal interface material very soft and the components can be easily separated.

Scrape Away Thick Residue

For a faster clean-up after components are separated, scrape away any large residual material amounts with a plastic spatula or a wooden tongue depressor. A clean dry rag also works well to wipe away excess material.

Clean Remaining Residue with Solvent

Using a clean cloth/wipe, wet it with your choice of solvent (see the following list) and wipe away any remaining residue:

- Toluene (easiest)
- Acetone (very good)
- Isoparaffinic hydrocarbon: Isopar, Soltrol (trade names) (very good)
- Isopropyl alcohol (OK)

Working with Laird Material

Safe handling, disposal, and first aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, www.lairdtech.com.

Applied Pressure from Heat Sink to the Package through Thermal Interface Materials

Xilinx recommends that the applied pressure on the package be in the range of 20 to 40 PSI for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, because their presence degrades the thermal contact and results in incorrect thermal measurements.

Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See Figure 10.

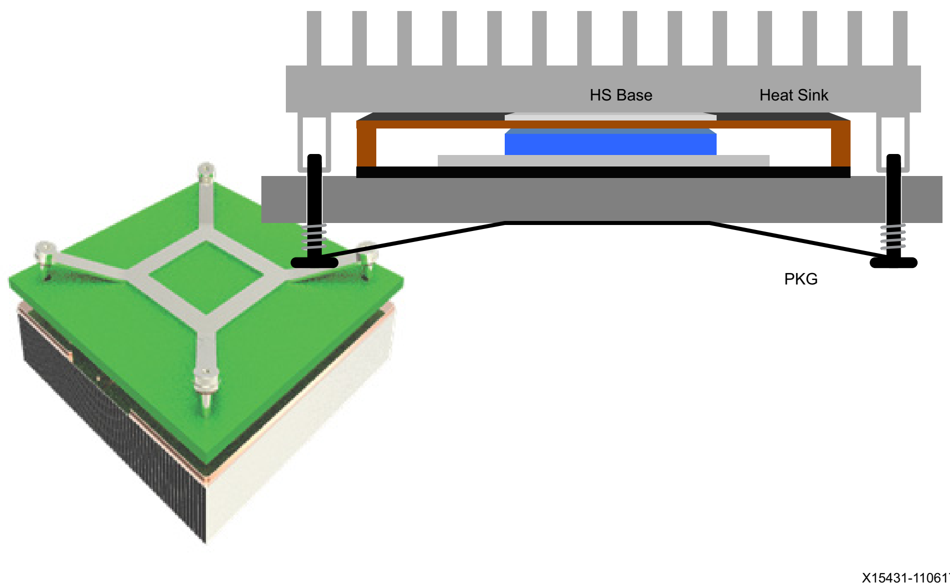

Figure 10: **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**

Appendix

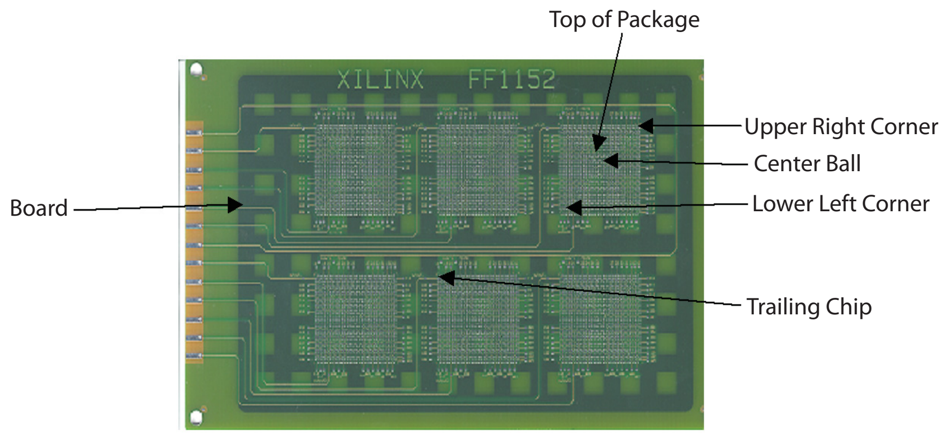

Figure 11: **Temperature Measurement Locations**

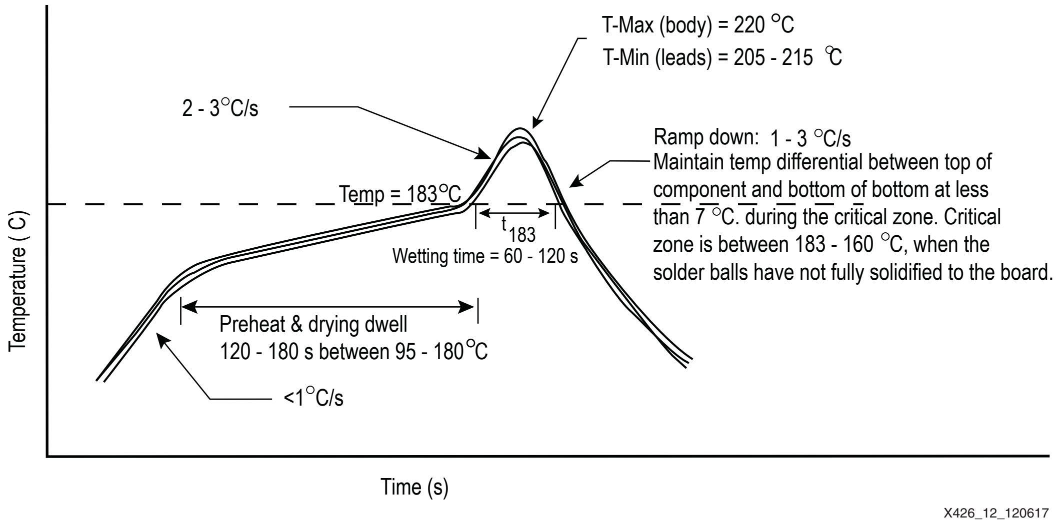

Figure 12: **Typical Solder Reflow Profile for Eutectic BGA**

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

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8. *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575)
9. *Zynq-7000 All Programmable SoC Packaging and Pinout Product Specification* (UG865)
10. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
11. *Virtex-6 FPGA Packaging and Pinout Specifications* (UG365)
12. *Spartan-6 FPGA Packaging and Pinouts Product Specification* (UG385)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/09/2002	1.0	Initial Xilinx release.
05/27/2003	1.1	Added BGA Reballing section
01/15/2004	1.2	Changed Peak Reflow Temperature from 200-210°C to 205-215°C.
03/03/2006	1.3	Included package construction with Type II Lids (Figure 2), added note about nonhermiticity and conformal coating.
04/03/2007	1.3.1	Corrected typo in document information form.
01/11/2018	1.4	Updated Package Construction section including Figure 1 and Figure 2, and added Figure 3, Figure 4, and Figure 5. Added Recommended PCB Reliability Guidelines and Post Reflow Baking sections. Updated Recommended PCB Design Rules section and Table 1. Added Figure 6 and Figure 7. Updated the Reflow Profiling, Post Reflow Cleaning/Washing, BGA Removal, and BGA Reballing sections. Updated Thermal Management section including Figure 8. Added Removing Heat Sink Phase Change Material and Applied Pressure from Heat Sink to the Package through Thermal Interface Materials sections.

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