MmcmClock

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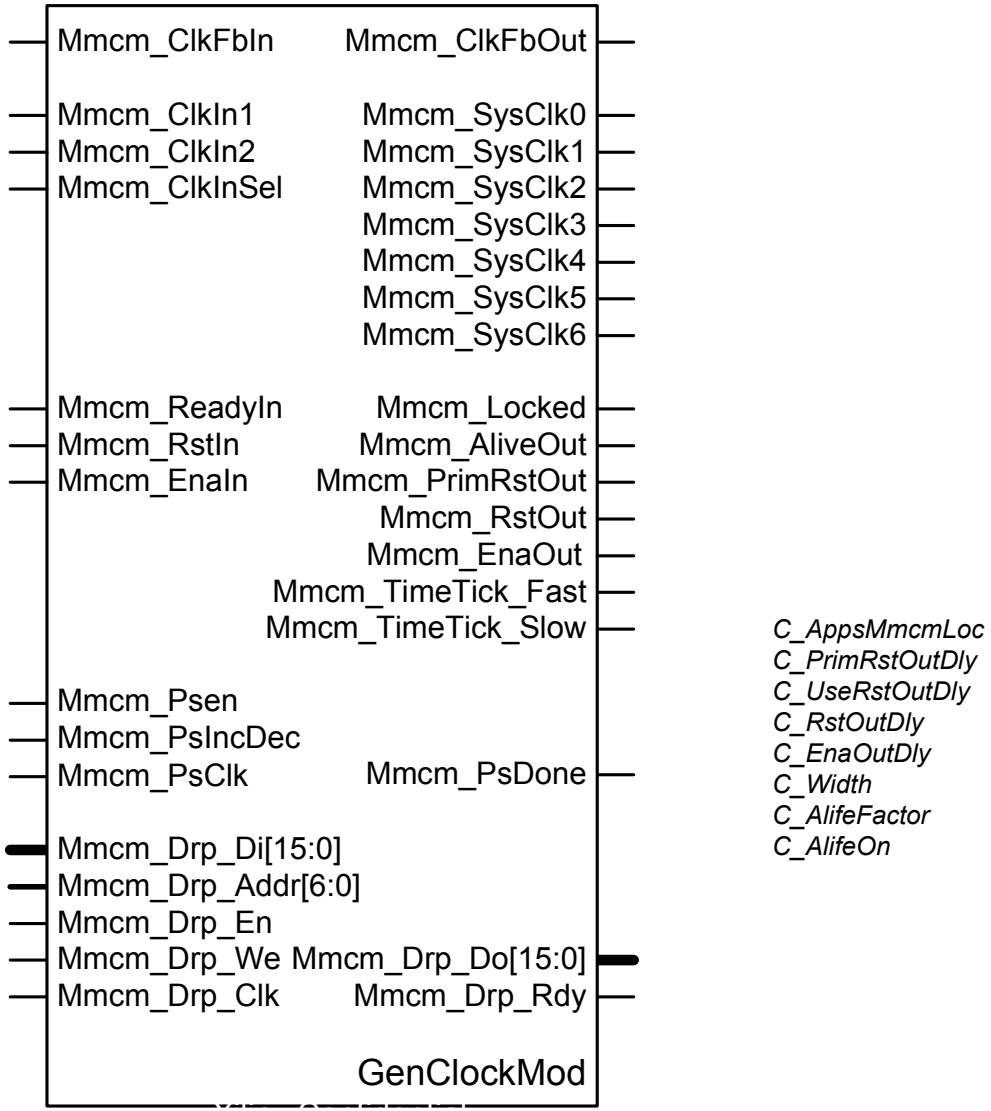
GenClockMod



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MMCM calculations

MMCM frequency calculations
Input frequency: 312.5 MHz
Component: Kintex -2

Fin_min	= 10 MHz
Fin_max	= 933 MHz
Fvco_min	= 600 MHz
Fvco_max	= 1440 MHz
Fout_min	= 4.69 Mhz
Fout_max	= 933 MHz
Fpfd_min	= 10 MHz
Fpfd_max	= 500 MHz

(Bandwidth set to High or Optimized).

Dmin = rndup Fin/Fpfd_max	=> **1** <==
Dmax = Rnddwn Fin/Fpfd_min	=> 31
Mmin = (rndup Fvco_min/Fin) * Dmin	=> 2
Mmax = rnddwn ((Dmax * Fvco_max)/Fin)	=> 142
Mideal = (Dmin * Fvco_max) / Fin	=> **4.6** <==

Fvco must be maximized for best functioning of the VCO.
For easy calculation and use, the multiply factor will be taken as a integer value close to the ideal multiplier setting the VCO frequency as high as possible.
M is taken as **4**, then Fvco is 1250 MHz (5 as M is too high, 1562.5 MHz)

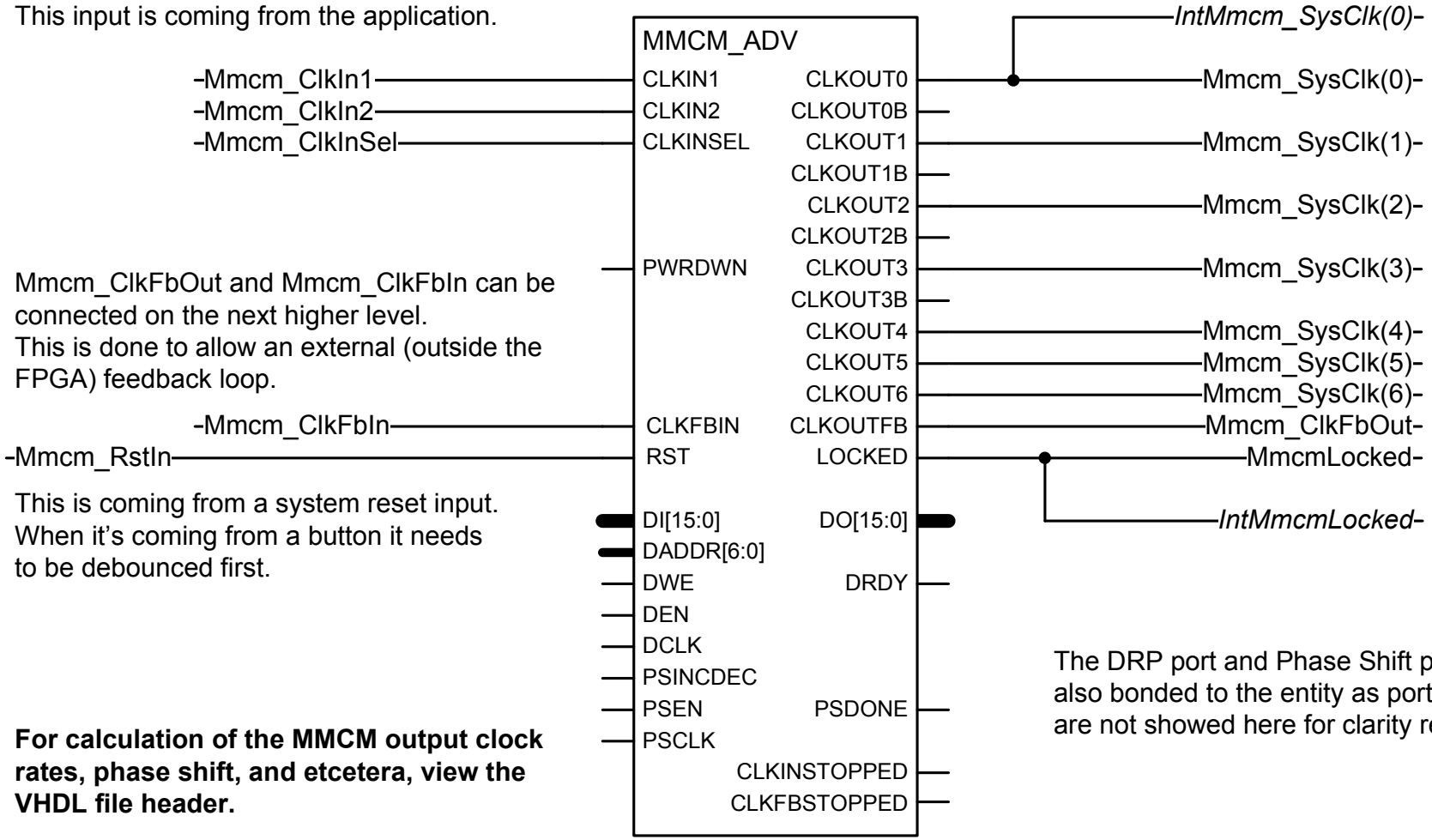
Fvco = Fin * M/D 312.5 x 4/1 => 1250
Fout = Fin * M/D*O

Fout_Clk0 => D = 4.0322	==> 310 MHz	(IDELAYCTRL)
Fout_Clk1 => D = 2	==> 625 MHz	(CLK)
Fout_Clk2 => D = 8	==> 156.25 MHz	(CLKDIV)
Fout_Clk3 => D = 4	==> 312.5 MHz	(AppsClock)
Fout_Clk4 => D = 8	==> 625 MHz	(AppsClock)
Fout_Clk5 => D = 8	|	
Fout_Clk6 => D = 8	|==> Not Used	

CLKOUT0 is used for the reference clock of the IDELAYCTRL component.
IDELAYCTRL is not needed for OSERDES but is is foreseen in case of ….
When the reference clock is set to 200 Mhz the tap delay is 78ps,
when the clock is set to 300 MHZ the tap delay is 52ps.
The clock precision must be +- 10MHz.

CLKOUT 1 and CLKOUT2 are both dedicated to the OSERDES components.
The rest of the clock outputs can be used for applications running in the FPGA fabric.

This input is coming from the application.



Mmcm_ClkFbOut and Mmcm_ClkFbIn can be connected on the next higher level.
This is done to allow an external (outside the FPGA) feedback loop.

This is coming from a system reset input. When it's coming from a button it needs to be debounced first.

For calculation of the MMCM output clock rates, phase shift, and etcetera, view the VHDL file header.

The DRP port and Phase Shift ports are also bonded to the entity as ports. They are not showed here for clarity reasons.