KC705 Used to Interface to a ADC and ADC is a Virtual Device.

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FMC connections (1)

- Only the FMC-LPC connector is used.
- The connector must be used for the ADC interface (Receiver) and for the virtual ADC (transmitter).
- The pinout fits also whenever hardware for ADC and DAC is created.
- The FMC-LPC connector is populated with IO from IO-Bank 12 and 13 on the KC705 board..

- FPGA implementation ADC interface (receiver) and Virtual ADC (transmitter) or DAC interface.

- IO-Bank 12 is used as virtual ADC or transmitter interface.
- IO-Bank 13 is used as ADC interface or receiver.

- IO-Bank 12 gets a clock from a high-speed programmable oscillator on the mezzanine board.
  - In reality, if there is a DAC, this will be the high-speed clock coming from the DAC.
- What is pinning is needed:
  - IO-Bank 12
    - A high-speed clock input ← Clock from the transmitter, in this case a clock from a programmable oscillator.
    - A high speed bit clock output.
    - A low speed, word or frame clock output.
    - LVDS lanes for data transmitter . (Most popular 8, 12, 14, or 16-bit).
  - IO-Bank 13
    - A high speed bit clock input.
    - A low speed, word or frame clock input.
    - LVDS lanes for data receiver. (Most popular 8, 12, 14, or 16-bit).

FMC Connections (2)

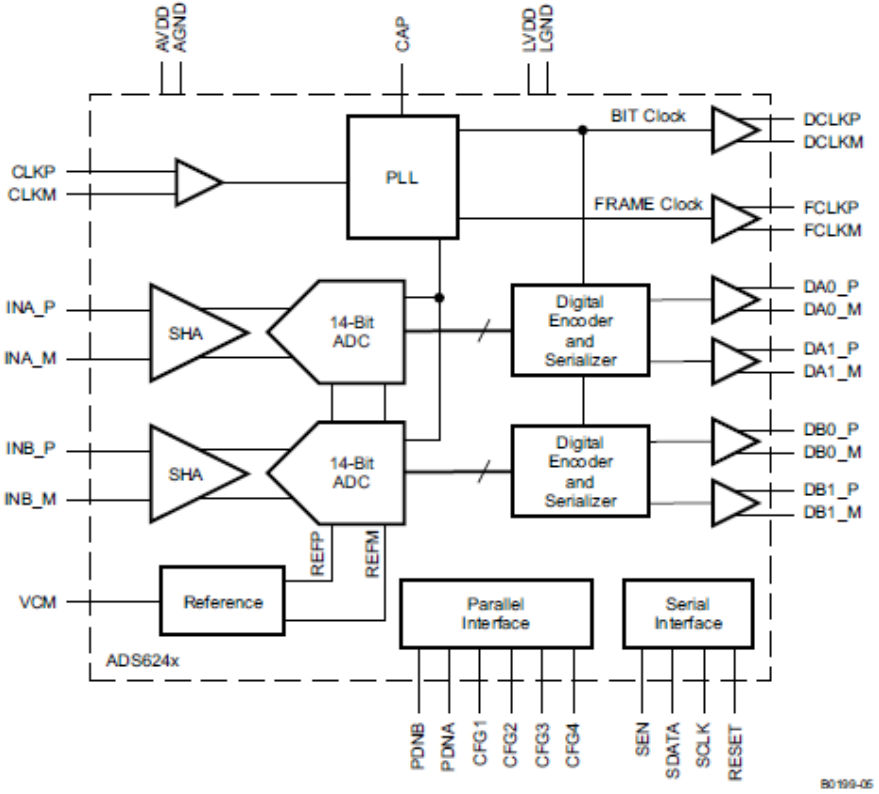
Virtual ADC.

- IO-Bank 12 is used as implementation of the digital part of an ADC (transmitter).
- Typical connections of an ADC are:
  - High speed clock (Bit clock)
  - Low speed clock (Sync or frame clock), can be seen as data.
  - A number of data channels. For ADC devices it is the number of LVDS data channels that counts.
  - Example:
    - A Dual, 2-wire ADC needs 4 LVDS data channels (+ Bit_Clk + Sync).
    - A Quad, 2-wire ADC needs 8 LVDS channels (+ Bit_Clk + Sync).

  - IO-bank 12 allows to connect:
    - Two Dual channel, 2-wire ADC
    - One Quad channel, 2-wire ADC

- For real ADC testing the FMC-HPC connector should be used to connect ADC devices.
- Because then ADC devices with different sorts of interfaces can be connected.
  - Serial LVDS ADC.
  - Full Parallel ADC
  - JESD204A multi-channels ADC.

ADC: Example for the test ADS6245



The plan is to use the Texas Instruments ADS6245 ADC device as example with the conversion of the Virtex-5 ADC interface. This Texas Instruments ADC is used because it has a small set of data channels and this makes it easier to debug the conversion of the design.
The goal is to interface to the more popular Quad channel ADC of this family.

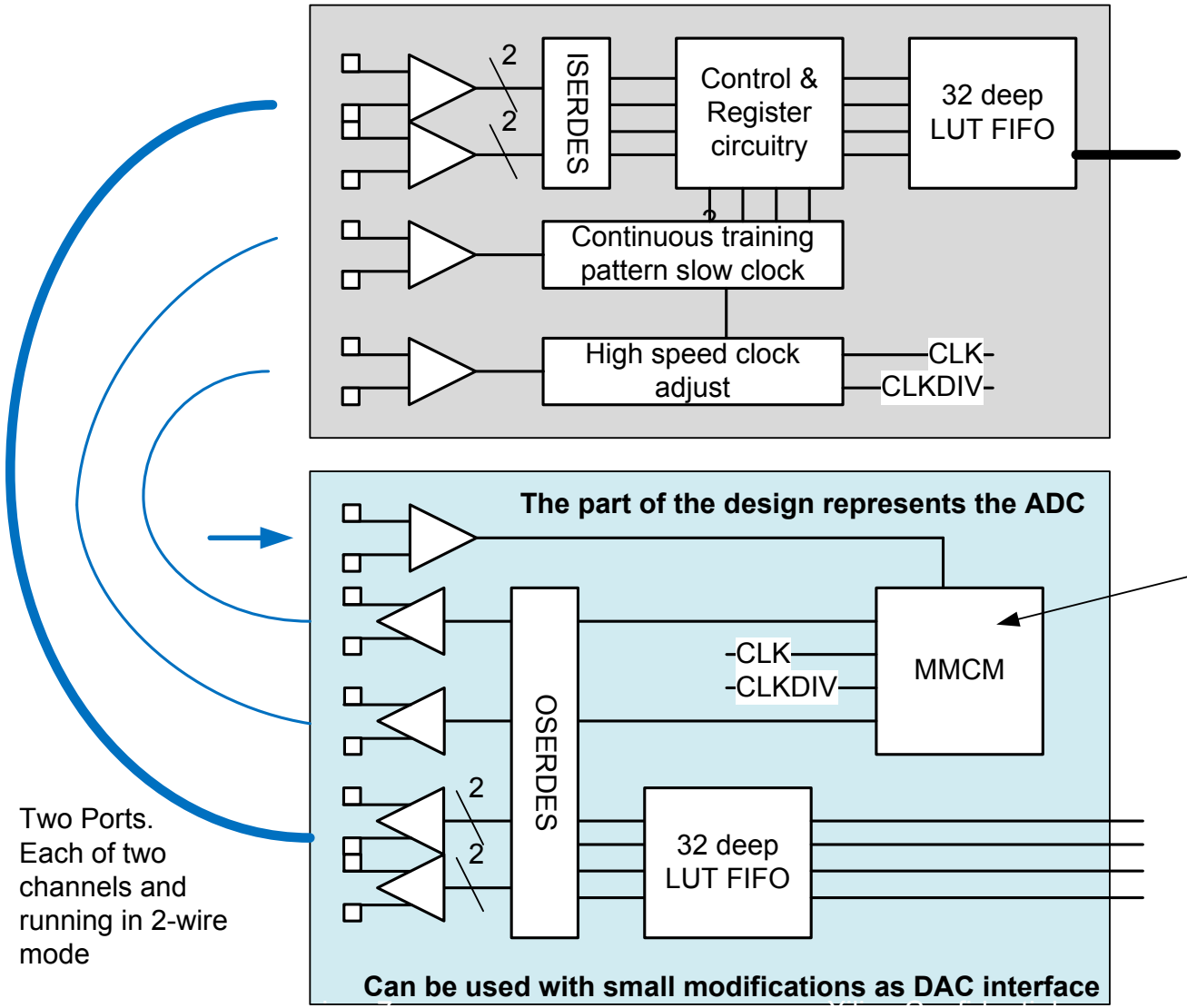
Dual 14-bit, 125 MSPS ADC with serial LVDS outputs.

The ADC is used in:

- 2-wire
- Byte wise
- MSB first
- DDR bit clock
- 16x serialisation

Mode.

RX and TX Interfaces



The MMCM has an IO available for an external feedback loop. The loop can go to the ADC part of the design an be looped-back there. This is not shown here.

Two Ports. Each of two channels and running in 2-wire mode

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FMC – LPC connector pinout

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

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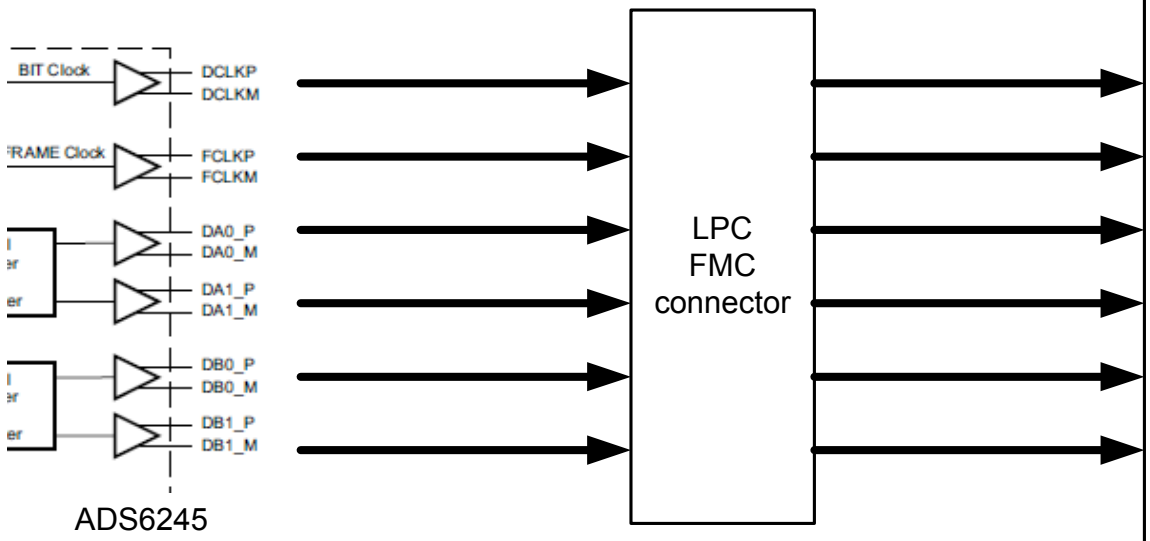
ADC (ADS6245) interface (receiver).

The ADS6245 is cooked into the FPGA and functions as Virtual ADC



The FPGA on the KC705 board is a 7KC325T-2-FFG900.

See next pages for the FMC connector pinout and for the FPGA pinout.

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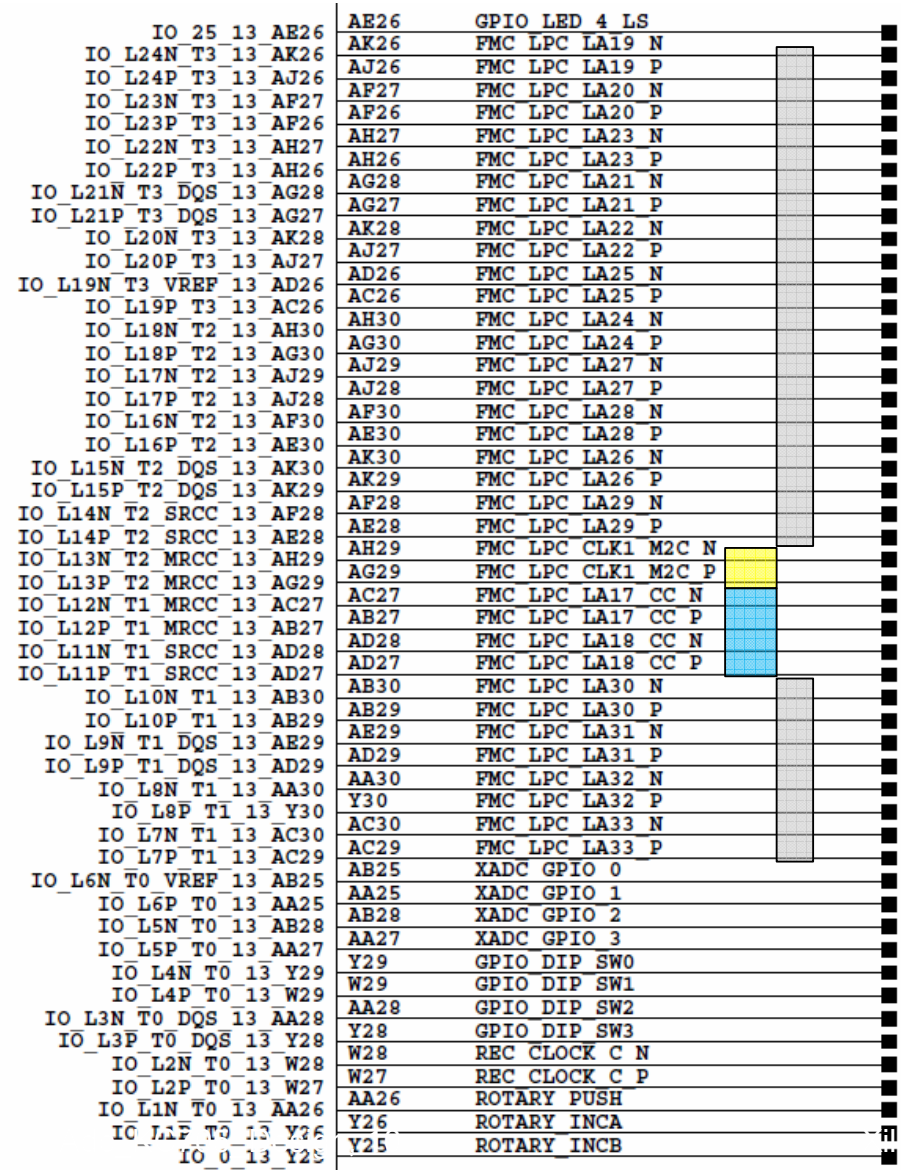
ADC Interface

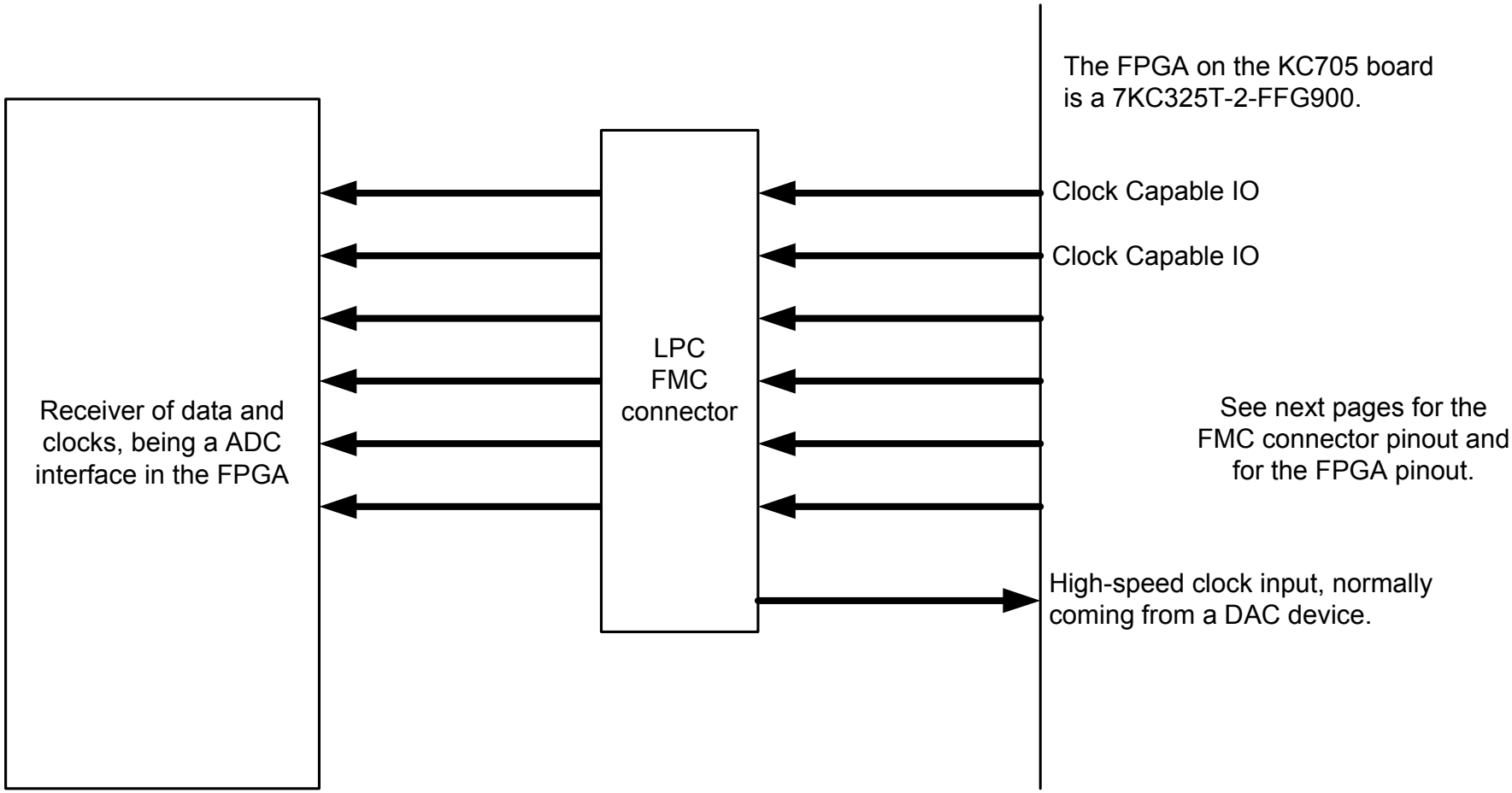


By design of the KC705 board the FPGA (7KC325T-FFG900) IO-Bank 12 and IO-Bank 13 are used for the LPC FMC connector.

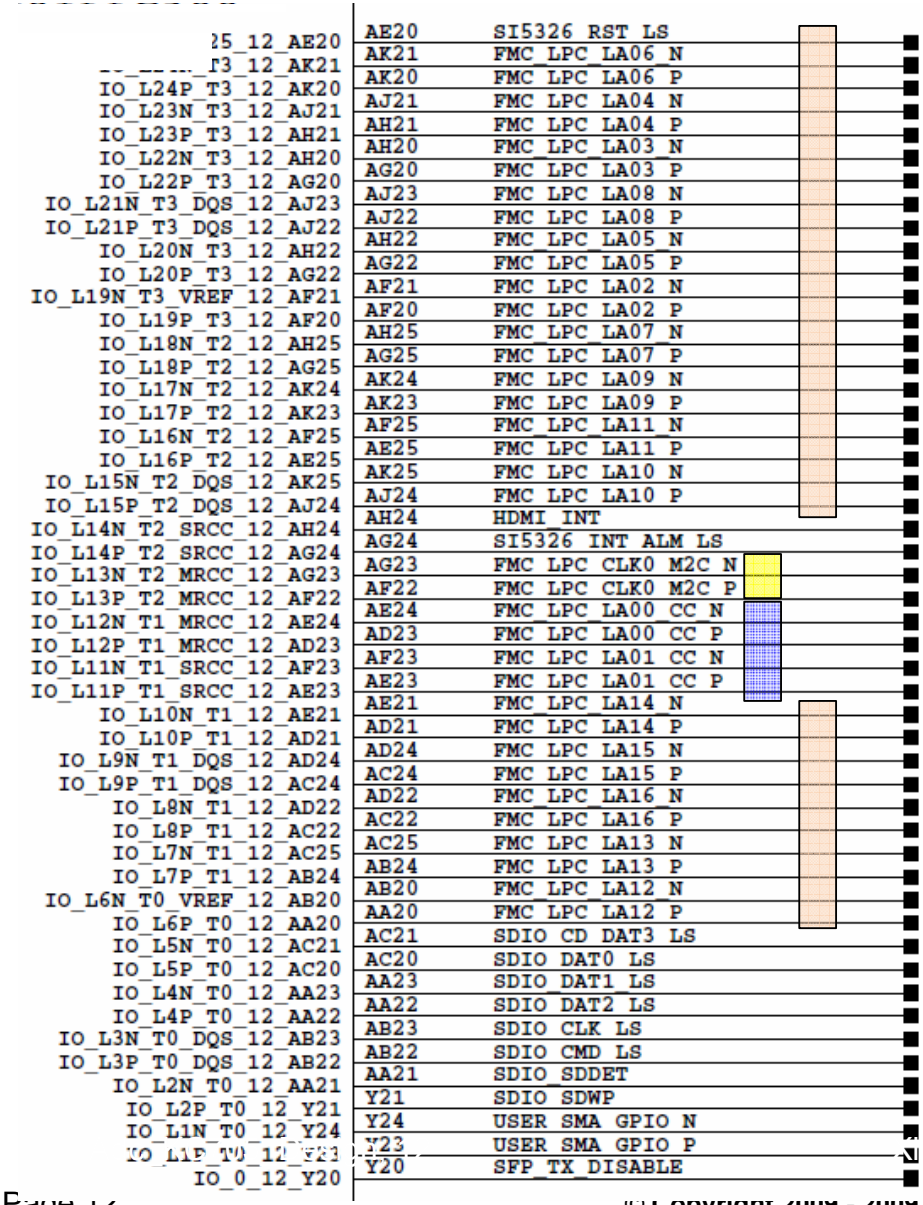
The FMC-LPC connector setup of the KC705 board dictates that for IO-Bank 12 this setup is possible:

- High-speed clock output.
- Bit clock (High Speed) and Frame/Sync (Low Speed) clock inputs.
- Data inputs.

FPGA Virtual ADC



Virtual ADC pinout.



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The FMC-LPC connector setup of the KC705 board dictates that for IO-Bank 13 this setup is possible:

- High-speed clock input.
- Bit clock (High Speed) and Frame/Sync (Low Speed) clock outputs.
- Data outputs.

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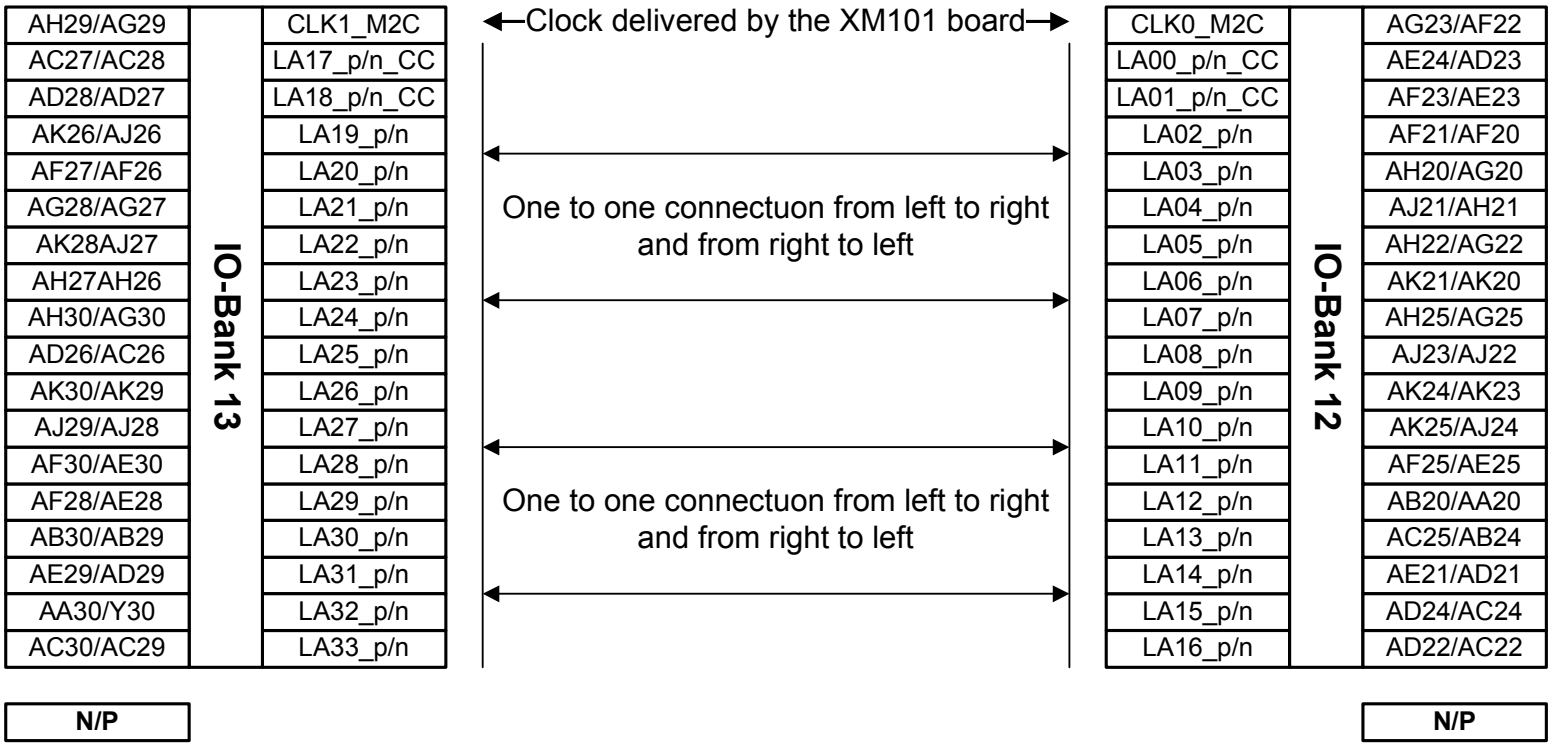
FPGA LPC IO-Banks 12 and 13 connected via cable

As shown on page 7 the transmitter, Virual ADC, will be connected to the receiver, ADC interface in the FPGA.
This holds that IO-Bank 12 is connected to IO-Bank 13 by means of a XM101 board plugged into the LPC FMC connector of the KC705 board.
This slide shows the interconnections via the XM101 board between the IO-Banks.



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The DAC (Transmitter)