



# KC705 Used to Interface to a ADC and ADC is a Virtual Device.

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# FMC connections (1)

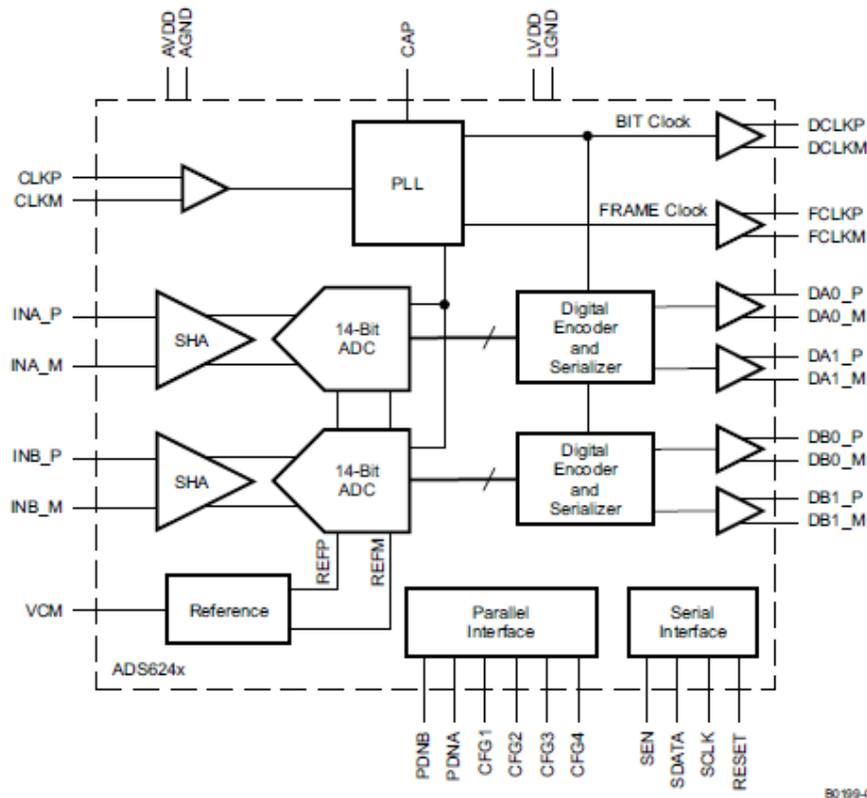
- Only the FMC-LPC connector is used.
- The connector must be used for the ADC interface (Receiver) and for the virtual ADC (transmitter).
- The pinout fits also whenever hardware for ADC and DAC is created.
- The FMC-LPC connector is populated with IO from IO-Bank 12 and 13 on the KC705 board..
- **FPGA implementation ADC interface (receiver) and Virtual ADC (transmitter) or DAC interface.**
  - IO-Bank 12 is used as virtual ADC or transmitter interface.
  - IO-Bank 13 is used as ADC interface or receiver.
- IO-Bank 12 gets a clock from a high-speed programmable oscillator on the mezzanine board.
  - In reality, if there is a DAC, this will be the high-speed clock coming from the DAC.
- What is pinning is needed:
  - IO-Bank 12
    - A high-speed clock input ← Clock from the transmitter, in this case a clock from a programmable oscillator.
    - A high speed bit clock output.
    - A low speed, word or frame clock output.
    - LVDS lanes for data transmitter . (Most popular 8, 12, 14, or 16-bit).
  - IO-Bank 13
    - A high speed bit clock input.
    - A low speed, word or frame clock input.
    - LVDS lanes for data receiver. (Most popular 8, 12, 14, or 16-bit).

# FMC Connections (2)

## Virtual ADC.

- IO-Bank 12 is used as implementation of the digital part of an ADC (transmitter).
- Typical connections of an ADC are:
  - High speed clock (Bit clock)
  - Low speed clock (Sync or frame clock), can be seen as data.
  - A number of data channels. For ADC devices it is the number of LVDS data channels that counts.
  - Example:
    - A Dual, 2-wire ADC needs 4 LVDS data channels (+ Bit\_Clk + Sync).
    - A Quad, 2-wire ADC needs 8 LVDS channels (+ Bit\_Clk + Sync).
- IO-bank 12 allows to connect:
  - Two Dual channel, 2-wire ADC
  - One Quad channel, 2-wire ADC
- For real ADC testing the FMC-HPC connector should be used to connect ADC devices.
- Because then ADC devices with different sorts of interfaces can be connected.
  - Serial LVDS ADC.
  - Full Parallel ADC
  - JESD204A multi-channels ADC.

# ADC: Example for the test ADS6245



The plan is to use the Texas Instruments ADS6245 ADC device as example with the conversion of the Virtex-5 ADC interface. This Texas Instruments ADC is used because it has a small set of data channels and this makes it easier to debug the conversion of the design. The goal is to interface to the more popular Quad channel ADC of this family.

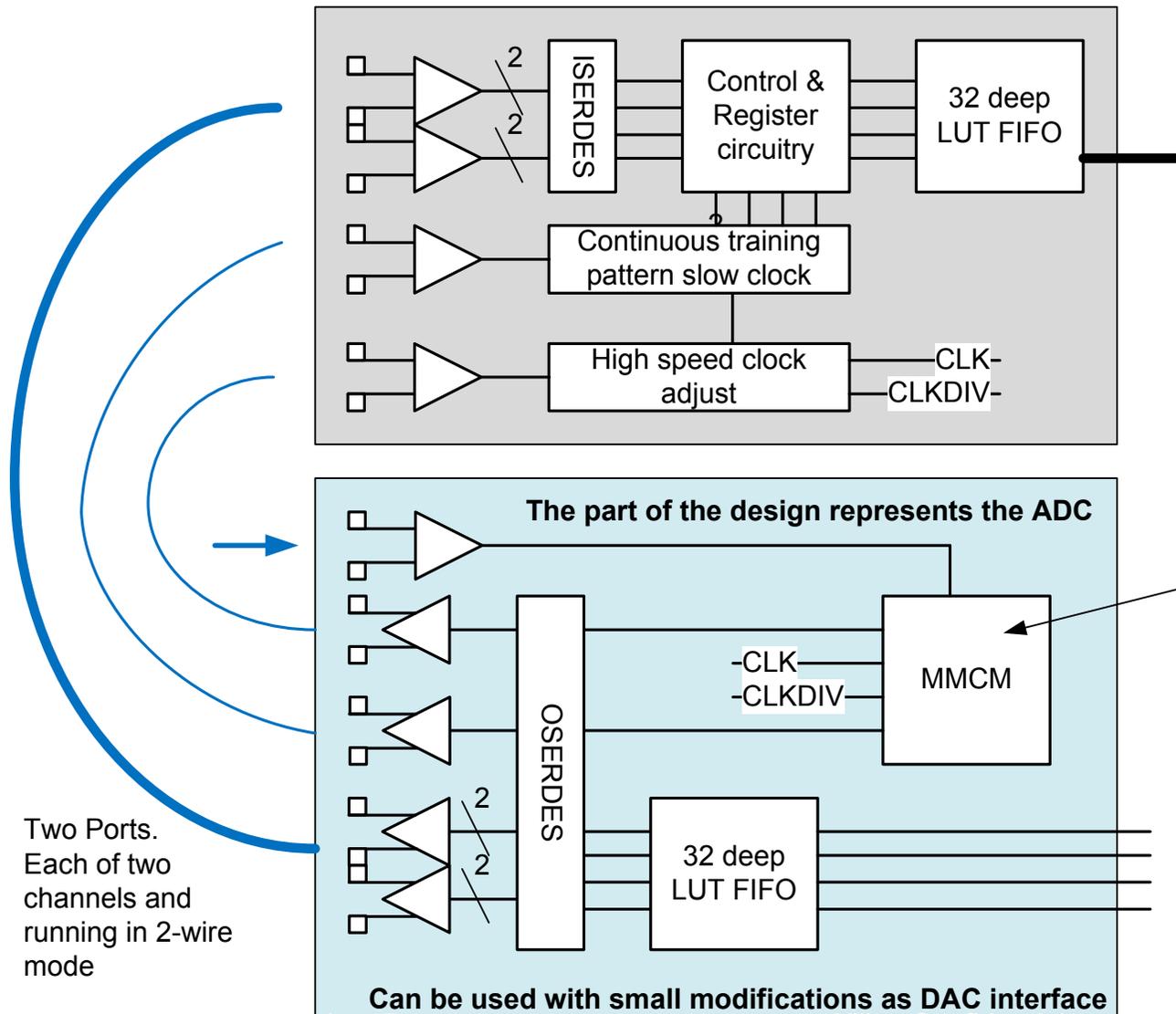
Dual 14-bit, 125 MSPS ADC with serial LVDS outputs.

The ADC is used in:

- 2-wire
- Byte wise
- MSB first
- DDR bit clock
- 16x serialisation

Mode.

# RX and TX Interfaces



The MMCM has an IO available for an external feedback loop. The loop can go to the ADC part of the design and be looped-back there. This is not shown here.

Two Ports.  
Each of two  
channels and  
running in 2-wire  
mode

# FMC – LPC connector pinout

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF A M2C	GND	NC	NC	PG C2M	GND	NC	NC
2	NC	NC	PRSNT M2C L	CLK1 M2C P	NC	NC	GND	DP0 C2M P	NC	NC
3	NC	NC	GND	CLK1 M2C N	NC	NC	GND	DP0 C2M N	NC	NC
4	NC	NC	CLK0 M2C P	GND	NC	NC	GBTCLK0 M2C P	GND	NC	NC
5	NC	NC	CLK0 M2C N	GND	NC	NC	GBTCLK0 M2C N	GND	NC	NC
6	NC	NC	GND	LA00 P CC	NC	NC	GND	DP0 M2C P	NC	NC
7	NC	NC	LA02 P	LA00 N CC	NC	NC	GND	DP0 M2C N	NC	NC
8	NC	NC	LA02 N	GND	NC	NC	LA01 P CC	GND	NC	NC
9	NC	NC	GND	LA03 P	NC	NC	LA01 N CC	GND	NC	NC
10	NC	NC	LA04 P	LA03 N	NC	NC	GND	LA06 P	NC	NC
11	NC	NC	LA04 N	GND	NC	NC	LA05 P	LA06 N	NC	NC
12	NC	NC	GND	LA08 P	NC	NC	LA05 N	GND	NC	NC
13	NC	NC	LA07 P	LA08 N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07 N	GND	NC	NC	LA09 P	LA10 P	NC	NC
15	NC	NC	GND	LA12 P	NC	NC	LA09 N	LA10 N	NC	NC
16	NC	NC	LA11 P	LA12 N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11 N	GND	NC	NC	LA13 P	GND	NC	NC
18	NC	NC	GND	LA16 P	NC	NC	LA13 N	LA14 P	NC	NC
19	NC	NC	LA15 P	LA16 N	NC	NC	GND	LA14 N	NC	NC
20	NC	NC	LA15 N	GND	NC	NC	LA17 P CC	GND	NC	NC
21	NC	NC	GND	LA20 P	NC	NC	LA17 N CC	GND	NC	NC
22	NC	NC	LA19 P	LA20 N	NC	NC	GND	LA18 P CC	NC	NC
23	NC	NC	LA19 N	GND	NC	NC	LA23 P	LA18 N CC	NC	NC
24	NC	NC	GND	LA22 P	NC	NC	LA23 N	GND	NC	NC
25	NC	NC	LA21 P	LA22 N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21 N	GND	NC	NC	LA26 P	LA27 P	NC	NC
27	NC	NC	GND	LA25 P	NC	NC	LA26 N	LA27 N	NC	NC
28	NC	NC	LA24 P	LA25 N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24 N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29 P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28 P	LA29 N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28 N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31 P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30 P	LA31 N	NC	NC	TRST L	GA0	NC	NC
35	NC	NC	LA30 N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33 P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32 P	LA33 N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32 N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

LPC Connector

LPC Connector

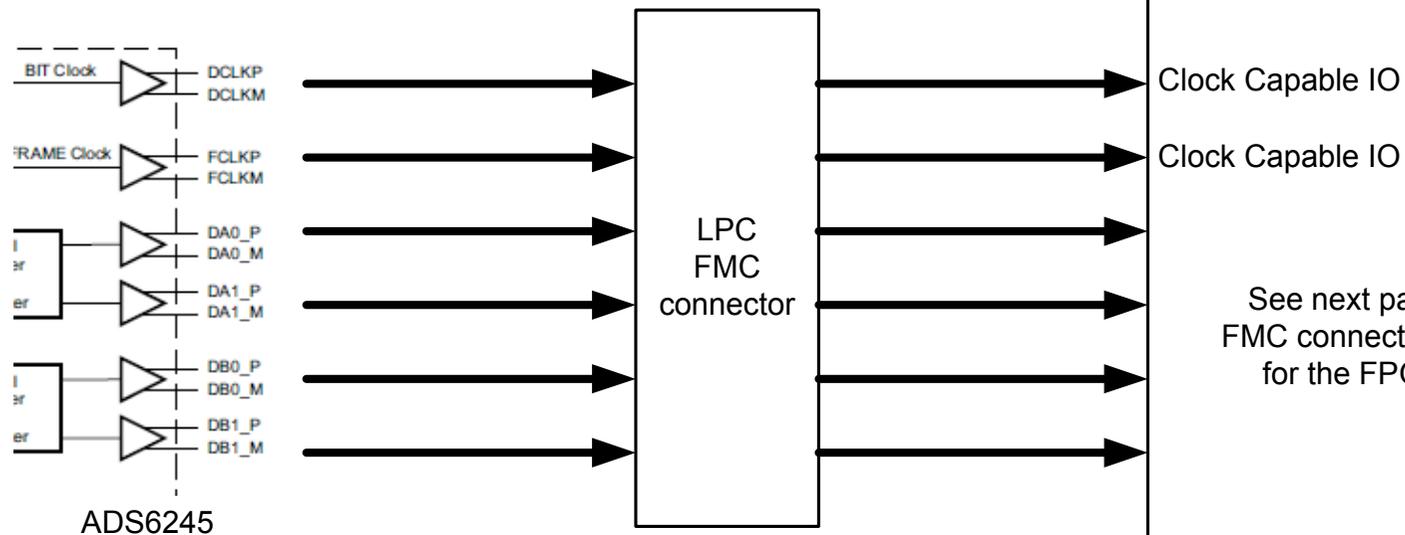
LPC Connector

LPC Connector

# ADC (ADS6245) interface (receiver).

The ADS6245 is cooked into the FPGA and functions as Virtual ADC

The FPGA on the KC705 board is a 7KC325T-2-FFG900.



See next pages for the FMC connector pinout and for the FPGA pinout.

# ADC Interface

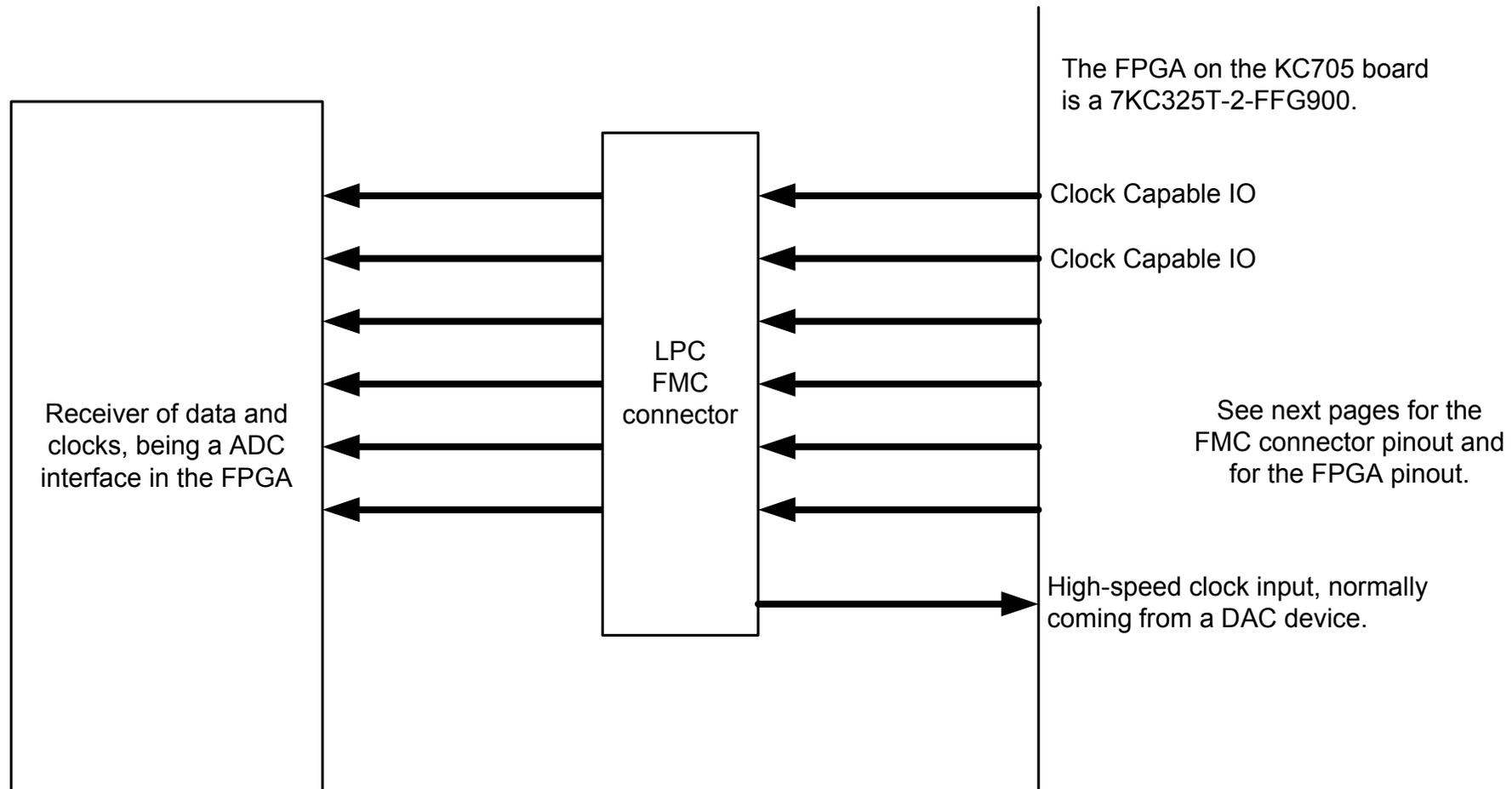
IO_25_T3_13_AE26	AE26	GPIO LED 4 LS
IO_L24N_T3_13_AK26	AK26	FMC LPC LA19 N
IO_L24P_T3_13_AJ26	AJ26	FMC LPC LA19 P
IO_L23N_T3_13_AF27	AF27	FMC LPC LA20 N
IO_L23P_T3_13_AF26	AF26	FMC LPC LA20 P
IO_L22N_T3_13_AH27	AH27	FMC LPC LA23 N
IO_L22P_T3_13_AH26	AH26	FMC LPC LA23 P
IO_L21N_T3_DQS_13_AG28	AG28	FMC LPC LA21 N
IO_L21P_T3_DQS_13_AG27	AG27	FMC LPC LA21 P
IO_L20N_T3_13_AK28	AK28	FMC LPC LA22 N
IO_L20P_T3_13_AJ27	AJ27	FMC LPC LA22 P
IO_L19N_T3_VREF_13_AD26	AD26	FMC LPC LA25 N
IO_L19P_T3_13_AC26	AC26	FMC LPC LA25 P
IO_L18N_T2_13_AH30	AH30	FMC LPC LA24 N
IO_L18P_T2_13_AG30	AG30	FMC LPC LA24 P
IO_L17N_T2_13_AJ29	AJ29	FMC LPC LA27 N
IO_L17P_T2_13_AJ28	AJ28	FMC LPC LA27 P
IO_L16N_T2_13_AF30	AF30	FMC LPC LA28 N
IO_L16P_T2_13_AE30	AE30	FMC LPC LA28 P
IO_L15N_T2_DQS_13_AK30	AK30	FMC LPC LA26 N
IO_L15P_T2_DQS_13_AK29	AK29	FMC LPC LA26 P
IO_L14N_T2_SRCC_13_AF28	AF28	FMC LPC LA29 N
IO_L14P_T2_SRCC_13_AE28	AE28	FMC LPC LA29 P
IO_L13N_T2_MRCC_13_AH29	AH29	FMC LPC CLK1 M2C N
IO_L13P_T2_MRCC_13_AG29	AG29	FMC LPC CLK1 M2C P
IO_L12N_T1_MRCC_13_AC27	AC27	FMC LPC LA17 CC N
IO_L12P_T1_MRCC_13_AB27	AB27	FMC LPC LA17 CC P
IO_L11N_T1_SRCC_13_AD28	AD28	FMC LPC LA18 CC N
IO_L11P_T1_SRCC_13_AD27	AD27	FMC LPC LA18 CC P
IO_L10N_T1_13_AB30	AB30	FMC LPC LA30 N
IO_L10P_T1_13_AB29	AB29	FMC LPC LA30 P
IO_L9N_T1_DQS_13_AE29	AE29	FMC LPC LA31 N
IO_L9P_T1_DQS_13_AD29	AD29	FMC LPC LA31 P
IO_L8N_T1_13_AA30	AA30	FMC LPC LA32 N
IO_L8P_T1_13_Y30	Y30	FMC LPC LA32 P
IO_L7N_T1_13_AC30	AC30	FMC LPC LA33 N
IO_L7P_T1_13_AC29	AC29	FMC LPC LA33 P
IO_L6N_T0_VREF_13_AB25	AB25	XADC GPIO 0
IO_L6P_T0_13_AA25	AA25	XADC GPIO 1
IO_L5N_T0_13_AB28	AB28	XADC GPIO 2
IO_L5P_T0_13_AA27	AA27	XADC GPIO 3
IO_L4N_T0_13_Y29	Y29	GPIO DIP SW0
IO_L4P_T0_13_W29	W29	GPIO DIP SW1
IO_L3N_T0_DQS_13_AA28	AA28	GPIO DIP SW2
IO_L3P_T0_DQS_13_Y28	Y28	GPIO DIP SW3
IO_L2N_T0_13_W28	W28	REC CLOCK C N
IO_L2P_T0_13_W27	W27	REC CLOCK C P
IO_L1N_T0_13_AA26	AA26	ROTARY PUSH
IO_L1P_T0_13_Y26	Y26	ROTARY INCA
IO_0_13_Y25	Y25	ROTARY INCB

By design of the KC705 board the FPGA (7KC325T-FFG900) IO-Bank 12 and IO-Bank 13 are used for the LPC FMC connector.

The FMC-LPC connector setup of the KC705 board dictates that for IO-Bank 12 this setup is possible:

-  - High-speed clock output.
-  - Bit clock (High Speed) and Frame/Sync (Low Speed) clock inputs.
-  - Data inputs.

# FPGA Virtual ADC



# Virtual ADC pinout.

	25	12	AE20	AE20	SI5326	RST	LS				
		F3	12	AK21	AK21	FMC	LPC	LA06	N		
	IO	L24P	T3	12	AK20	AK20	FMC	LPC	LA06	P	
	IO	L23N	T3	12	AJ21	AJ21	FMC	LPC	LA04	N	
	IO	L23P	T3	12	AH21	AH21	FMC	LPC	LA04	P	
	IO	L22N	T3	12	AH20	AH20	FMC	LPC	LA03	N	
	IO	L22P	T3	12	AG20	AG20	FMC	LPC	LA03	P	
IO	L21N	T3	DQS	12	AJ23	AJ23	FMC	LPC	LA08	N	
IO	L21P	T3	DQS	12	AJ22	AJ22	FMC	LPC	LA08	P	
	IO	L20N	T3	12	AH22	AH22	FMC	LPC	LA05	N	
	IO	L20P	T3	12	AG22	AG22	FMC	LPC	LA05	P	
IO	L19N	T3	VREF	12	AF21	AF21	FMC	LPC	LA02	N	
	IO	L19P	T3	12	AF20	AF20	FMC	LPC	LA02	P	
	IO	L18N	T2	12	AH25	AH25	FMC	LPC	LA07	N	
	IO	L18P	T2	12	AG25	AG25	FMC	LPC	LA07	P	
	IO	L17N	T2	12	AK24	AK24	FMC	LPC	LA09	N	
	IO	L17P	T2	12	AK23	AK23	FMC	LPC	LA09	P	
	IO	L16N	T2	12	AF25	AF25	FMC	LPC	LA11	N	
	IO	L16P	T2	12	AE25	AE25	FMC	LPC	LA11	P	
IO	L15N	T2	DQS	12	AK25	AK25	FMC	LPC	LA10	N	
IO	L15P	T2	DQS	12	AJ24	AJ24	FMC	LPC	LA10	P	
IO	L14N	T2	SRCC	12	AH24	AH24	HDMI	INT			
IO	L14P	T2	SRCC	12	AG24	AG24	SI5326	INT	ALM	LS	
IO	L13N	T2	MRCC	12	AG23	AG23	FMC	LPC	CLK0	M2C	N
IO	L13P	T2	MRCC	12	AF22	AF22	FMC	LPC	CLK0	M2C	P
IO	L12N	T1	MRCC	12	AE24	AE24	FMC	LPC	LA00	CC	N
IO	L12P	T1	MRCC	12	AD23	AD23	FMC	LPC	LA00	CC	P
IO	L11N	T1	SRCC	12	AF23	AF23	FMC	LPC	LA01	CC	N
IO	L11P	T1	SRCC	12	AE23	AE23	FMC	LPC	LA01	CC	P
	IO	L10N	T1	12	AE21	AE21	FMC	LPC	LA14	N	
	IO	L10P	T1	12	AD21	AD21	FMC	LPC	LA14	P	
IO	L9N	T1	DQS	12	AD24	AD24	FMC	LPC	LA15	N	
IO	L9P	T1	DQS	12	AC24	AC24	FMC	LPC	LA15	P	
	IO	L8N	T1	12	AD22	AD22	FMC	LPC	LA16	N	
	IO	L8P	T1	12	AC22	AC22	FMC	LPC	LA16	P	
	IO	L7N	T1	12	AC25	AC25	FMC	LPC	LA13	N	
	IO	L7P	T1	12	AB24	AB24	FMC	LPC	LA13	P	
IO	L6N	T0	VREF	12	AB20	AB20	FMC	LPC	LA12	N	
	IO	L6P	T0	12	AA20	AA20	FMC	LPC	LA12	P	
	IO	L5N	T0	12	AC21	AC21	SDIO	CD	DAT3	LS	
	IO	L5P	T0	12	AC20	AC20	SDIO	DAT0	LS		
	IO	L4N	T0	12	AA23	AA23	SDIO	DAT1	LS		
	IO	L4P	T0	12	AA22	AA22	SDIO	DAT2	LS		
IO	L3N	T0	DQS	12	AB23	AB23	SDIO	CLK	LS		
IO	L3P	T0	DQS	12	AB22	AB22	SDIO	CMD	LS		
	IO	L2N	T0	12	AA21	AA21	SDIO	SDDET			
	IO	L2P	T0	12	Y21	Y21	SDIO	SDWP			
	IO	L1N	T0	12	Y24	Y24	USER	SMA	GPIO	N	
	IO	L1P	T0	12	Y23	Y23	USER	SMA	GPIO	P	
	IO	0	12	Y20	Y20	SFP	TX	DISABLE			



By design of the KC705 board the FPGA (7KC325T-FFG900) IO-Bank 12 and IO-Bank 13 are used for the LPC FMC connector.

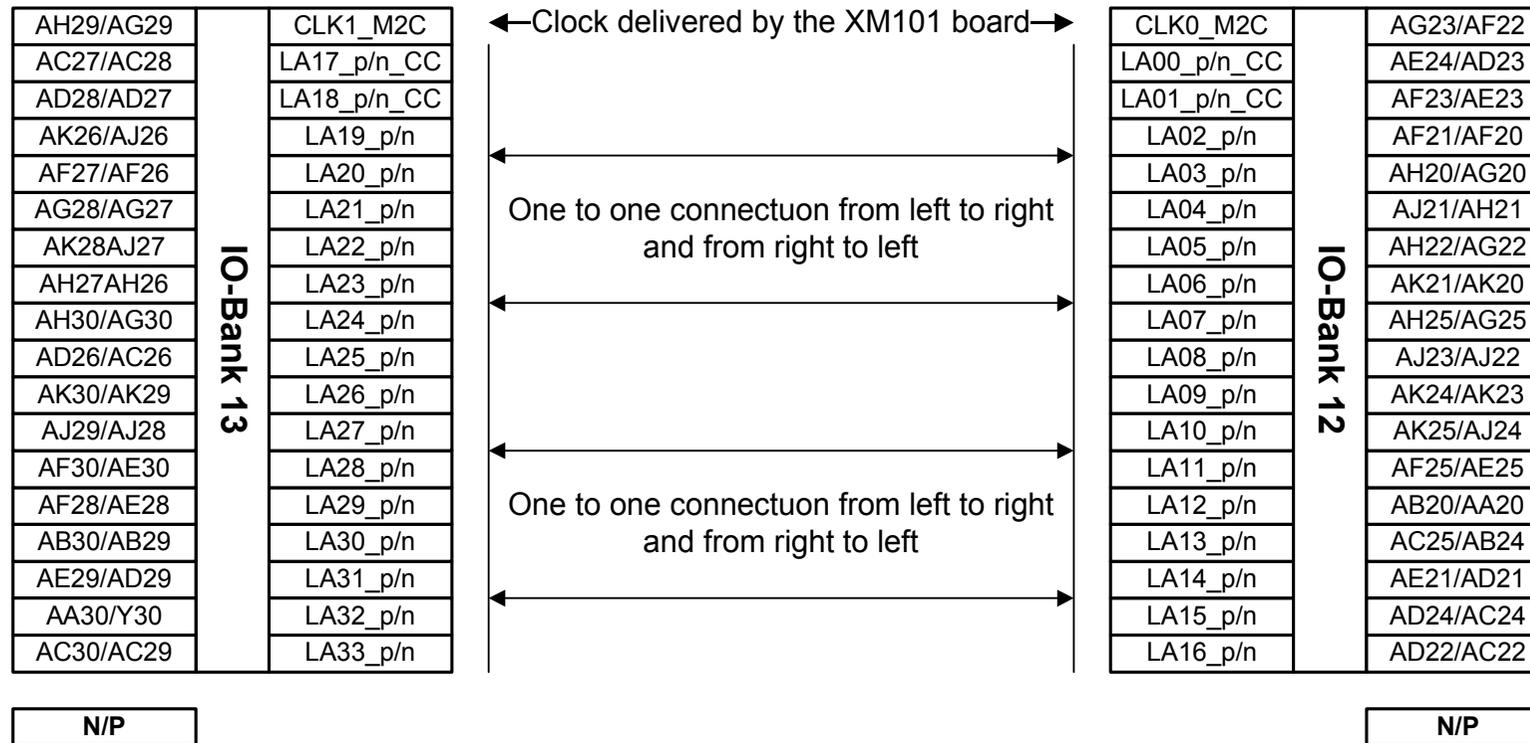
The FMC-LPC connector setup of the KC705 board dictates that for IO-Bank 13 this setup is possible:

-  - High-speed clock input.
-  - Bit clock (High Speed) and Frame/Sync (Low Speed) clock outputs.
-  - Data outputs.

# FPGA LPC IO-Banks 12 and 13 connected via cable

As shown on page 7 the transmitter, Virtual ADC, will be connected to the receiver, ADC interface in the FPGA. This holds that IO-Bank 12 is connected to IO-Bank 13 by means of a XM101 board plugged into the LPC FMC connector of the KC705 board.

This slide shows the interconnections via the XM101 board between the IO-Banks.



# The DAC (Transmitter)

