AdcData

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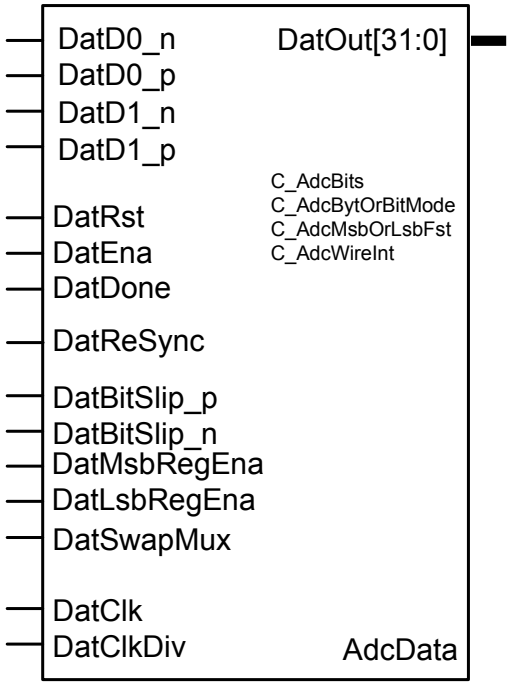

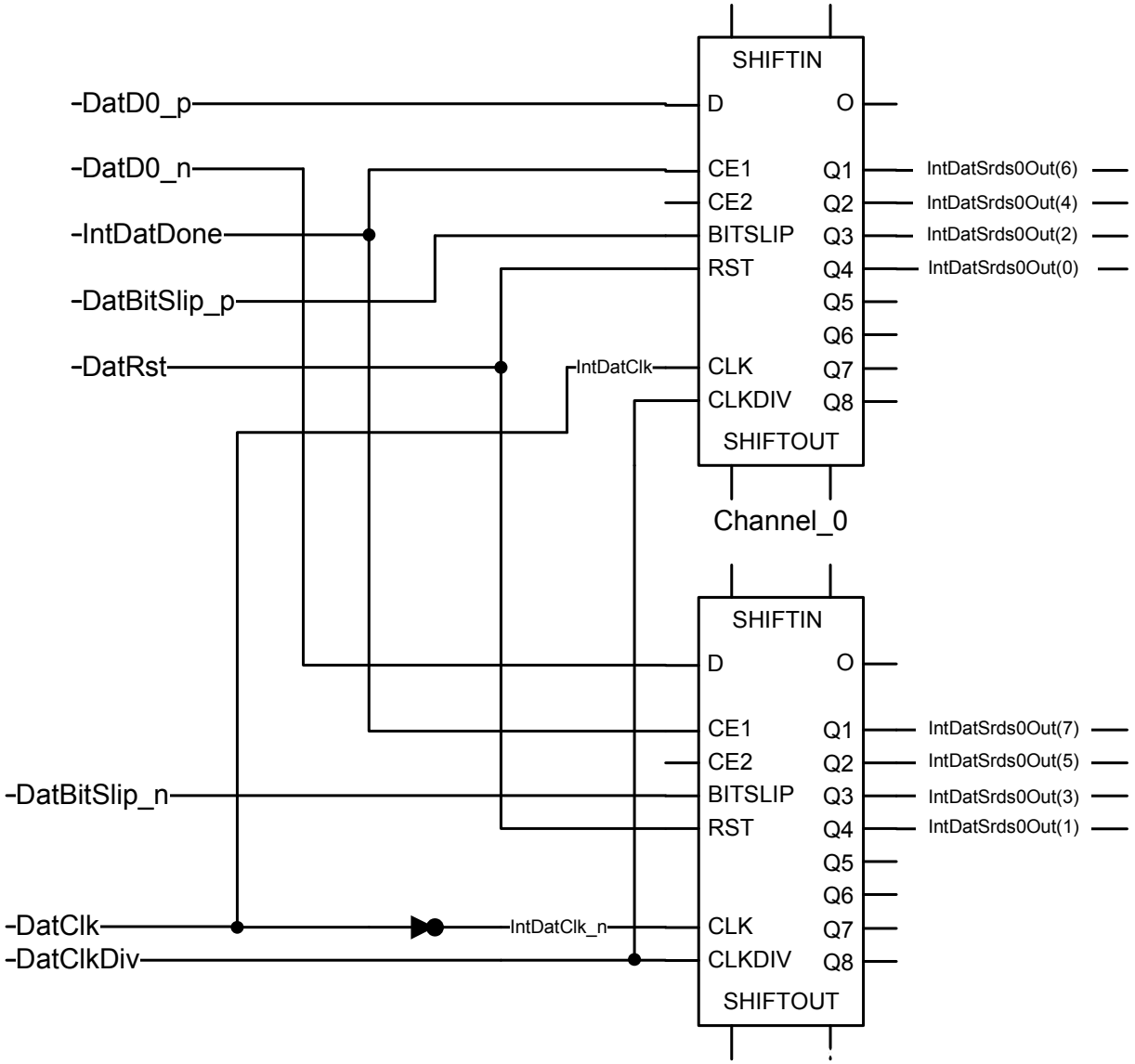

Bit – Byte ordering setup.
This hierarchical level is called from a "AdcDataMultiChnl" level.
On that level bits and bytes are split and assembled.
The way it is done is explained here:

Assume 1-wire, 8 channel interface.
The ADC pinning and pin naming will be as:
DH_p/n, DG_p/n, DF_p/n, DE_p/n, DD_p/n, DC_p/n, DB_P/n, and DA_P/n.

These 1-wire channels IO align to a 2-wire channel IO setup as:

DA0_p/n	DA_p/n
DA1_p/n	DB_p/n
DB0_p/n	DC_p/n
DB1_p/n	DD_p/n
DC0_p/n	DE_p/n
DC1_P/n	DF_p/n
DD0_p/n	DG_p/n
DD1_p/n	DH_p/n

Before the inputs enter this level they are grouped into a busses. Busses of depth depending the number of input channels. In case of 1-wire, 8 channels there will be 4 busses of 4 bits each:

```
-- 8 channel
-- 1-wire          chnl_7  chnl_5  chnl_3  chnl_1
--                 chnl_8  chnl_6  chnl_4  chnl_2
IntDat0_p <=       DD0_p & DC0_p & DB0_p & DA0_p;
IntDat0_n <=       DD0_n & DC0_n & DB0_n & DA0_n;
IntDat1_p <=       DD1_p & DC1_p & DB1_p & DA1_p;
IntDat1_n <=       DD1_n & DC1_n & DB1_n & DA1_n;
```

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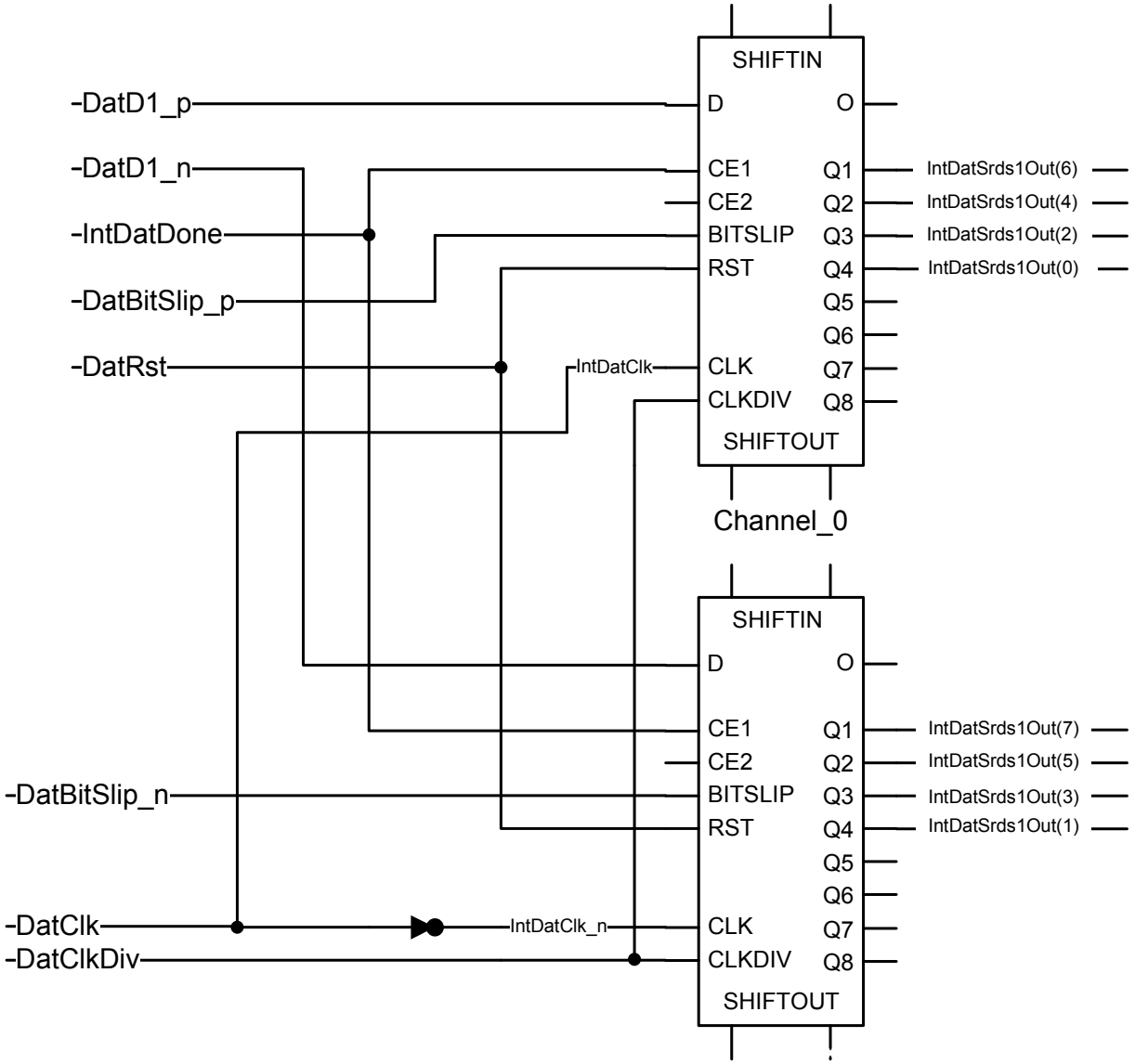

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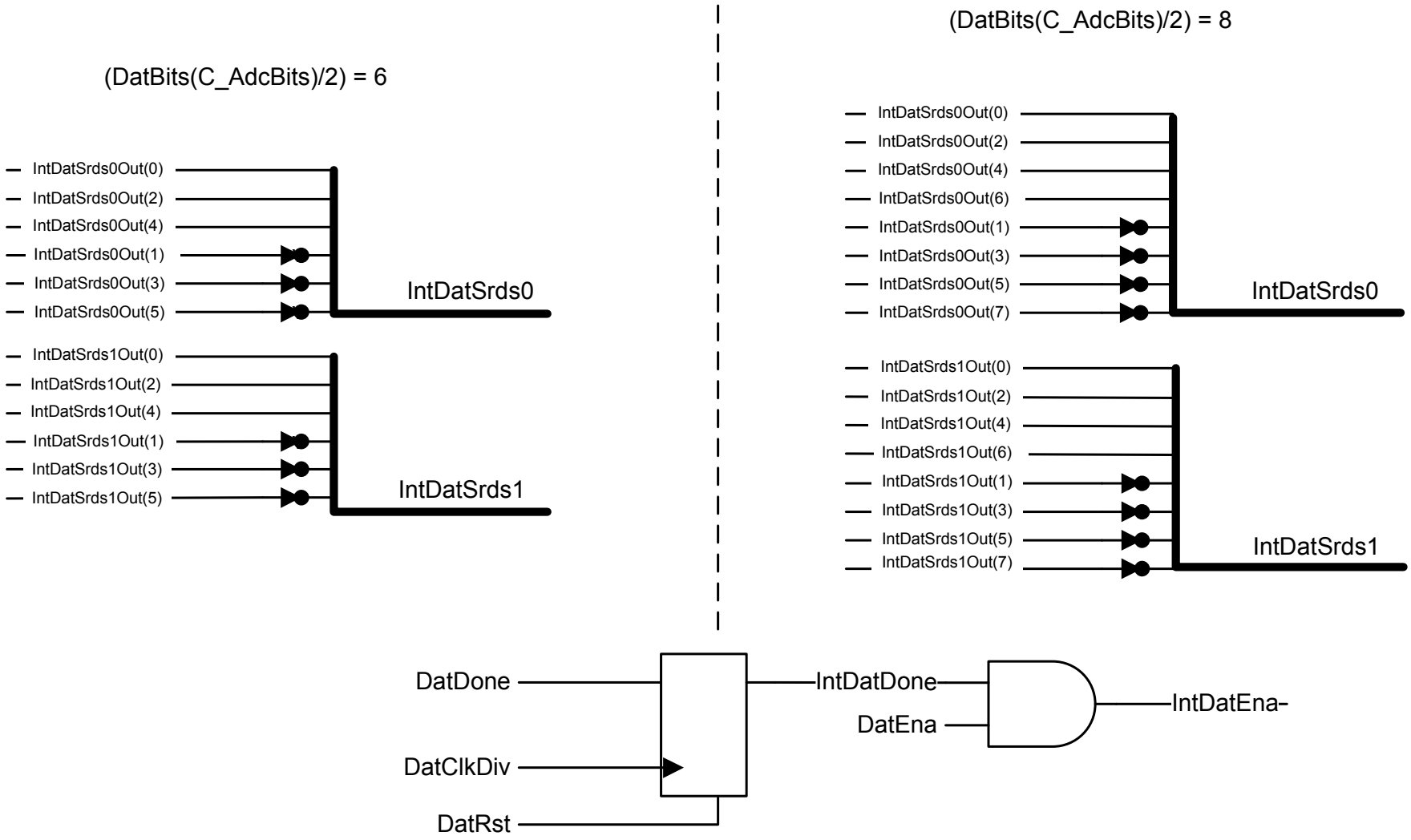
This implementation “AdcDataChnl” takes two ADC inputs per channel. It thus takes one channel in 2-wire mode or two channels in 1-wire mode.

In case of 2-wire mode this module is called for the amount of channels needed. In case of 1-wire mode this module is called for ½ the amount of channels needed.

Example: 1-wire, 8 channels
The module will be called 4 times.
The first time it’s called as: n = 3
the input and output data are looking then as:
- input
DatD0_n/p <= IntDat0_n/p(3)
DatD1_n/p <= IntDat1_n/p(3)
- output
DatOut => IntDatOut (127: 96)
All the next times the module is called,
the output will look as:
DatOut => IntDatOut (95: 64)
DatOut => IntDatOut (63: 32)
DatOut => IntDatOut (31: 0)

Each output data contains two 16-bit channels and in the total bus the channels are arranged as:
DH, DG, DF, DE, DD, DC, DB, DA.



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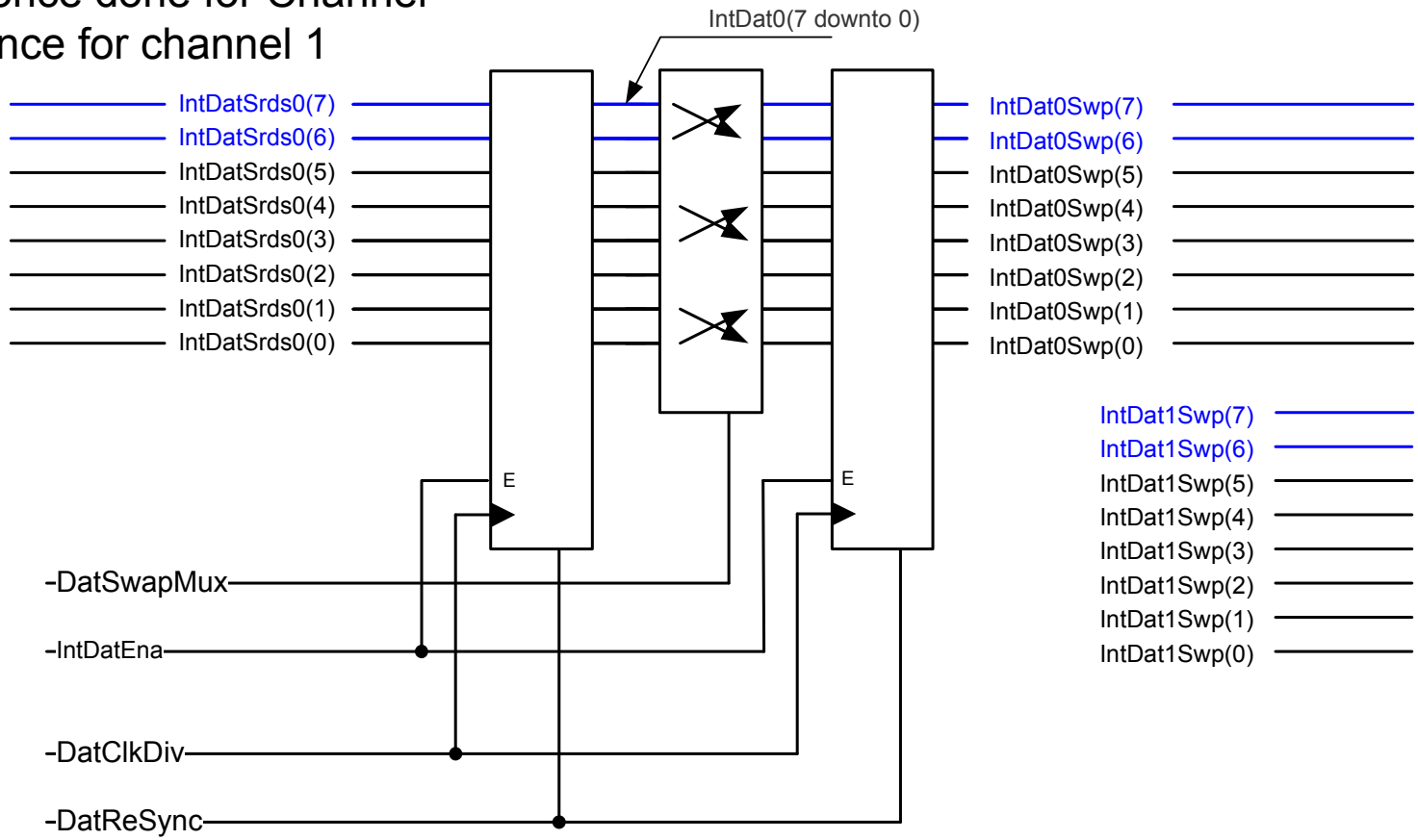
This is once done for Channel 0 and once for channel 1



For a 12-bit Data capturing circuit the blue signals are not available.