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Adclo

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DISCLAIMER:

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Adclo Symbol

DCLK_p('p')
DCLK_n('p')
FCLK_p('p')
FCLK_n('p')

DATA_p[('c'*'w'*'p')-1:0]
DATA_n[('c'*'w'*'p')-1:0]

Adc_DCLK_'p'_p_pin
Adc_DCLK_'p'_n_pin

Adc_FCLK_'p'_p_pin
Adc_FCLK_'p'_n_pin

Adc_DI_'cw'_'p'_p_pin
Adc_DI_'cw'_'p'_n_pin

Adclo
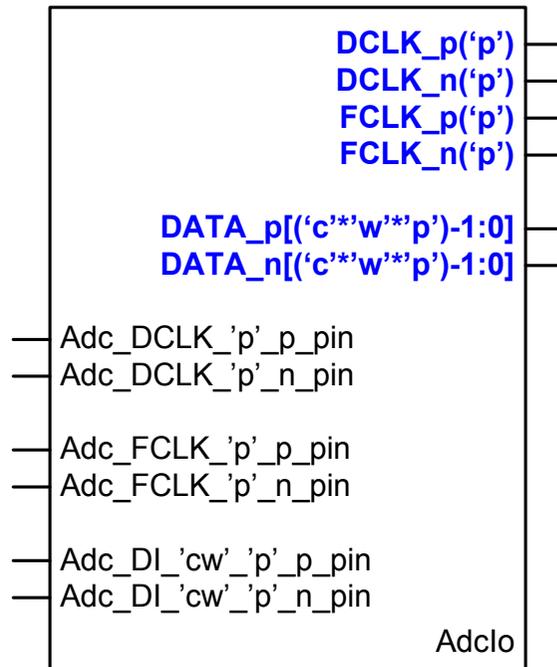
'c' = Number of channels
'w' = Wire interface
'p' = Number op ports

Example of pin naming:
When there are 2 ports with each 4 channels then:
DCLK_p/n(1), DCLK_p/n(0), and etcetera
DATA_p/n[15:0]
      4 channels in 2-wire mode means 8 pins per port.
      2-wire mode uses two pins per channel.
Adc_DI_7_1_p/n_pin
....
....
Adc_DI_0_1_p/n_pin
Adc_DI_7_0_p/n_pin
Adc_DI_6_0_p/n_pin
....
...............…

This file needs to be modified and adapted whenever pins, ports, or channels are added, removed, or altered.
This file changes from design to design and the pin naming of the external world pins must match that of the naming used in the UCF file.
A good extension could be to put the pin LOC-king information into this file too, then all IO information fits one place in the design.

This hierarchical block holds all the IO buffers used with the ADC interface.
The blue coloured signals are interconnects to the other hierarchical blocks in the design,
mainly (only) to the "AdcToplevel" block.
The other pins are connected to the outside world. They are the pins of the interface.

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