



Adclo

Marc Defossez
Sr. Staff Applications Engineer

Created: December 4, 2009
Modified: December 4, 2009

© Copyright 2009 - 2009, Xilinx, Inc. All rights reserved.

DISCLAIMER:

© Copyright 2009 - 2009, Xilinx, Inc. All rights reserved.

This file contains confidential and proprietary information of Xilinx, Inc. and is protected under U.S. and international copyright and other intellectual property laws.

Disclaimer:

This disclaimer is not a license and does not grant any rights to the materials distributed herewith. Except as otherwise provided in a valid license issued to you by Xilinx, and to the maximum extent permitted by applicable law: (1) THESE MATERIALS ARE MADE AVAILABLE "AS IS" AND WITH ALL FAULTS, AND XILINX HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under or in connection with these materials, including for any direct, or any indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same.

CRITICAL APPLICATIONS

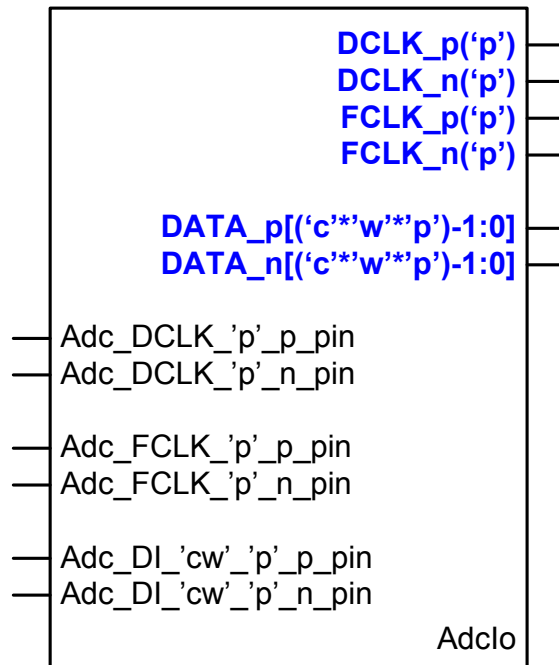
Xilinx products are not designed or intended to be fail-safe, or for use in any application requiring fail-safe performance, such as life-support or safety devices or systems, Class III medical devices, nuclear facilities, applications related to the deployment of airbags, or any other applications that could lead to death, personal injury, or severe property or environmental damage (individually and collectively, "Critical Applications"). Customer assumes the sole risk and liability of any use of Xilinx products in Critical Applications, subject only to applicable laws and regulations governing limitations on product liability.

THIS COPYRIGHT NOTICE AND DISCLAIMER MUST BE RETAINED AS PART OF THIS FILE AT ALL TIMES.

Contact: e-mail hotline@xilinx.com phone + 1 800 255 7778

This page is intentionally left blank.

Adclo Symbol



'c' = Number of channels

'w' = Wire interface

'p' = Number of ports

Example of pin naming:

When there are 2 ports with each 4 channels then:

DCLK_p/n(1), DCLK_p/n(0), and etcetera

DATA_p/n[15:0]

4 channels in 2-wire mode means 8 pins per port.

2-wire mode uses two pins per channel.

Adc_DI_7_1_p/n_pin

.....

.....

Adc_DI_0_1_p/n_pin

Adc_DI_7_0_p/n_pin

Adc_DI_6_0_p/n_pin

.....

.....

This file needs to be modified and adapted whenever pins, ports, or channels are added, removed, or altered.

This file changes from design to design and the pin naming of the external world pins must match that of the naming used in the UCF file. A good extension could be to put the pin LOC-ing information into this file too, then all IO information fits one place in the design.

This hierarchical block holds all the IO buffers used with the ADC interface.

The blue coloured signals are interconnects to the other hierarchical blocks in the design, mainly (only) to the "AdcToplevel" block.

The other pins are connected to the outside world. They are the pins of the interface.