# AppsRstEna

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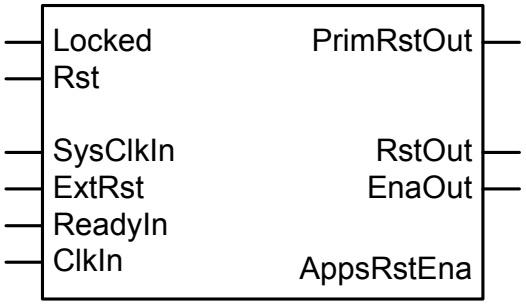
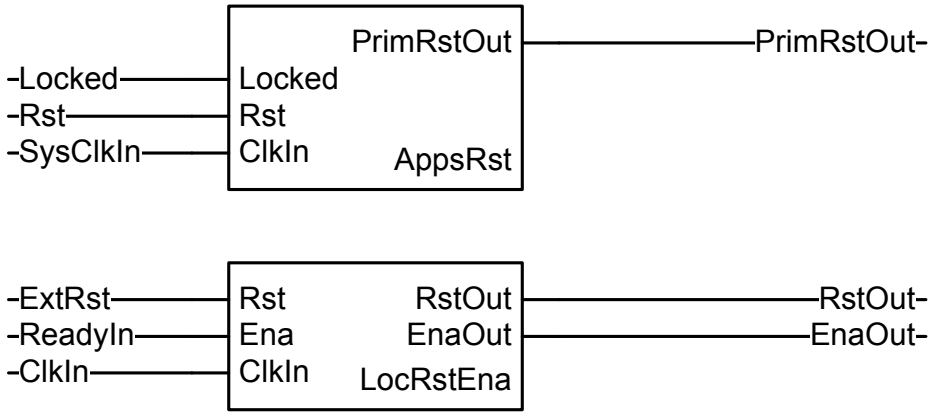
# Toplevel

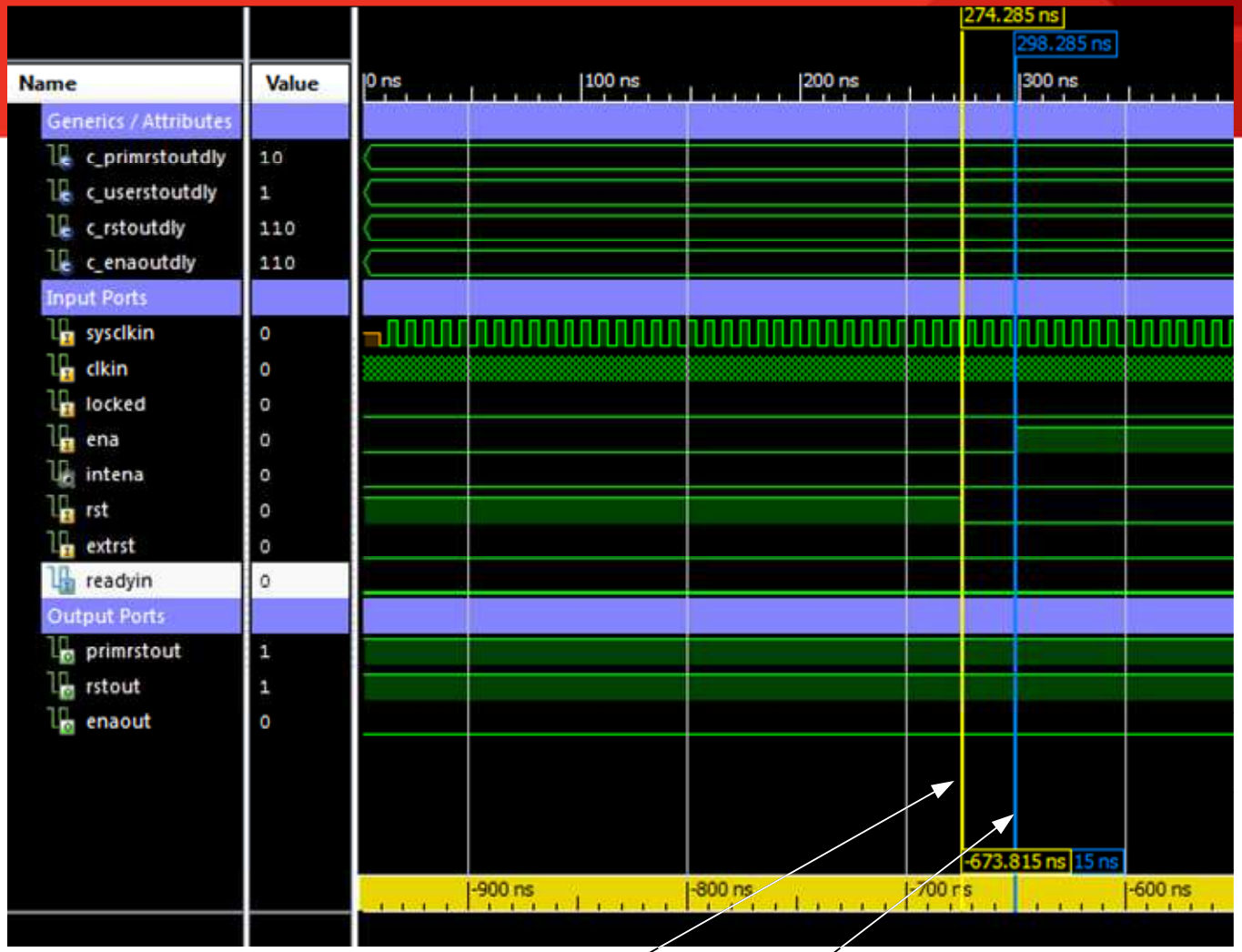





AppsRst runs on the raw system clock, this is the clock that is input into the MMCM.
The Rst input is the raw system reset, this is the same reset as used for the MMCM.
When an Ena signal is high and the MMCM is locked (high active) then the circuit will produce a high-to-low signal.
This signal is synchronized to the external applied system clock.
The output signal of AppsRst is used to activate the IDELAYCTRL component.
When the IDLEAYCTRL goes ready then the second part of this circuit comes alive.

This second part iof this circuit runs on one of the output clocks of the MMCM (this is now stable, else the previous part of this circuit could not have been run).
When an external reset is Low and the IDELAYCTRL ready (RDY) signal is high, this part of the design will release the reset and produce after a programmable delay an enable output.

These signals can be used throughout the whole design.
These signals are synchronous to one of the output clocks of the MMCM were this circuit is used.




System / Application reset goes low (active)

System / Application enable goes High (active)

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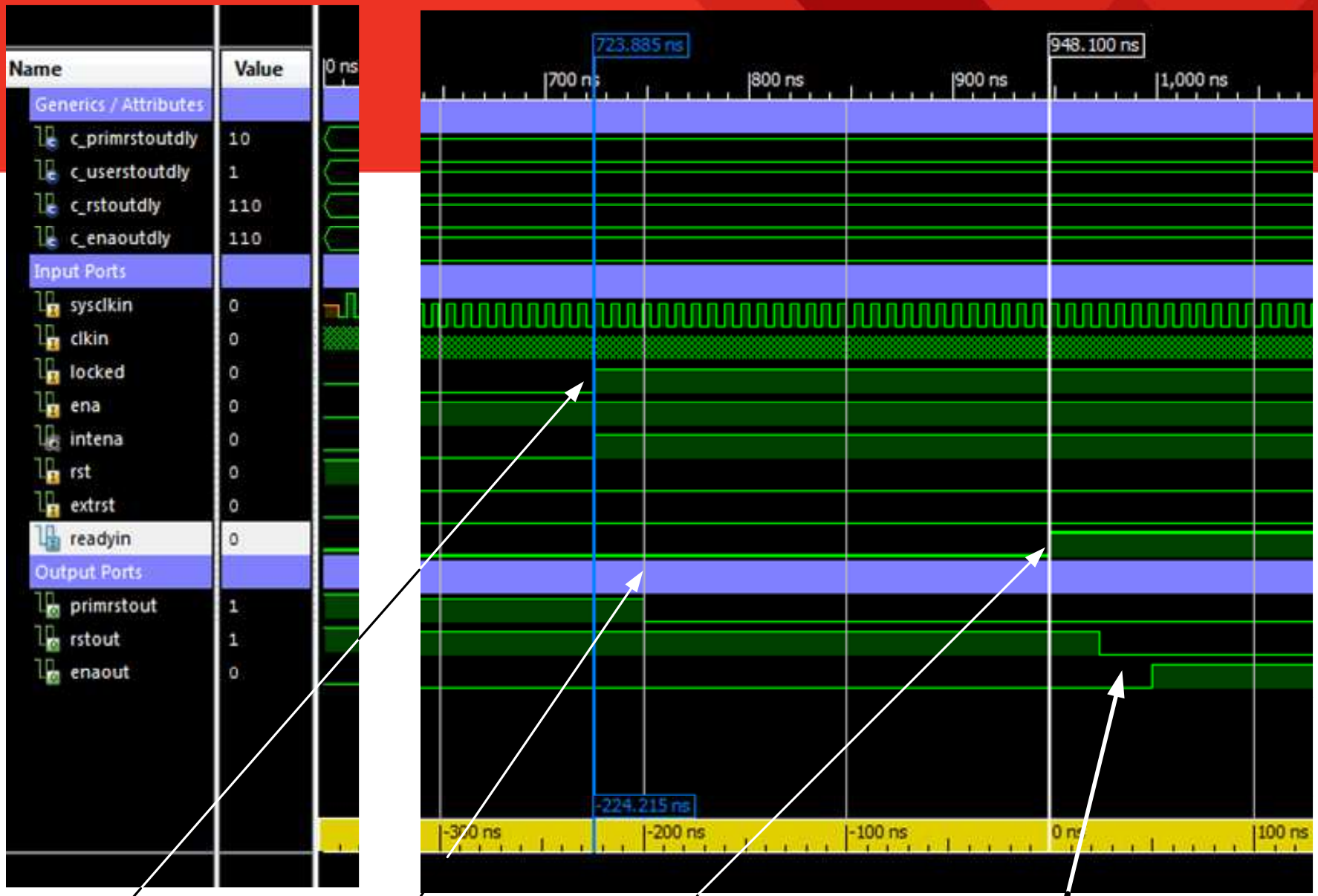


MMCM LOCKED goes high

Primary reset goes low (active

IDELAYCTRL.RDY goes high

Internal reset goes low and internal enable goes high. The logic can now run.





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