



AdcData

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Created: February 7, 2008
Modified: July 25, 2012

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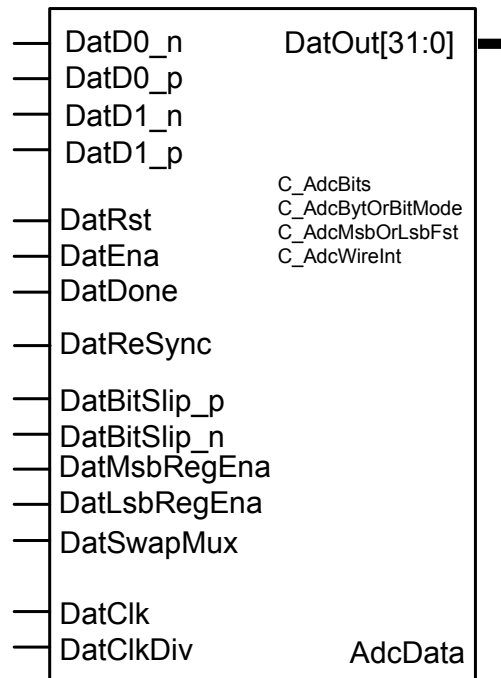
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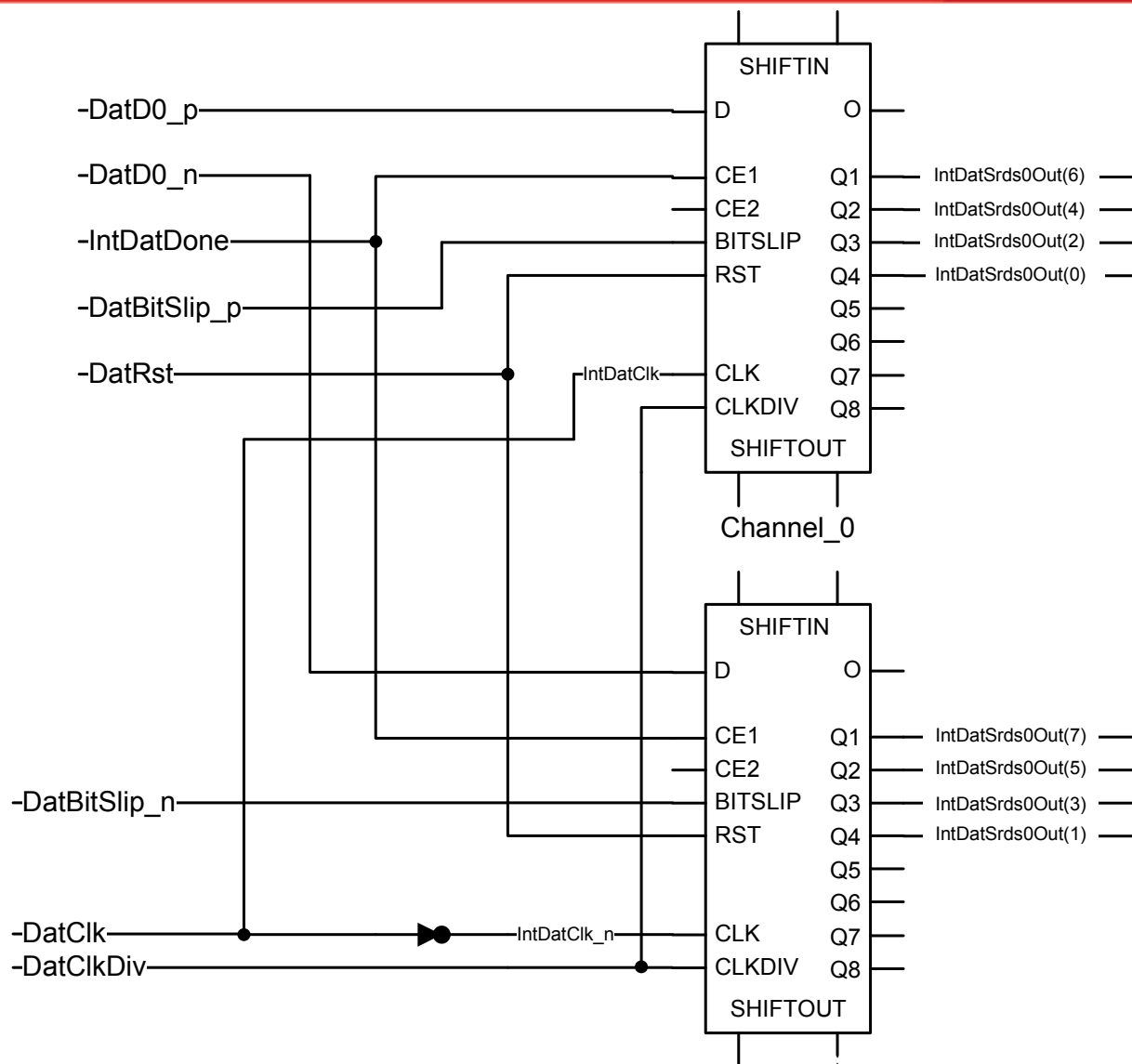
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Bit – Byte ordering setup.

This hierarchical level is called from a

“AdcDataMultiChnl” level.

On that level bits and bytes are split and assembled.

The way it is done is explained here:

Assume 1-wire, 8 channel interface.

The ADC pinning and pin naming will be as:

DH_p/n, DG_p/n, DF_p/n, DE_p/n, DD_p/n, DC_p/n, DB_P/n, and DA_P/n.

These 1-wire channels IO align to a 2-wire channel IO setup as:

DA0_p/n	DA_p/n
DA1_p/n	DB_p/n
DB0_p/n	DC_p/n
DB1_p/n	DD_p/n
DC0_p/n	DE_p/n
DC1_P/n	DF_p/n
DD0_p/n	DG_p/n
DD1_p/n	DH_p/n

Before the inputs enter this level they are grouped into a busses. Busses of depth depending the number of input channels. In case of 1-wire, 8 channels there will be 4 busses of 4 bits each:

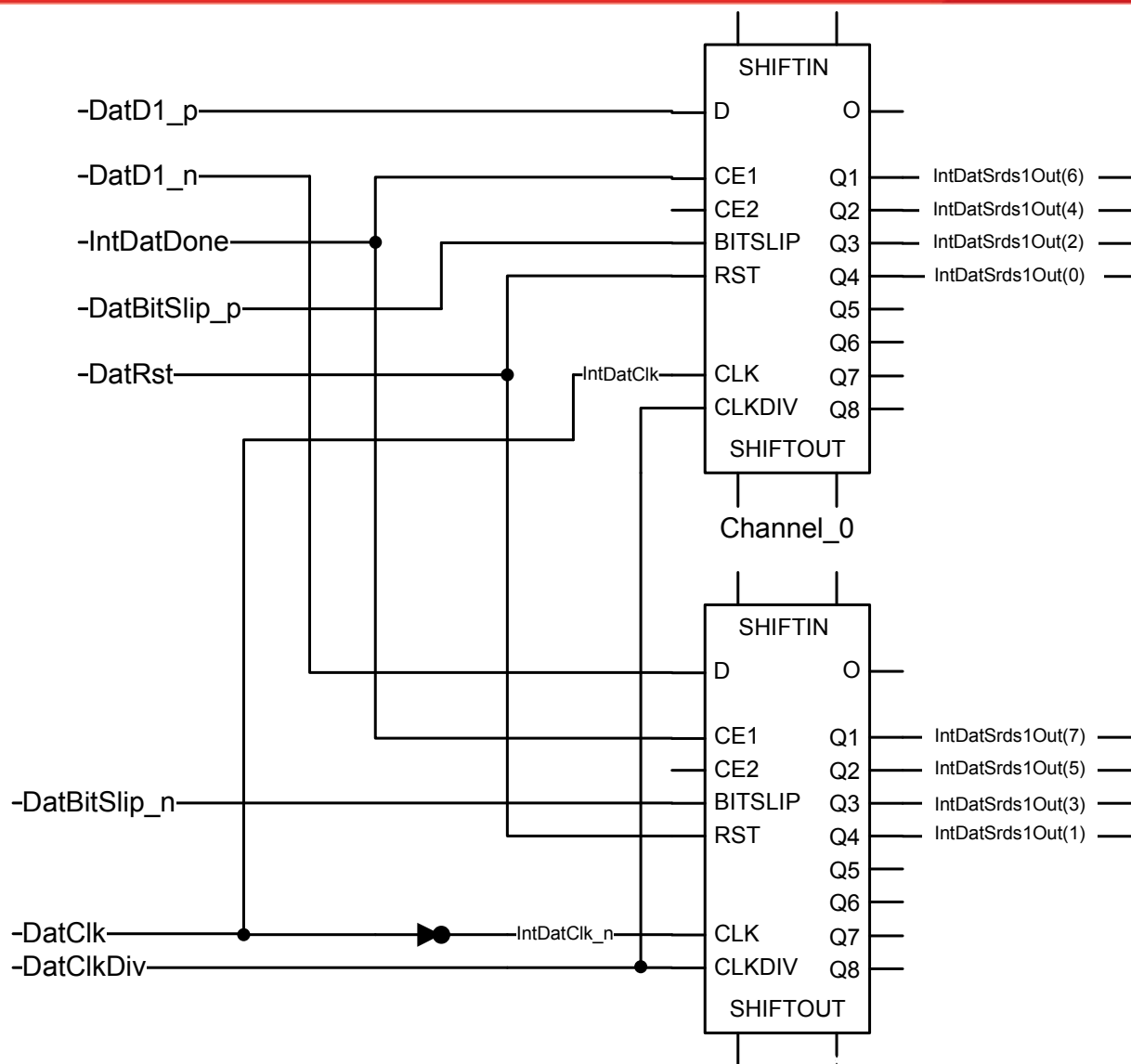
-- 8 channel

-- 1-wire

--

chnl_7	chnl_5	chnl_3	chnl_1
chnl_8	chnl_6	chnl_4	chnl_2
IntDat0_p <=	DD0_p & DC0_p & DB0_p & DA0_p;		
IntDat0_n <=	DD0_n & DC0_n & DB0_n & DA0_n;		
IntDat1_p <=	DD1_p & DC1_p & DB1_p & DA1_p;		
IntDat1_n <=	DD1_n & DC1_n & DB1_n & DA1_n;		

More next page.



From previous page:

This implementation "AdcDataChnl" takes two ADC inputs per channel. It thus takes one channel in 2-wire mode or two channels in 1-wire mode.

In case of 2-wire mode this module is called for the amount of channels needed. In case of 1-wire mode this module is called for $\frac{1}{2}$ the amount of channels needed.

Example: 1-wire, 8 channels

The module will be called 4 times.

The first time it's called as: $n = 3$

the input and output data are looking then as:

- input

$\text{DatD0_n/p} \leq \text{IntDat0_n/p}(3)$

$\text{DatD1_n/p} \leq \text{IntDat1_n/p}(3)$

- output

$\text{DatOut} \Rightarrow \text{IntDatOut}(127:96)$

All the next times the module is called,

the output will look as:

$\text{DatOut} \Rightarrow \text{IntDatOut}(95:64)$

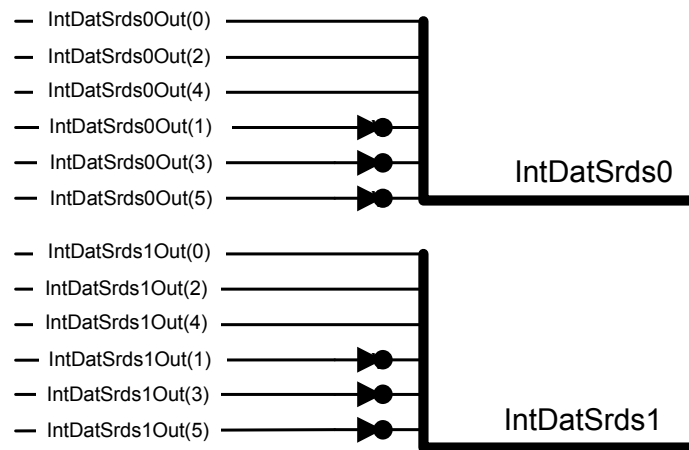
$\text{DatOut} \Rightarrow \text{IntDatOut}(63:32)$

$\text{DatOut} \Rightarrow \text{IntDatOut}(31:0)$

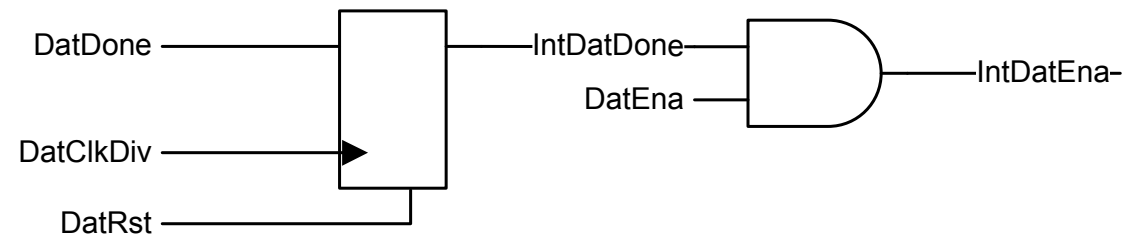
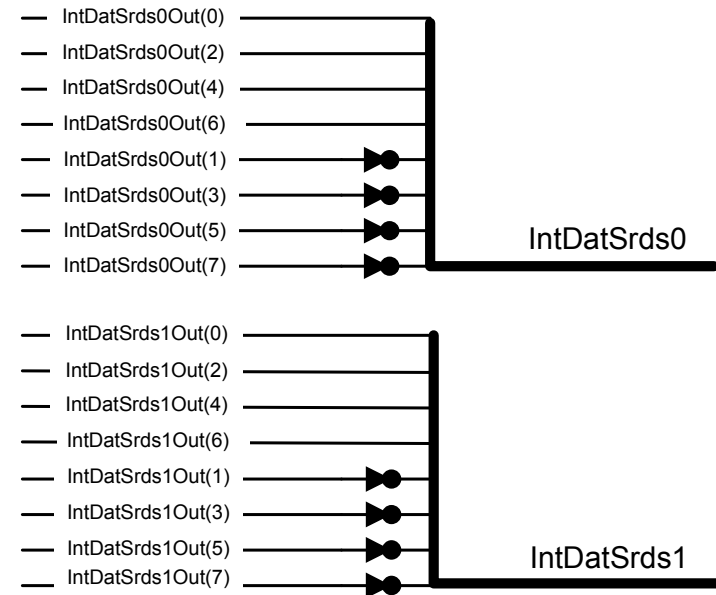
Each output data contains two 16-bit channels and in the total bus the channels are arranged as:

DH, DG, DF, DE, DD, DC, DB, DA.

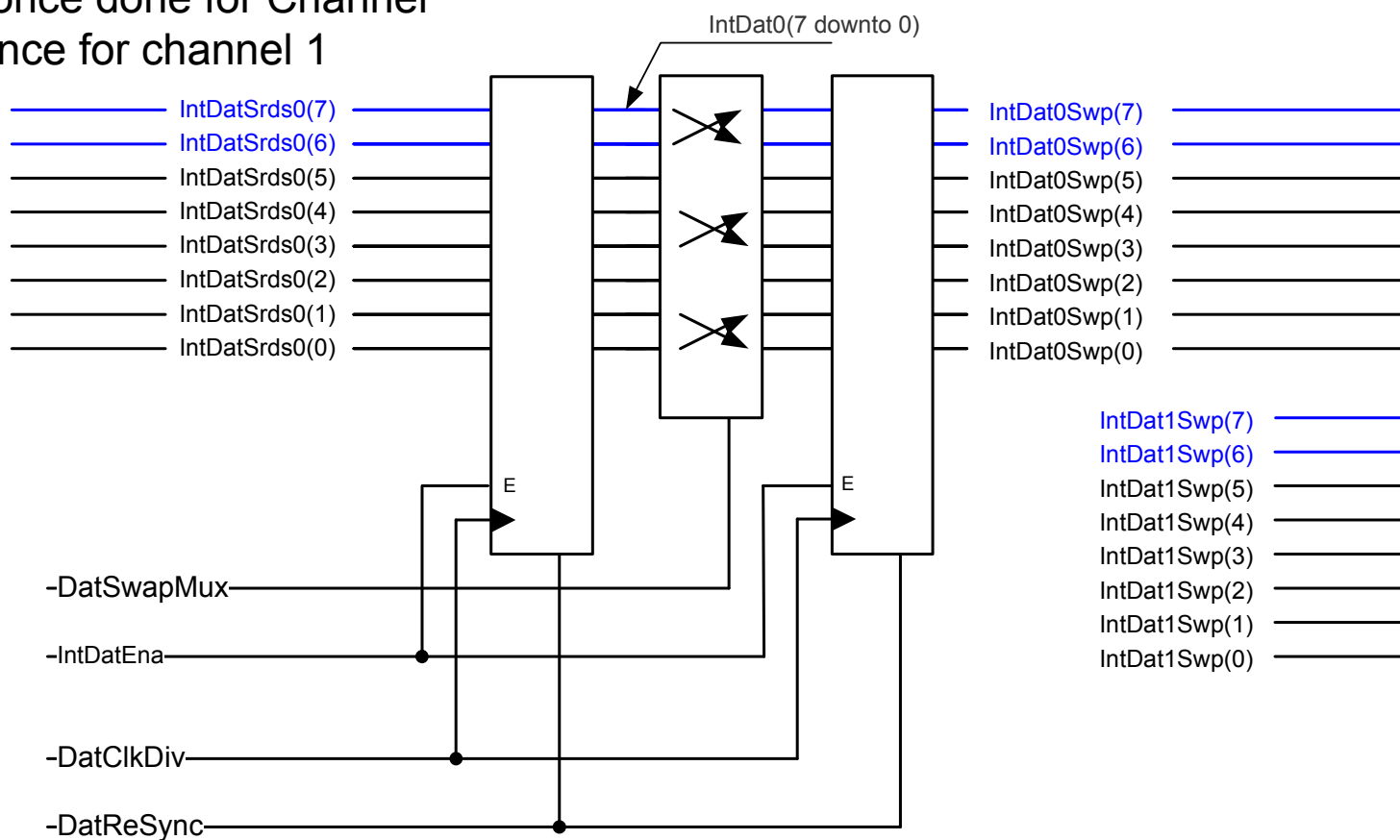
$$(\text{DatBits}(\text{C_AdcBits})/2) = 6$$



$$(\text{DatBits}(\text{C_AdcBits})/2) = 8$$



This is once done for Channel 0 and once for channel 1



For a 12-bit Data capturing circuit the blue signals are not available.

IntDat0Swp(7)
IntDat0Swp(6)
IntDat0Swp(5)
IntDat0Swp(4)
IntDat0Swp(3)
IntDat0Swp(2)
IntDat0Swp(1)
IntDat0Swp(0)
IntDat1Swp(7)
IntDat1Swp(6)
IntDat1Swp(5)
IntDat1Swp(4)
IntDat1Swp(3)
IntDat1Swp(2)
IntDat1Swp(1)
IntDat1Swp(0)

-DatReSync

1-wire = 1
2-wire = 2

1-wire/2-wire

C_AdcBits = 12 or 14/16
C_AdcWireInt

This is no logic but routing depending the choice of interface of the ADC.
1-wire or 2-wire and Bit or Byte arrangement and Msb or LSB transmitted first.

1-wire will output data of two channels into the 32-bit bus.
The lower 16-bit are the 0 channel and the higher 16-bit are the 1 channel.

2-wire will output only one channel in the 32-bit bus.
Both halves of the bus will contain the same value.

For 12-bit ADCs the upper four bits of each 16-bit word are stuffed with zero (0).

Of course any other scheme of connection is possible.

