



Double Nibble Detect

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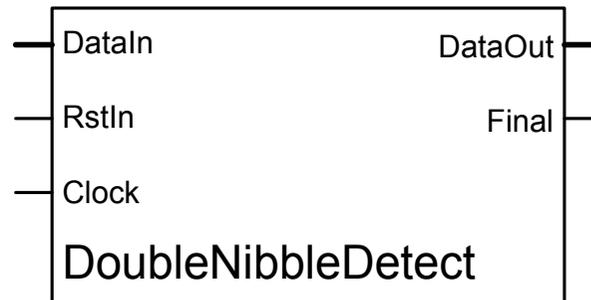
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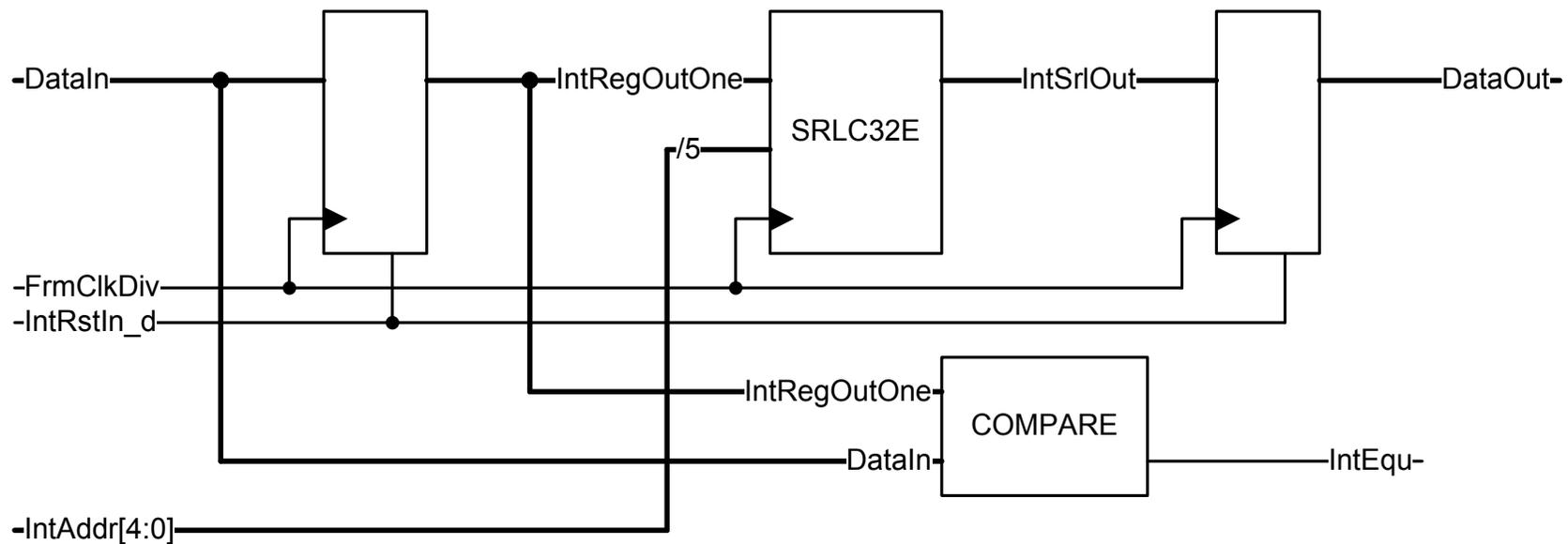
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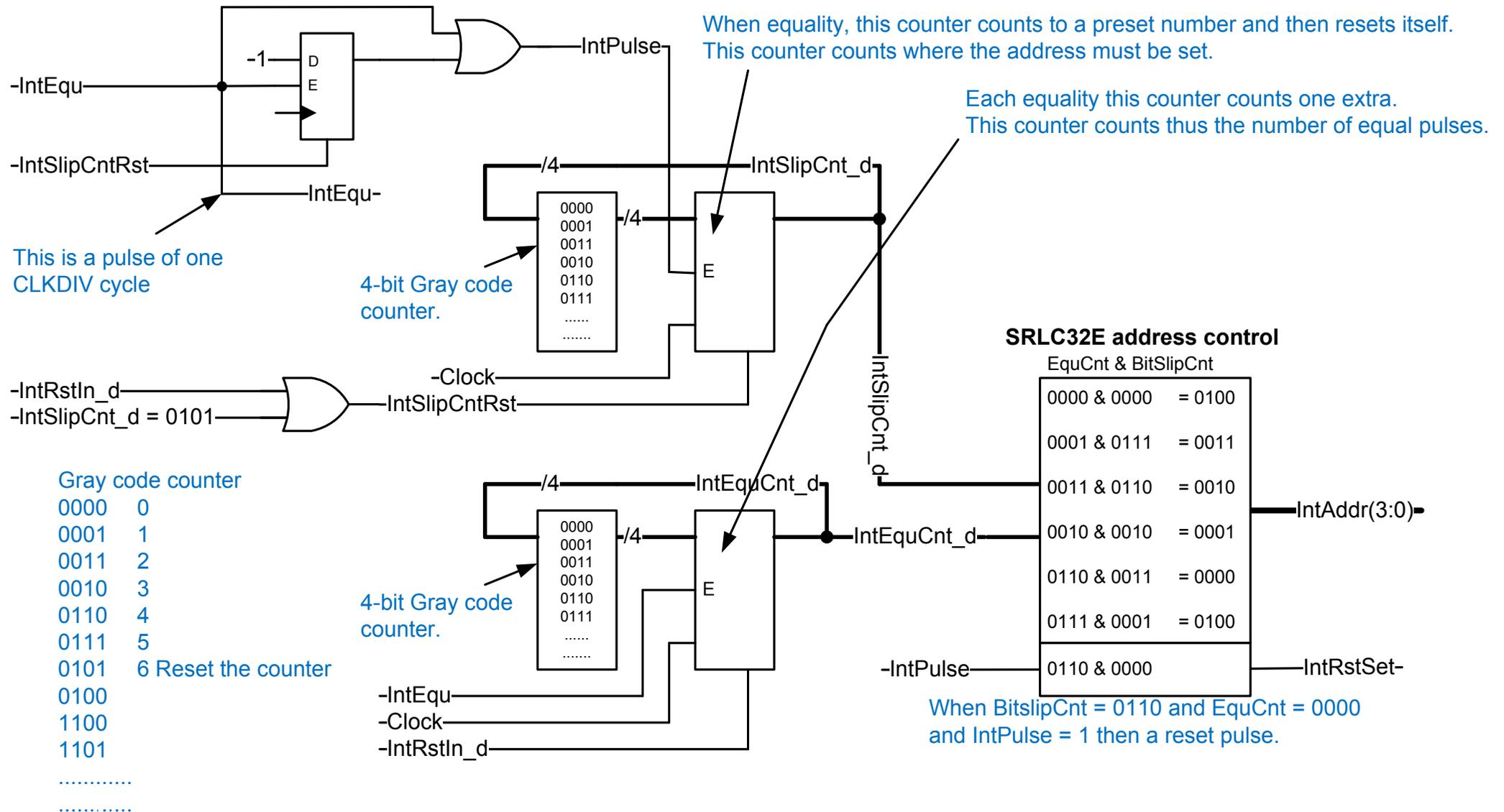
Symbol



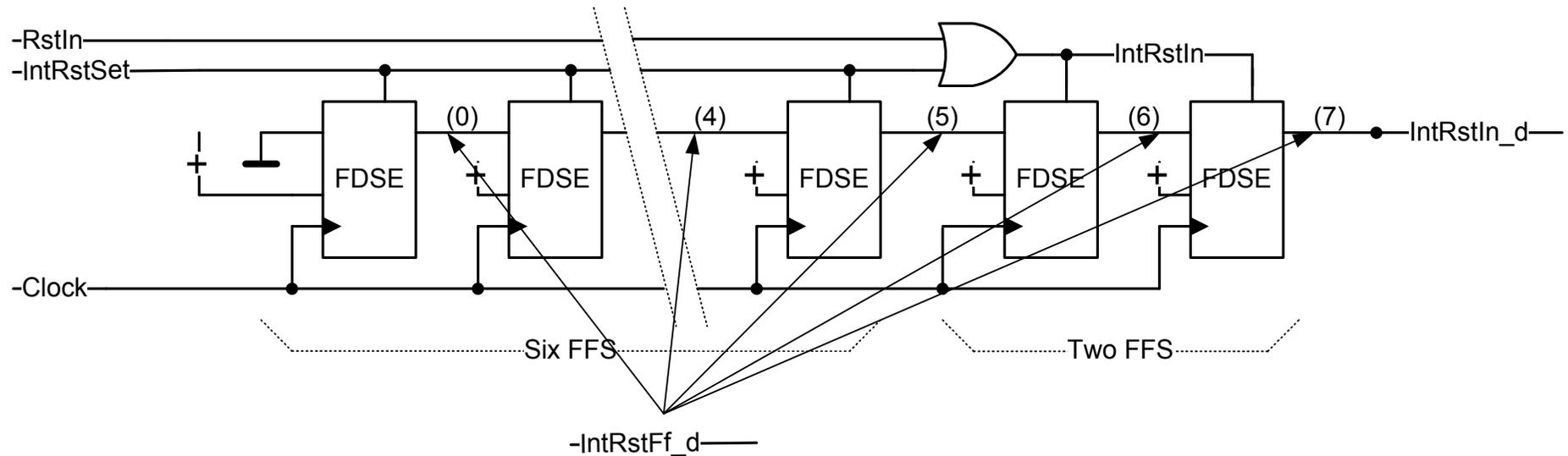
Datapath



Counters & SRL Control



Rst Control



When RstIn is applied, made high, the last two FFS will be set and immediately filled back with zero at the rate of Clock (rising edge). IntRstIn_d will thus go high for two Clock periods.

When IntRstSet is made high for a Clock cycle all FFS will turn high and then back filled with zero at the rate of Clock. IntRstIn_d will be high for eight Clock cycles.