GenPulse

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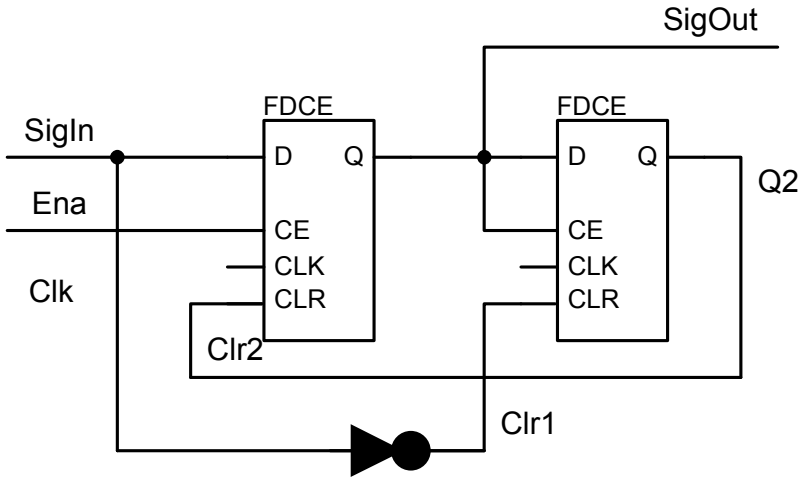
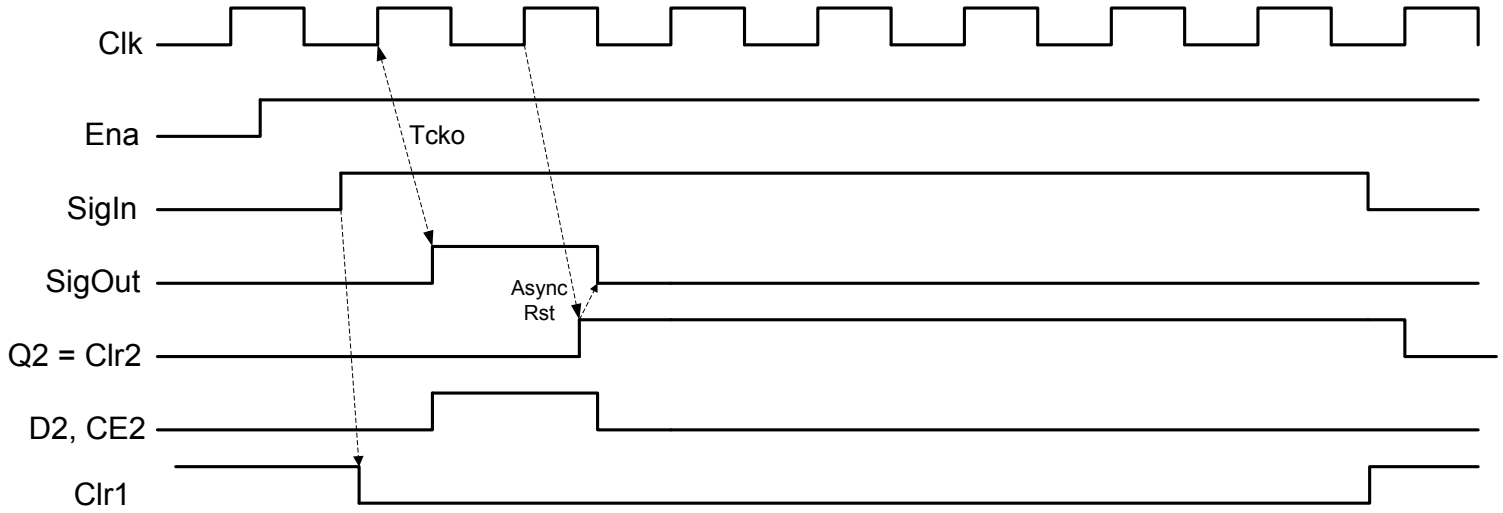
Original Circuit



In series 7 FPGA all FFs in a SLICE use the same S/R net. Also the CE net is shared by all FFs and the slice dictates that CE for the FF is shared with WE for the LUTs (it is CE or We not both). All LUTs share the same WE inputs.
This implementation occupies two SLICES!



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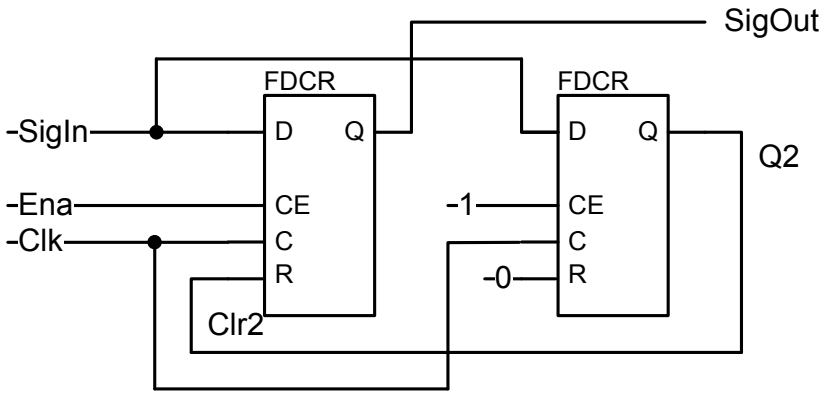
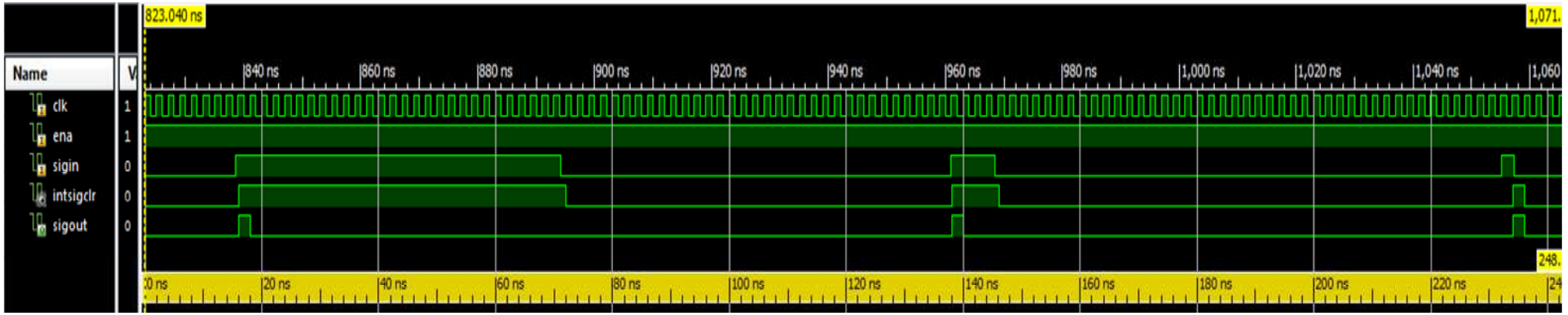
7-Series circuit



FDCR is a component made with R and CE implemented in logic (LUT). This FF react synchronous, a clock edge is needed to activate CE or R.

The cirecuit provide the same result as previous circuit. Make from a high going and staying signal a one clock period wide pulse.



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