TimeTickCnt

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The TimeTick counter is used to generate timing tick pulses with specific timing intervals.
The counting device is constructed with SRLC32E components for the Virtex-6 FPGA family.

For the generation of a regular time tick a known and very often available clock must be used.
A clock that is mostly available in designs with LVDS inputs and outputs is the IDELAYCTRL reference clock.
This is a clock with a frequency of 200 MHz.

As example:

    To Generate a pulse of 5 ns every 1 ms.
    The first SRLC32E generates a 5 ns pulse every 32 clock cycles. A pulse of 5 ns is thus generated every 160 ns.
    This pulse enables a second SRLC32E.
        Because the second SRLC32E is enabled every 160 ns, it will produce an output pulse every 5.12 us (160 ns * 32).
    When nothing is done this pulse will be 160 ns long. In this design we use a pulse generator that reduces the output pulse to a clock cycle or the reference clock (5 ns).
    This pulse will enable a third SRLC32E component who generates a pulse every (5.12 us * 32) or164 us.
        As above a pulse generator is used to limit the pulse length to one reference clock cycle.
    The Third pulse enables a fourth SRLC32E that will generate a pulse every (32* 164 us) 5.3 ms.
   This pulse is also reduced in length to one reference clock cycle.
    A pulse of 5.3 ms is to long, the SRL can't thus be used at full length.
        The address input of the SRLC32E must be set at 6, then the output will generate a pulse every (6 * 164 us) = 984 us
   984 us is ~ 1 ms.

By modifying the length of the SRLC32E shift registers it is thus possible to adjust the output timing of the tick generator.
For this design the address inputs are connected to fixed values but when they are connected to a register set used by a processor or state machine every possible with between two pulses can be constructed.
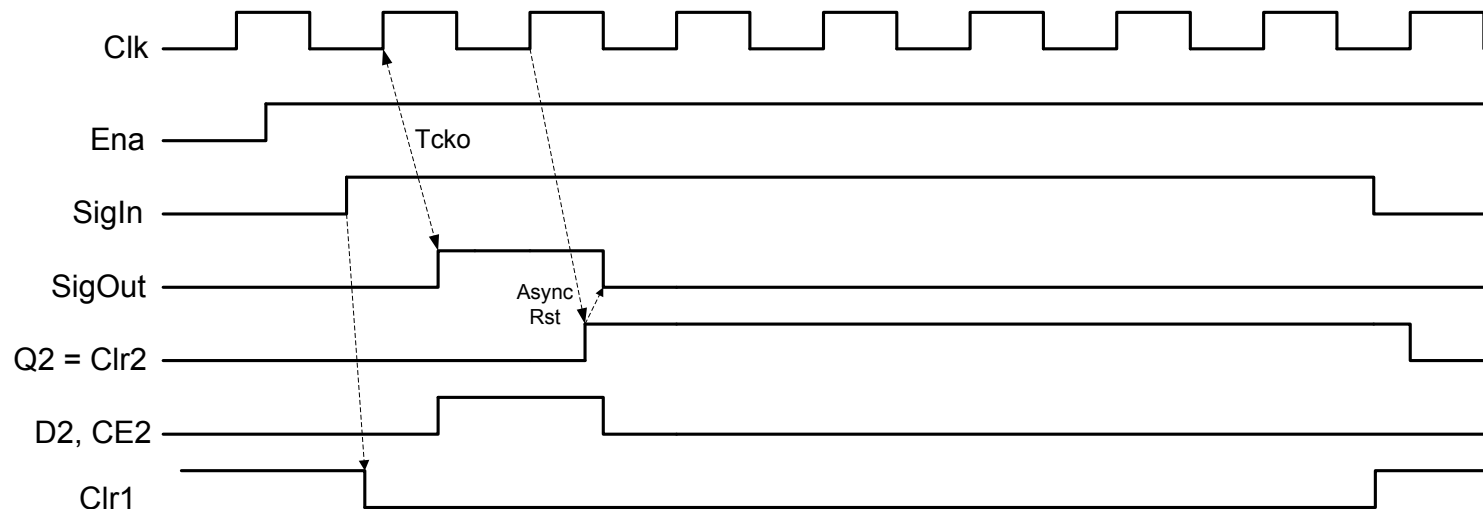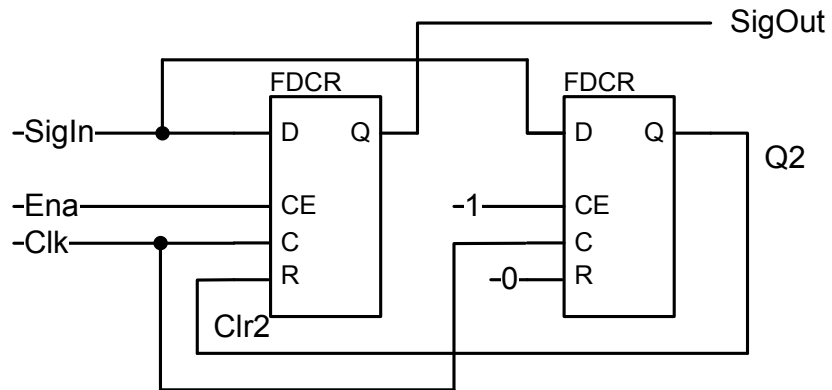
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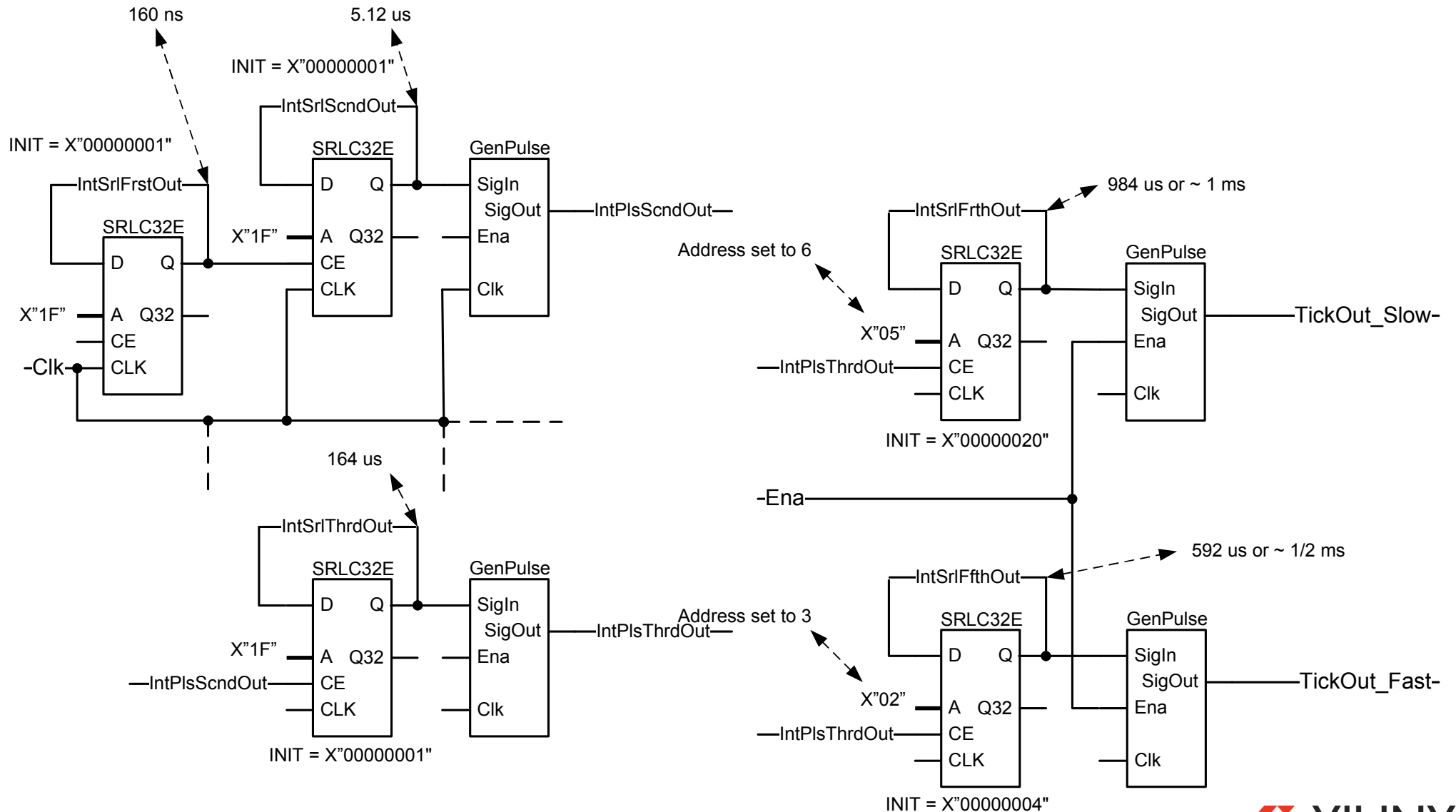
PulseGen Original Circuit
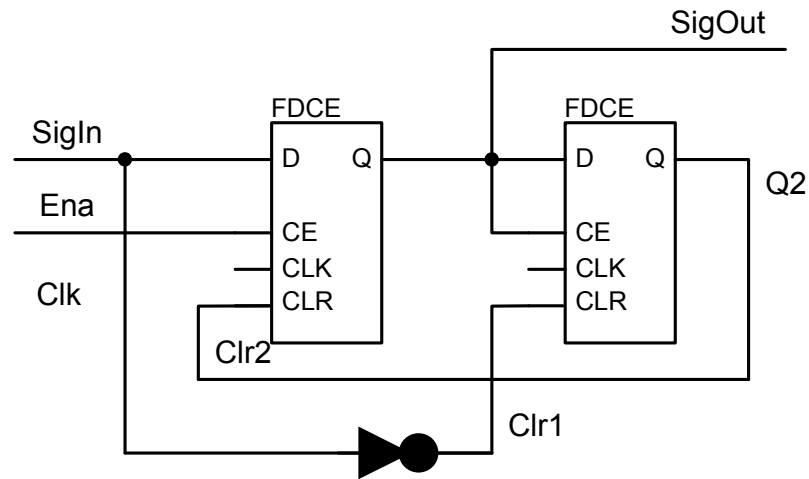
In series 7 FPGA all FFs in a SLICE use the same S/R net. Also the CE net is shared by all FFs and the slice dictates that CE for the FF is shared with WE for the LUTs (it is CE or We not both). All LUTs share the same WE inputs.
This implementation occupies two SLICES!

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7-Series circuit

FDCR is a component made with R and CE implemented in logic (LUT). This FF react synchronous, a clock edge is needed to activate CE or R.

The cirecuit provide the same result as previous circuit. Make from a high going and staying signal a one clock period wide pulse.