LogiCORE™ AXI Perf Mon IP (v1.00.a)

DS February 06, 2012 **Product Specification**

Introduction

The AXI Performance Monitor (axi_perf_mon) is for the AMBA Advanced eXtensible Interface (AXI) system. The Performance Monitor has the capability to measure major performance metrics, such as bus latency for the specific master/slave in a system and amount of memory traffic for specific durations.

The Performance Monitor Unit (PMU) designed for monitoring and analyzing system behavior on AXI bus of the multi-core system. The PMU provides monitoring hardware for counting certain events related with AXI bus transactions. The PMU is a set of hardware counters whose contents may be set and read by software and used to analyze and enhance the performance of the entire system.

Features

The AXI Performance Monitor IP contains the following features:

- AXI protocol compliant :
  - Configurable as AXI4 full or AXI4-Lite slave interface
- Interface data widths:
  - AXI4: 32, 64, 128, or 256 bits
  - AXI4-Lite: 32 bits
- 32-bit address width
- Computes performance metrics for upto 4 agents
- Consists of a free-running global clock counter
- Gives more control for the software/application in terms of getting the metrics for the system
- This core is more helpful during the development phase of an application
- Agents (Master/Slave) can be of any data width, any frequency and of any ID width

LogiCORE IP Facts					
Core Specifics					
Supported Device Family(1)	Artix-7, Kintex-7, Virtex-7,Virtex-6, Spartan-6				
Supported User Interfaces	AXI4-Lite and AXI4				
Configuration	**Resources**				**Frequency**
	Slices	LUTs	FFs	Block RAMs	Max Freq
	See Table 48 and Table 49			0	See Table 48, Table 49, Table 50
Provided with Core					
Documentation	Product Specification				
Design Files	VHDL				
Example Design	Not Provided				
Test Bench	Not Provided				
Constraints File	None				
Simulation Model	None				
Tested Design Tools					
Design Entry Tools	ISE 13.3 software				
Simulation	Mentor Graphics ModelSim(2)				
Synthesis Tools	XST 13.3				
Support					
Provided by Xilinx, Inc.					

1. For a complete list of supported derivative devices, see IDS Embedded Edition Derivative Device Support.
2. For the supported version of the tool, see the ISE Design Suite 13: Release Notes Guide.

Functional Description

The top level block diagram of the AXI Performance Monitor is is shown in Figure 1.

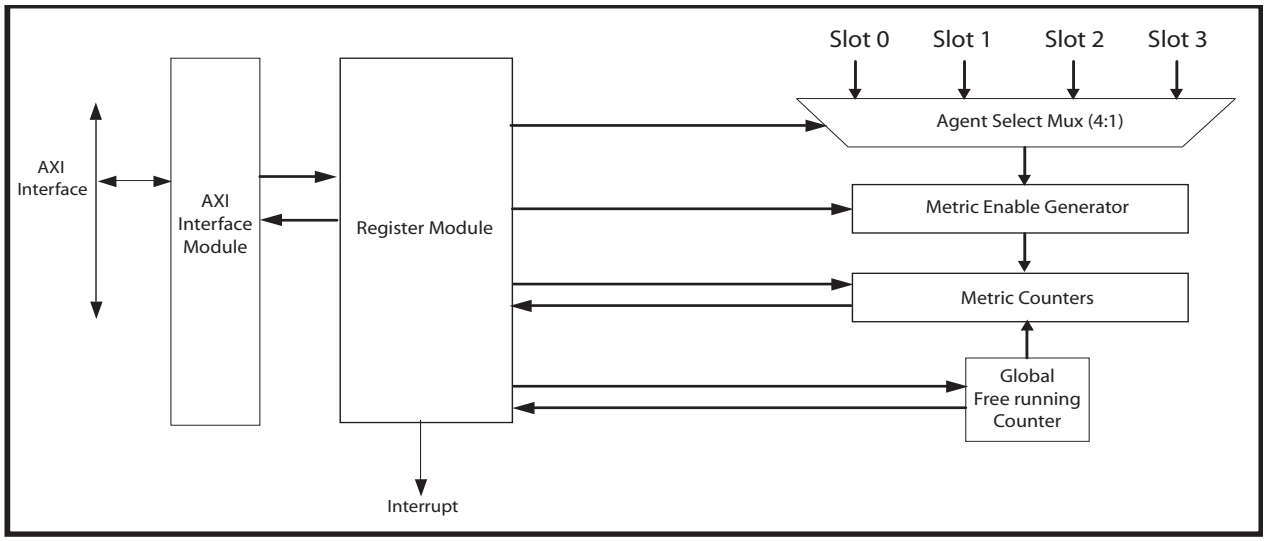

Figure 1: **Block Diagram of AXI Performance Monitor**

All the AXI signals of agents in an AXI system are connected to the monitor slots of the core. This core helps in getting the performance metrics of any chosen agent. The metrics that can be captured are categorised into 5 sets. For a single run of the application on the system, we can get one set of metrics of the chosen agent. So, in order to get all the metrics of one agent we need to run the application multiple times. This approach was taken to reduce the footprint of the core in the FPGA and give more control for the software/application.

There are a set of 10 counters in the core, which will count the events based on the selected metric set. And the events are generated based on the activities at the AXI interface of the selected agent.

The Global clock counter runs for the total application duration and will be used in calcutating the read/write latencies of an agent. It will also give the application runtime and is considered for calculating the throughput of the agent.

Configuration registers can be configured through the AXI interface the core provides. At the end of the application, the metric counters and the global clock counter are read through the same AXI interface.

The various performance metrics that can be computed and the 5 categories of metrics are described in detail in the later sections.

AXI4-Lite Interface Support

For system where burst is not supported or not required by the AXI master, this core can be configured for an AXI4-Lite interface. This configuration reduces the FPGA resource utilization. The AXI Performance Monitor supports all requests from an AXI master as per the AXI4-Lite specification. The AXI4-Lite interface is selected by configuring the parameter C_S_AXI_PROTOCOL as “AXI4LITE”.

Performance Metrics

- Each agent connected on the monitor slots can independently have data widths of 32, 64, 128, or 256 bits wide.
- Number of monitor slots in the performance monitor is 4.
- The metrics are obtained for the selected agent/slot. This selection is done through configuration register.
- Configurable read latency ranges - eight intervals. Since the read/write latency has wide distribution, such as from a couple of cycles to several hundreds of cycles , its not effective to have dedicated counters for each latency cycle. So an interval-based counting method is used for counting read/write latency effectively.
- Configurable write latency ranges - four intervals
- Metrics that are computed:
  - Write Request Count - gives the total number of write requests by/to the agent
  - Read Request Count - gives the total number of read requests given by/to the agent
  - Read Latency Distribution - gives the number of read requests that fall in eight different latency intervals
  - Write Latency Distribution - gives the number of write requests that fall in four different latency intervals
  - Write Byte Count - gives the total number of bytes written by/to the agent. This metric helps in calculating the throughput of the system.
  - Read Byte Count - gives the total number of bytes read from/by the agent
  - Average Write Latency - gives the average write latency seen by the agent
  - Average Read Latency - gives the average read latency
  - Master Write Idle Cycle Count - gives the number of idle cycles caused by the masters during write transactions to the slave
  - Slave Write Idle Cycle Count - gives the number of idle cycles caused by this slave during write transactions to the slave
  - Master Read Idle Cycle Count - gives the number of idle cycles caused by the masters during read transactions to the slave
  - Slave Read Idle Cycle Count - gives the number of idle cycles caused by this slave during read transactions to the slave
  - Global clock count - gives the number of cycles for which the application is run
- System level metrics like Write data throughput, Read data throughput, Interconnect read latency can be computed by getting all the metrics for all the agents in the system.

Use cases

- This core can be used to compute the cache hits/misses (hit ratio) and come up with optimal cache size for an application.
- To study the latencies involved for any AXI based slave like memory controller and tune the core.
- It helps in comparing different applications (facilitates in benchmarking)
- Also helps in debugging of a system (like counting the responses against requests, expected and actual requests etc...)
- To get various charts like latency distribution, throughput, burst distribution etc... for a slave and across the system.
- It will help in getting the system level metrics like write throughput, read throughput, average interconnect read latency etc...
- Gets the run time of an application and helps in optimising the software.
- Helps in analyzing the latencies involved in transactions by identifying the agent causing more idle cycles in the transactions.
- It will be helpful in comparing two similar AXI agents.

AXI Performance Monitor Limitations

- Bus contention metrics is not computed by the Performance Monitor.
- It doesn't provide the metrics for all the agents in the system in a single run of the application (as it would consume lot of logic)
- Reordering depth of 1 is only supported (The read data reordering depth is the number of addresses pending in the slave that can be reordered).
- Out of order transactions are not supported.
- Monitor Slots' clock should be synchronous to the core clock of the monitor.

Definitions, Acronyms, and Abbreviations

Table 1 provides a list of acronyms, abbreviations, and specific definitions used in this document.

Table 1: **Definitions, Acronyms, and Abbreviations**

Item	Description
AXI	The generic term for all implemented AXI protocol interfaces.
master device	An IP or device (or one of multiple interfaces on an IP) that generates AXI transactions out from the IP onto the wires connecting to a slave IP.
slave device	An IP or device (or one of multiple interfaces on an IP) that receives and responds to AXI transactions coming in to the IP from the wires connecting to a master IP.
master interface (generic)	An interface of an IP or module that generates out-bound AXI transactions and thus is the initiator (source) of an AXI transfer. On AXI master interfaces, AWVALID, ARVALID, and WVALID are outputs, and RVALID and BVALID are inputs.
slave interface (generic)	An interface of an IP or module that receives in-bound AXI transactions and becomes the target (destination) of an AXI transfer. On AXI slave interfaces, AWVALID, ARVALID, and WVALID are inputs, and RVALID and BVALID are outputs.
Slot	Slot: A slice of the Monitor Interface vector signals of the AXI Performance Monitor that connect to a single agent (master/slave).
Agent	It could be a master or slave in the AXI system.
Write Latency	Write Latecny is defined as the period needed for a master to complete the write data transaction. Write Latency does not consider the time from write address transaction to write data transaction, beacause the interval is not dependent on bus status, but on master's operating time.
Read Latency	Read Latency is defined as the time from start of read address transaction to the beginning of read data service.
Latency Range	Because the read/write latency has wide distribution, we can use an interval based counting for measuring read and write latency effectively.

I/O Signals

This section lists the AXI Performance Monitor signals.

The different kinds of I/O signals are AXI interface signals through which the IP is configured and registers are read, Monitor slot I/O signals to which the agents (masters/slaves) that need to be monitored are connected. The following tables (Table 3, Table 4, page 10, Table 4, page 9, Table 6, page 12, Table 7, page 13, and Table 8, page 15) detail the pins and their description.

AXI4 / AXI4-Lite I/O signals

Table 2: **AXI4 / AXI4-Lite I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
AXI Interface System Signals					
P1	S_AXI_ACLK	System	I	-	AXI clock
P2	S_AXI_ARESETN	System	I	-	AXI reset, active low
AXI Write Address Channel Signals					
P3	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	AXI4	I	-	AXI Write address. The write address bus gives the address of the first transfer in a write burst transaction

Table 2: **AXI4 / AXI4-Lite I/O Signal Description *(Cont.)***

Port	Signal Name	Interface	I/O	Initial State	Description
P4	S_AXI_AWPROT[2:0][(1)]	AXI4	I	-	Protection type. This signal indicates the normal, privileged, or secure protection level of the write transaction and whether the transaction is a data access or an instruction access. The default value is normal non secure data access
P5	S_AXI_AWVALID	AXI4	I	-	Write address valid. This signal indicates that valid write address and control information are available
P6	S_AXI_AWREADY	AXI4	O	0	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
AXI Write Data Channel Signals					
P7	S_AXI_WDATA[C_S_AXI_DATA_WIDTH-1:0]	AXI4	I	-	Write data bus
P8	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0][(1)]	AXI4	I	-	Write strobes. This signal indicates which byte lanes to update in memory
P10	S_AXI_WVALID	AXI4	I	-	Write valid. This signal indicates that valid write data and strobes are available
P11	S_AXI_WREADY	AXI4	O	0	Write ready. This signal indicates that the slave can accept the write data
AXI Write Response Channel Signals					
P12	S_AXI_BRESP[1:0]	AXI4	O	0	Write response. This signal indicates the status of the write transaction
P13	S_AXI_BVALID	AXI4	O	0	Write response valid. This signal indicates that a valid write response is available
P14	S_AXI_BREADY	AXI4	I	-	Response ready. This signal indicates that the master can accept the response information
AXI Read Address Channel Signals					
P15	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH -1:0]	AXI4	I	-	Read address. The read address bus gives the initial address of a read burst transaction
P16	S_AXI_ARPROT[2:0][(1)]	AXI4	I	-	Protection type. This signal provides protection unit information for the read transaction. The default value is normal non secure data access
P17	S_AXI_ARVALID	AXI4	I	-	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledgement signal, S_AXI_ARREDY, is high.
P18	S_AXI_ARREADY	AXI4	O	0	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Read Data Channel Signals					
P19	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	AXI4	O	0	Read data bus
P20	S_AXI_RRESP[1:0]	AXI4	O	0	Read response. This signal indicates the status of the read transfer.

Table 2: **AXI4 / AXI4-Lite I/O Signal Description *(Cont.)***

Port	Signal Name	Interface	I/O	Initial State	Description
P21	S_AXI_RVALID	AXI4	O	0	Read valid. This signal indicates that the required read data is available and the read transfer can complete
P22	S_AXI_RREADY	AXI4	I	-	Read ready. This signal indicates that the master can accept the read data and response information

Notes:

Monitor Slot 0 I/O Signals

Table 3 lists the Monitor Slot 0 Interface signals.

Table 3: **Monitor Slot 0 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXI_ACLK	Input	1	AXI Clock
SLOT_0_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_0_AXI_AWID	Input	C_SLOT_0_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_0_AXI_AWADDR	Input	C_SLOT_0_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_0_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_0_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_0_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2).
SLOT_0_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_0_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_0_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_0_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_0_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_0_AXI_WDATA	Input	C_SLOT_0_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_0_AXI_WSTRB	Input	C_SLOT_0_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_0_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_0_AXI_WVALID	Input	1	Write Data Channel Valid.
SLOT_0_AXI_WREADY	Input	1	Write Data Channel Ready.

Table 3: **Monitor Slot 0 I/O Signals *(Cont.)***

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXI_BID	Input	C_SLOT_0_AXI_ID_WIDTH	Write Response Channel Transaction ID.
SLOT_0_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3).
SLOT_0_AXI_BVALID	Input	1	Write Response Channel Valid.
SLOT_0_AXI_BREADY	Input	1	Write Response Channel Ready.
SLOT_0_AXI_ARID	Input	C_SLOT_0_AXI_ID_WIDTH	Read Address Channel Transaction ID.
SLOT_0_AXI_ARADDR	Input	C_SLOT_0_AXI_ADDR_WIDTH	Read Address Channel Address.
SLOT_0_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255).
SLOT_0_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7).
SLOT_0_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2).
SLOT_0_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1).
SLOT_0_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics.
SLOT_0_AXI_ARPROT	Input	3	Read Address Channel Protection Bits.
SLOT_0_AXI_ARVALID	Input	1	Read Address Channel Valid.
SLOT_0_AXI_ARREADY	Input	1	Read Address Channel Ready.
SLOT_0_AXI_RID	Input	C_SLOT_0_AXI_ID_WIDTH	Read Data Channel Transaction ID.
SLOT_0_AXI_RDATA	Input	C_SLOT_0_AXI_DATA_WIDTH	Read Data Channel Data.
SLOT_0_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3).
SLOT_0_AXI_RLAST	Input	1	Read Data Channel Last Data Beat.
SLOT_0_AXI_RVALID	Input	1	Read Data Channel Valid.
SLOT_0_AXI_RREADY	Input	1	Read Data Channel Ready.

Monitor Slot 1 I/O Signals

Table 3 lists the Monitor Slot 1 Interface signals.

Table 4: **Monitor Slot 1 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_1_AXI_ACLK	Input	1	AXI Clock
SLOT_1_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_1_AXI_AWID	Input	C_SLOT_1_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_1_AXI_AWADDR	Input	C_SLOT_1_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_1_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_1_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_1_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2).
SLOT_1_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_1_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_1_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_1_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_1_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_1_AXI_WDATA	Input	C_SLOT_1_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_1_AXI_WSTRB	Input	C_SLOT_1_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_1_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_1_AXI_WVALID	Input	1	Write Data Channel Valid.
SLOT_1_AXI_WREADY	Input	1	Write Data Channel Ready.
SLOT_1_AXI_BID	Input	C_SLOT_1_AXI_ID_WIDTH	Write Response Channel Transaction ID.
SLOT_1_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3).
SLOT_1_AXI_BVALID	Input	1	Write Response Channel Valid.
SLOT_1_AXI_BREADY	Input	1	Write Response Channel Ready.
SLOT_1_AXI_ARID	Input	C_SLOT_1_AXI_ID_WIDTH	Read Address Channel Transaction ID.

Table 4: **Monitor Slot 1 I/O Signals *(Cont.)***

Signal Name	Direction	Width	Description (Range)
SLOT_1_AXI_ARADDR	Input	C_SLOT_1_AXI_ADDR_WIDTH	Read Address Channel Address.
SLOT_1_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255).
SLOT_1_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7).
SLOT_1_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2).
SLOT_1_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1).
SLOT_1_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics.
SLOT_1_AXI_ARPROT	Input	3	Read Address Channel Protection Bits.
SLOT_1_AXI_ARVALID	Input	1	Read Address Channel Valid.
SLOT_1_AXI_ARREADY	Input	1	Read Address Channel Ready.
SLOT_1_AXI_RID	Input	C_SLOT_1_AXI_ID_WIDTH	Read Data Channel Transaction ID.
SLOT_1_AXI_RDATA	Input	C_SLOT_1_AXI_DATA_WIDTH	Read Data Channel Data.
SLOT_1_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3).
SLOT_1_AXI_RLAST	Input	1	Read Data Channel Last Data Beat.
SLOT_1_AXI_RVALID	Input	1	Read Data Channel Valid.
SLOT_1_AXI_RREADY	Input	1	Read Data Channel Ready.

Monitor Slot 2 I/O Signals

Table 3 lists the Monitor Slot 2 Interface signals.

Table 5: **Monitor Slot 2 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_ACLK	Input	1	AXI Clock
SLOT_2_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_2_AXI_AWID	Input	C_SLOT_2_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_2_AXI_AWADDR	Input	C_SLOT_2_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_2_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)

Table 5: **Monitor Slot 2 I/O Signals *(Cont.)***

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_2_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2).
SLOT_2_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_2_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_2_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_2_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_2_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_2_AXI_WDATA	Input	C_SLOT_2_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_2_AXI_WSTRB	Input	C_SLOT_2_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_2_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_2_AXI_WVALID	Input	1	Write Data Channel Valid.
SLOT_2_AXI_WREADY	Input	1	Write Data Channel Ready.
SLOT_2_AXI_BID	Input	C_SLOT_2_AXI_ID_WIDTH	Write Response Channel Transaction ID.
SLOT_2_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3).
SLOT_2_AXI_BVALID	Input	1	Write Response Channel Valid.
SLOT_2_AXI_BREADY	Input	1	Write Response Channel Ready.
SLOT_2_AXI_ARID	Input	C_SLOT_2_AXI_ID_WIDTH	Read Address Channel Transaction ID.
SLOT_2_AXI_ARADDR	Input	C_SLOT_2_AXI_ADDR_WIDTH	Read Address Channel Address.
SLOT_2_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255).
SLOT_2_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7).
SLOT_2_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2).
SLOT_2_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1).
SLOT_2_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics.
SLOT_2_AXI_ARPROT	Input	3	Read Address Channel Protection Bits.
SLOT_2_AXI_ARVALID	Input	1	Read Address Channel Valid.

Table 5: **Monitor Slot 2 I/O Signals *(Cont.)***

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_ARREADY	Input	1	Read Address Channel Ready.
SLOT_2_AXI_RID	Input	C_SLOT_2_AXI_ID_WIDTH	Read Data Channel Transaction ID.
SLOT_2_AXI_RDATA	Input	C_SLOT_2_AXI_DATA_WIDTH	Read Data Channel Data.
SLOT_2_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3).
SLOT_2_AXI_RLAST	Input	1	Read Data Channel Last Data Beat.
SLOT_2_AXI_RVALID	Input	1	Read Data Channel Valid.
SLOT_2_AXI_RREADY	Input	1	Read Data Channel Ready.

Monitor Slot 3 I/O Signals

Table 3 lists the Monitor Slot 3 Interface signals.

Table 6: **Monitor Slot 3 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_3_AXI_ACLK	Input	1	AXI Clock
SLOT_3_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_3_AXI_AWID	Input	C_SLOT_3_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_3_AXI_AWADDR	Input	C_SLOT_3_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_3_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_3_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_3_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2).
SLOT_3_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_3_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_3_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_3_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_3_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_3_AXI_WDATA	Input	C_SLOT_3_AXI_DATA_WIDTH	Write Data Channel Data

Table 6: **Monitor Slot 3 I/O Signals *(Cont.)***

Signal Name	Direction	Width	Description (Range)
SLOT_3_AXI_WSTRB	Input	C_SLOT_3_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_3_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_3_AXI_WVALID	Input	1	Write Data Channel Valid.
SLOT_3_AXI_WREADY	Input	1	Write Data Channel Ready.
SLOT_3_AXI_BID	Input	C_SLOT_3_AXI_ID_WIDTH	Write Response Channel Transaction ID.
SLOT_3_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3).
SLOT_3_AXI_BVALID	Input	1	Write Response Channel Valid.
SLOT_3_AXI_BREADY	Input	1	Write Response Channel Ready.
SLOT_3_AXI_ARID	Input	C_SLOT_3_AXI_ID_WIDTH	Read Address Channel Transaction ID.
SLOT_3_AXI_ARADDR	Input	C_SLOT_3_AXI_ADDR_WIDTH	Read Address Channel Address.
SLOT_3_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255).
SLOT_3_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7).
SLOT_3_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2).
SLOT_3_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1).
SLOT_3_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics.
SLOT_3_AXI_ARPROT	Input	3	Read Address Channel Protection Bits.
SLOT_3_AXI_ARVALID	Input	1	Read Address Channel Valid.
SLOT_3_AXI_ARREADY	Input	1	Read Address Channel Ready.
SLOT_3_AXI_RID	Input	C_SLOT_3_AXI_ID_WIDTH	Read Data Channel Transaction ID.
SLOT_3_AXI_RDATA	Input	C_SLOT_3_AXI_DATA_WIDTH	Read Data Channel Data.
SLOT_3_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3).
SLOT_3_AXI_RLAST	Input	1	Read Data Channel Last Data Beat.
SLOT_3_AXI_RVALID	Input	1	Read Data Channel Valid.
SLOT_3_AXI_RREADY	Input	1	Read Data Channel Ready.

Core Signals

Table 3 lists the core signals.

Table 7: **Core I/O Signals**

Signal Name	Direction	Width	Description (Range)
CORE_ACLK	Input	1	Core Clock -Highest frequency clock in the system (Interconnect clock)
CORE_ARESETN	Input	1	Active Low Reset - Reset of the slowest clock domain in the system

Design Parameters

T

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6	virtex6	string
G2	AXI Base Address	C_BASEADDR	Valid Address(1)	0xFFFFFFFF(3)	std_logic_vector
G3	AXI High Address	C_HIGHADDR	Valid Address(2)	0x00000000(3)	std_logic_vector
AXI Interface Parameters					
G4	AXI Identification tag width	C_S_AXI_ID_WIDTH	1-16	4	integer
G5	AXI most significant address bus width	C_S_AXI_ADDR_WIDTH	32	32	integer
G6	AXI data bus width	C_S_AXI_DATA_WIDTH	32, 64	32	integer
G7	AXI protocol	C_S_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
SLOT 0 Monitor Interface Parameters					
G8	SLOT 0 AXI Identification tag width	C_SLOT_0_AXI_ID_WIDTH	1-16	4	integer
G9	SLOT 0 AXI address bus width	C_SLOT_0_AXI_ADDR_WIDTH	32	32	integer
G10	SLOT 0 AXI data bus width	C_SLOT_0_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G11	SLOT 0 AXI protocol	C_SLOT_0_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G12	SLOT 0 AXI clock div value	C_SLOT_0_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
SLOT 1 Monitor Interface Parameters					
G13	SLOT 1 AXI Identification tag width	C_SLOT_1_AXI_ID_WIDTH	1-16	4	integer
G14	SLOT 1 AXI address bus width	C_SLOT_1_AXI_ADDR_WIDTH	32	32	integer
G15	SLOT 1 AXI data bus width	C_SLOT_1_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G16	SLOT 1 AXI protocol	C_SLOT_1_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G17	SLOT 1 AXI clock div value	C_SLOT_1_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
SLOT 2 Monitor Interface Parameters					
G18	SLOT 2 AXI Identification tag width	C_SLOT_2_AXI_ID_WIDTH	1-16	4	integer
G19	SLOT 2 AXI address bus width	C_SLOT_2_AXI_ADDR_WIDTH	32	32	integer
G20	SLOT 2 AXI data bus width	C_SLOT_2_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G21	SLOT 2 AXI protocol	C_SLOT_2_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G22	SLOT 2 AXI clock div value	C_SLOT_2_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
SLOT 3 Monitor Interface Parameters					
G23	SLOT 3 AXI Identification tag width	C_SLOT_3_AXI_ID_WIDTH	1-16	4	integer
G24	SLOT 3 AXI address bus width	C_SLOT_3_AXI_ADDR_WIDTH	32	32	integer
G25	SLOT 3 AXI data bus width	C_SLOT_3_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G26	SLOT 3 AXI protocol	C_SLOT_3_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G27	SLOT 3 AXI clock div value	C_SLOT_3_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
Monitor Slots Maximum Widths					
G28	Maximum width of AXI Identification tag	C_MON_SLOTS_AXI_ID_MAX_WIDTH	1-16	4	integer
G29	Maximum AXI address bus width	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	32	32	integer
G30	Maximim AXI data bus width	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	32, 64, 128, 256	32	integer
Counter Width and max outstanding Parameters					
G31	Width of all the counters inside the monitors	C_METRIC_COUNT_WIDTH	32, 64	32	integer
G32	Width of the Global Free running counter	C_GLOBAL_COUNT_WIDTH	32, 64, 128	32	integer
G33	Maximum Number of outstanding requests given/taken by any agent in the system	C_MAX_OUTSTAND_DEPTH	1-16	1	integer

Notes:

1. The user must set values.
2. The range specified by C_HIGHADDR - C_BASEADDR must be a power of 2 and greater than equal to C_BASEADDR + 0x1FFF.
3. An invalid default value will be specified to insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated.

Register Descriptions

This section tabulates the registers of AXI Performance Monitor core and their reset values. Table 8 shows all the AXI Performance Monitor registers and their addresses.

Table 8: **Registers**

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0000	Control Register	Write	0x0	Control Register
C_BASEADDR + 0x0004	Read Latency Range A Register	Write	0x0	Read Latency Range A Register
C_BASEADDR + 0x0008	Read Latency Range B Register	Write	0x0	Read Latency Range B Register
C_BASEADDR + 0x000C	Read Latency Range C Register	Write	0x0	Read Latency Range C Register
C_BASEADDR + 0x0010	Read Latency Range D Register	Write	0x0	Read Latency Range D Register
C_BASEADDR + 0x0014	Write Latency Range A Register	Write	0x0	Write Latency Range A Register
C_BASEADDR + 0x0018	Write Latency Range B Register	Write	0x0	Write Latency Range B Register
C_BASEADDR + 0x0024	Metric Selector Register	Write	0x0	Metric Selector register
C_BASEADDR + 0x1000	Metric Counter 0(1)	Read	0x0	Higher 32-bit data of the Metric Counter 0 Register
C_BASEADDR + 0x1004	Metric Counter 0	Read	0x0	Lower 32-bit data of the Metric Counter 0 Register
C_BASEADDR + 0x1008	Metric Counter 1(1)	Read	0x0	Higher 32-bit data of the Metric Counter 1 Register
C_BASEADDR + 0x100C	Metric Counter 1	Read	0x0	Lower 32-bit data of the Metric Counter 1 Register
C_BASEADDR + 0x1010	Metric Counter 2(1)	Read	0x0	Higher 32-bit data of the Metric Counter 2 Register
C_BASEADDR + 0x1014	Metric Counter 2	Read	0x0	Lower 32-bit data of the Metric Counter 2 Register
C_BASEADDR + 0x1018	Metric Counter 3(1)	Read	0x0	Higher 32-bit data of the Metric Counter 3 Register
C_BASEADDR + 0x101C	Metric Counter 3	Read	0x0	Lower 32-bit data of the Metric Counter 3 Register
C_BASEADDR + 0x1020	Metric Counter 4(1)	Read	0x0	Higher 32-bit data of the Metric Counter 4 Register
C_BASEADDR + 0x1024	Metric Counter 4	Read	0x0	Lower 32-bit data of the Metric Counter 4 Register

Table 8: **Registers**

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x1028	Metric Counter 5(1)	Read	0x0	Higher 32-bit data of the Metric Counter 5 Register
C_BASEADDR + 0x102C	Metric Counter 5	Read	0x0	Lower 32-bit data of the Metric Counter 5 Register
C_BASEADDR + 0x1030	Metric Counter 6(1)	Read	0x0	Higher 32-bit data of the Metric Counter 6 Register
C_BASEADDR + 0x1034	Metric Counter 6	Read	0x0	Lower 32-bit data of the Metric Counter 6 Register
C_BASEADDR + 0x1038	Metric Counter 7(1)	Read	0x0	Higher 32-bit data of the Metric Counter 7 Register
C_BASEADDR + 0x103C	Metric Counter 7	Read	0x0	Lower 32-bit data of the Metric Counter 7 Register
C_BASEADDR + 0x1040	Metric Counter 8(1)	Read	0x0	Higher 32-bit data of the Metric Counter 8 Register
C_BASEADDR + 0x1044	Metric Counter 8	Read	0x0	Lower 32-bit data of the Metric Counter 8 Register
C_BASEADDR + 0x1048	Metric Counter 9(1)	Read	0x0	Higher 32-bit data of the Metric Counter 9 Register
C_BASEADDR + 0x104C	Metric Counter 9	Read	0x0	Lower 32-bit data of the Metric Counter 9 Register
C_BASEADDR + 0x0808	Global Clock Counter	Read	0x0	Higher 32-bit data of the Global Clock Counter Register
C_BASEADDR + 0x080C	Global Clock Counter	Read	0x0	Lower 32-bit data of the Global Clock Counter Register

Notes:

1. These registers are valid only if C_METRIC_COUNT_WIDTH is 64.

Control Register

The Control Register is a 32-bit register as shown in Figure 2. This register is used to enable the global free running counter and metrics counters inside the core. The bit definition and accessibility of this register is shown in Table 8.

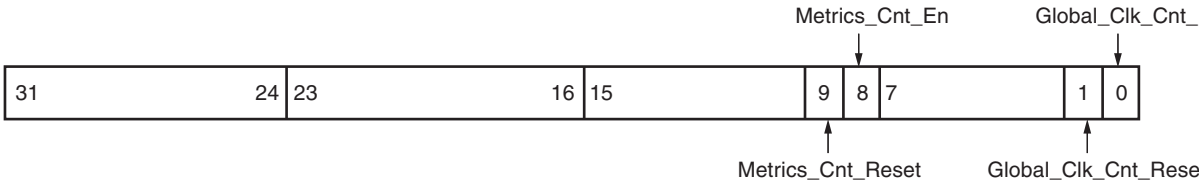

Figure 2: **Control Register**

Table 9: **Control Register Bit Definitions (C_BASEADDR + 0x0000)**

Bit	Name	Access	Reset value	Description
31-10	Reserved	N/A	N/A	Reserved
9	Metrics_Cnt_Reset	Read/Write	'0'	1: Resets all the metrics counters in the monitor.
8	Metrics_Cnt_En	Read/Write	'0'	1: Enables all the metrics counters in the monitor.
7-2	Reserved	N/A	N/A	Reserved
1	Global_Clk_Cnt_Reset	Read/Write	'0'	1: Resets the free-running Global Clock Counter
0	Global_Clk_Cnt_En	Read/Write	'0'	1: Enables the free-running Global Clock Counter

Note:-

1.

Read Latency Range A Register

The Read Latency Range A Register is a 32-bit register as shown in Figure 3. This register is used to store two read latency ranges. The bit definition and accessibility of this register is shown in Table 10.

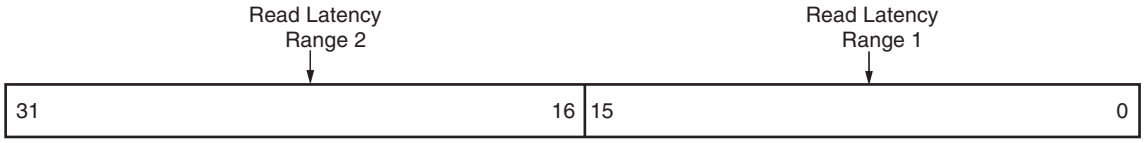

Figure 3: **Read Latency Range A Register**

Table 10: **Read Latency Range A Register Bit Definitions (C_BASEADDR + 0x0004)**

Bit	Name	Access	Reset value	Description
31-16	Read Latency Range 2	Write	"0x00"	This is Read Latency Range 2, i.e. the read transactions with latency that falls between Read Latency Range 1 and this value are said to be having Range 2 Latency
15-0	Read Latency Range 1	Write	"0x00"	This is Read Latency Range 1, i.e. the read transactions with latency that falls between 0 and this value are said to be having Range 1 Latency

Read Latency Range B Register

The Read Latency Range B Register is a 32-bit register as shown in Figure 3. This register is used to store two read latency ranges. The bit definition and accessibility of this register is shown in Table 10.

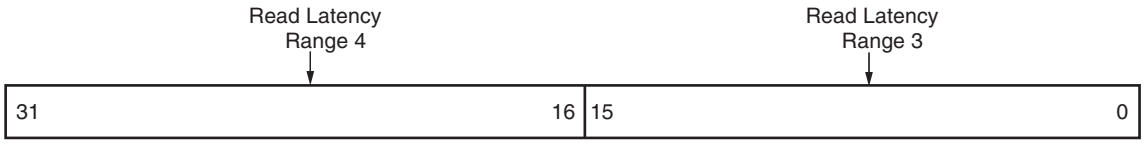

Figure 4: **Read Latency Range B Register**

Table 11: **Read Latency Range B Register Bit Definitions (C_BASEADDR + 0x0008)**

Bit	Name	Access	Reset value	Description
31-16	Read Latency Range 4	Read/Write	“0x50”	This is Read Latency Range 4, i.e. the read transactions with latency that falls between Read Latency Range 3 and this value are said to be having Range 4 Latency
15-0	Read Latency Range 3	Read/Write	“0x40”	This is Read Latency Range 3, i.e. the read transactions with latency that falls between Read Latency Range 2 and this value are said to be having Range 3 Latency

Read Latency Range C Register

The Read Latency Range C Register is a 32-bit register as shown in Figure 3. This register is used to store two read latency ranges. The bit definition and accessibility of this register is shown in Table 10.

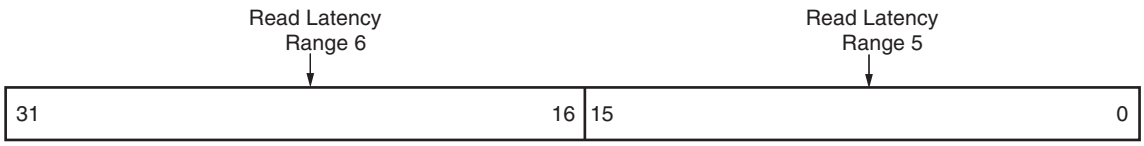

Figure 5: **Read Latency Range C Register**

Table 12: **Read Latency Range C Register Bit Definitions (C_BASEADDR + 0x000C)**

Bit	Name	Access	Reset value	Description
31-16	Read Latency Range 6	Read/Write	“0x00”	This is Read Latency Range 6, i.e. the read transactions with latency that falls between Read Latency Range 5 and this value are said to be having Range 6 Latency
15-0	Read Latency Range 5	Read/Write	“0x00”	This is Read Latency Range 5, i.e. the read transactions with latency that falls between Read Latency Range 4 and this value are said to be having Range 5 Latency

Read Latency Range D Register

The Read Latency Range D Register is a 32-bit register as shown in Figure 3. This register is used to store two read latency ranges. The bit definition and accessibility of this register is shown in Table 10.

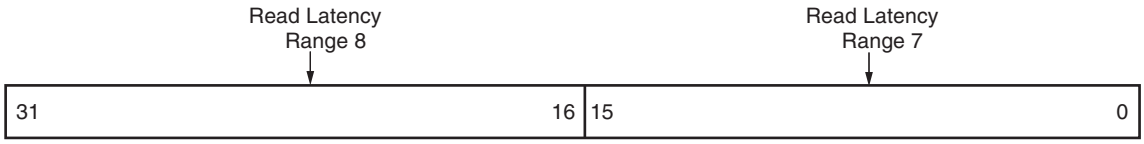

Figure 6: **Read Latency Range D Register**

Table 13: **Read Latency Range D Register Bit Definitions (C_BASEADDR + 0x0010)**

Bit	Name	Access	Reset value	Description
31-16	Read Latency Range 8	Read/Write	“0x00”	This is Read Latency Range 8, i.e. the read transactions with latency that falls between Read Latency Range 7 and this value are said to be having Range 8 Latency
15-0	Read Latency Range 7	Read/Write	“0x00”	This is Read Latency Range 7, i.e. the read transactions with latency that falls between Read Latency Range 6 and this value are said to be having Range 7 Latency

Write Latency Range A Register

The Write Latency Range A Register is a 32-bit register as shown in Figure 3. This register is used to store two Write latency ranges. The bit definition and accessibility of this register is shown in Table 10.

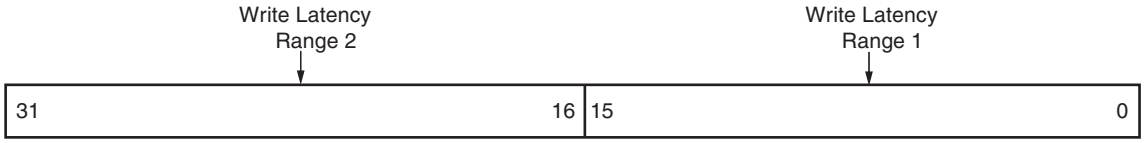

Figure 7: **Write Latency Range A Register**

Table 14: **Write Latency Range A Register Bit Definitions (C_BASEADDR + 0x0014)**

Bit	Name	Access	Reset value	Description
31-16	Write Latency Range 2	Read/Write	“0x00”	This is Write Latency Range 2, i.e. the Write transactions with latency that falls between Write Latency Range 1 and this value are said to be having Range 2 Latency
15-0	Write Latency Range 1	Read/Write	“0x00”	This is Write Latency Range 1, i.e. the Write transactions with latency that falls between 0 and this value are said to be having Range 1 Latency

Write Latency Range B Register

The Write Latency Range B Register is a 32-bit register as shown in Figure 3. This register is used to store two Write latency ranges. The bit definition and accessibility of this register is shown in Table 10.

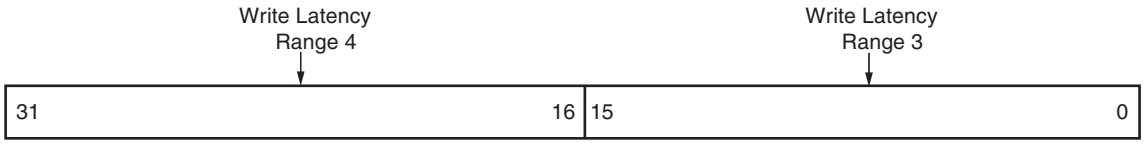

Figure 8: **Write Latency Range B Register**

Table 15: **Write Latency Range A Register Bit Definitions (C_BASEADDR + 0x0018)**

Bit	Name	Access	Reset value	Description
31-16	Write Latency Range 4	Read/Write	“0x00”	This is Write Latency Range 4, i.e. the Write transactions with latency that falls between Write Latency Range 3 and this value are said to be having Range 4 Latency
15-0	Write Latency Range 3	Read/Write	“0x00”	This is Write Latency Range 3, i.e. the Write transactions with latency that falls between Write Latency Range 2 and this value are said to be having Range 3 Latency

Metric Selector Register

The Metric Selector Register is a 32-bit register as shown in Figure 10. This register is used to select the metric set and the agent for which the metrics need to be computed. The bit definition and accessibility of this register is shown in Table 8.

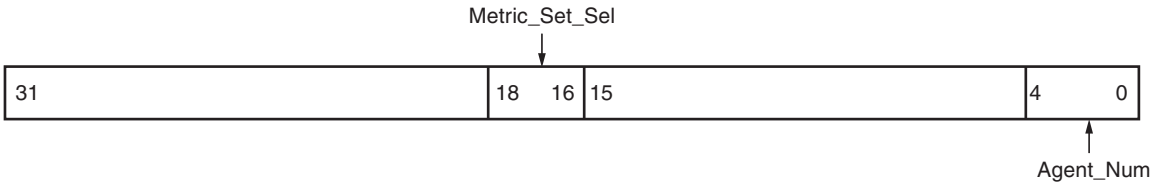

Figure 9: **Metric Selector Register**

Table 16: **Metric Selector Register Bit Definitions (C_BASEADDR + 0x0024)**

Bit	Name	Access	Reset value	Description
31-19	Reserved	N/A	N/A	Reserved
18-16	Metric_Set_Sel	Write	x”0”	b000: Set 0 of metrics b001: Set 1 of metrics b010: Set 2 of metrics b011: Set 3 of metrics b100: Set 4 of metrics
15-5	Reserved	N/A	N/A	Reserved
4-0	Agent_Num	Write	x“00”	Agent Number is the slot number for which the metrics would be computed. Agent Number should be lesser than the num of monitor slots.

Note:-

1.

Global Clock Count Register

The Global Clock Count is a 32/64/128-bit read register as shown in Figure 2. This register holds the information of the total number of simulation cycles. The bit definition and accessibility of this register is shown in Table 8.

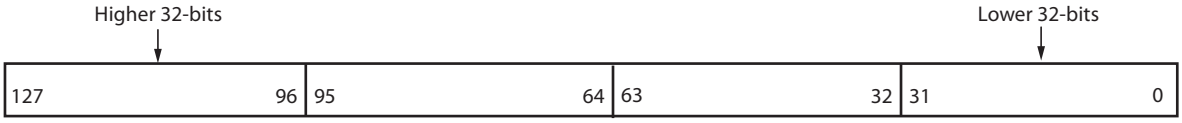

Figure 10: **Global Clock Count Register**

Table 17: **Global Clock Count Register Bit Definitions (C_BASEADDR + 0x0800)**

Bit	Name	Access	Reset value	Description
127-96	Global Clock Count	Read	“0x00”	Higher 32-bits of Global Clock Count Register
95-64	Global Clock Count	Read	“0x00”	[95:64] bits of Global Clock Count Register
63-32	Global Clock Count	Read	“0x00”	[63:32] bits of Global Clock Count Register
31-0	Global Clock Count	Read	“0x00”	Lower 32-bits of Global Clock Count Register

Note:-

2. If parameter C_S_AXI_DATA_WIDTH is 32, then the register can be read by doing a read transaction to 4 locations, i.e. to (C_BASEADDR + 0x800), (C_BASEADDR + 0x804), (C_BASEADDR + 0x808) and (C_BASEADDR + 0x80C) locations
3. If C_GLOBAL_COUNT_WIDTH=32, then only lower 32-bits of the register are valid
4. If C_GLOBAL_COUNT_WIDTH=64, then only lower 64-bits of the register are valid

Metric Counter Registers

Metric Counter	Set 0 (Metric_Set_Sel =b000)	Set 1 (Metric_Set_Sel = b001)	Set 2 (Metric_Set_Sel = b010)
Metric Counter 0	Read Latency Range 1	Write Latency Range 1	Num_Wr_Reqs
Metric Counter 1	Read Latency Range 2	Write Latency Range 2	Num_Rd_Reqs
Metric Counter 2	Read Latency Range 3	Write Latency Range 3	Slv_Wr_Idle_Cnt
Metric Counter 3	Read Latency Range 4	Write Latency Range 4	Mst_Rd_Idle_Cnt
Metric Counter 4	Read Latency Range 5	Write Latency Range 5	Num_BValids
Metric Counter 5	Read Latency Range 6	Num_Wr_Reqs	Num_WLasts
Metric Counter 6	Read Latency Range 7	Num_Rd_Reqs	Num_RLasts
Metric Counter 7	Read Latency Range 8	Write Byte Count	Num_Wr_Bursts_Len0
Metric Counter 8	Read Latency Range 9	Read Byte Count	Num_Rd_Bursts_Len0
Metric Counter 9	Total Read Latency	Total Write Latency	Total Write Latency

Note:-

5.

Metric Counter	Set 3 (Metric_Set_Sel =b011)	Set 4 (Metric_Set_Sel = b100)	Set 5 (Metric_Set_Sel = b101)
Metric Counter 0	Read Latency Range 1	Write Latency Range 1	Num_Wr_Reqs
Metric Counter 1	Read Latency Range 2	Write Latency Range 2	Num_Rd_Reqs
Metric Counter 2	Read Latency Range 3	Write Latency Range 3	Slv_Wr_Idle_Cnt
Metric Counter 3	Read Latency Range 4	Write Latency Range 4	Mst_Rd_Idle_Cnt
Metric Counter 4	Read Latency Range 5	Write Latency Range 5	Num_BValids
Metric Counter 5	Num_Rd_Reqs	Num_Wr_Reqs	Num_WLasts
Metric Counter 6	Num_RLasts	Num_WLasts	Num_RLasts
Metric Counter 7	Num_Rd_Bursts_Len0	Num_BValids	Num_BValids
Metric Counter 8	Read Byte Count	Write Byte Count	Num_Rd_Bursts_Len0
Metric Counter 9	Total Read Latency	Total Write Latency	Total Write Latency

Note:-

6.

The metric counters give different metrics based on the metric set chosen in the metric selector register.

Each of the metrics is explained in the sections below.

Read Latency Range 1

The Read Latency Range 1 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 1.

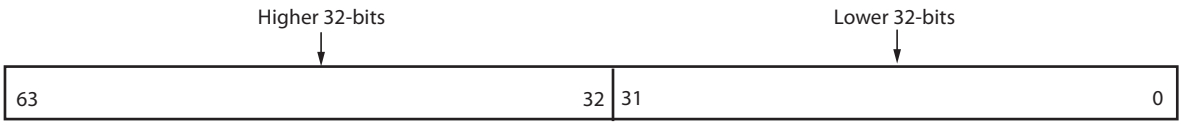

Figure 11: **Read Latency Range 1**

Table 18: **Read Latency Range 1 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 1	Read	“0x00”	Higher 32-bits of Read Latency Range 1.
31-0	Read Latency Range 1	Read	“0x00”	Lower 32-bits of Read Latency Range 1.

7.

Read Latency Range 2

The Read Latency Range 2 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 2.

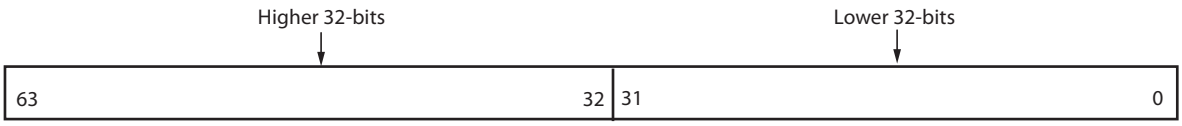

Figure 12: **Read Latency Range 2**

Table 19: **Read Latency Range 2 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 2	Read	“0x00”	Higher 32-bits of Read Latency Range 2 .
31-0	Read Latency Range 2	Read	“0x00”	Lower 32-bits of Read Latency Range 2 .

8.

Read Latency Range 3

The Read Latency Range 3 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 3.

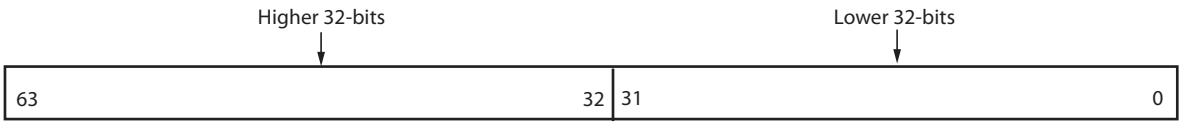

Figure 13: **Read Latency Range 3**

Table 20: **Read Latency Range 3 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 3	Read	“0x00”	Higher 32-bits of Read Latency Range 3 .
31-0	Read Latency Range 3	Read	“0x00”	Lower 32-bits of Read Latency Range 3 .

9.

Read Latency Range 4 Register

The Read Latency Range 4 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 4. The bit definition and accessibility of this register is shown in Table 8.

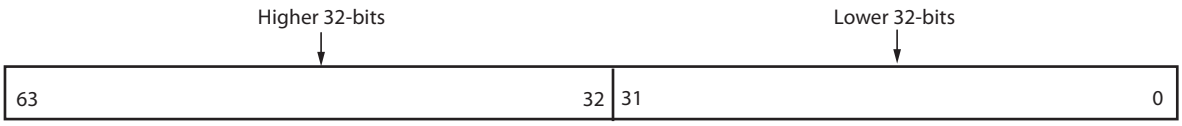

Figure 14: **Read Latency Range 4**

Table 21: **Read Latency Range 4 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 4	Read	“0x00”	Higher 32-bits of Read Latency Range 4 .
31-0	Read Latency Range 4	Read	“0x00”	Lower 32-bits of Read Latency Range 4 .

10.

Read Latency Range 5 Register

The Read Latency Range 5 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 5.

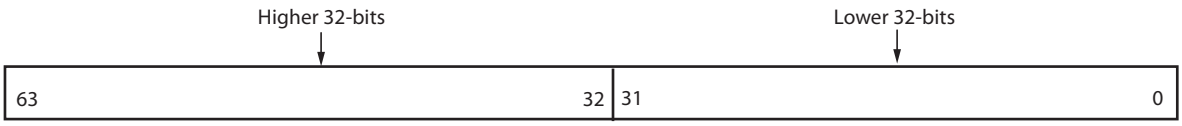

Figure 15: **Read Latency Range 5**

Table 22: **Read Latency Range 5 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 5	Read	“0x00”	Higher 32-bits of Read Latency Range 5 .
31-0	Read Latency Range 5	Read	“0x00”	Lower 32-bits of Read Latency Range 5 .

11.

Read Latency Range 6 Register

The Read Latency Range 6 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 6.

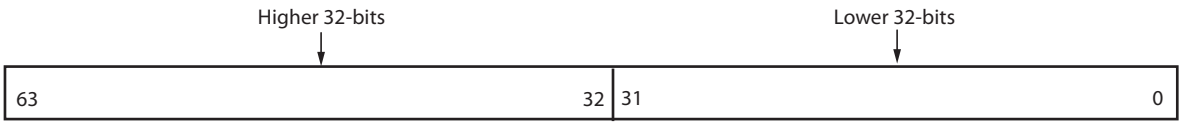

Figure 16: **Read Latency Range 6**

Table 23: **Read Latency Range 6 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 6	Read	“0x00”	Higher 32-bits of Read Latency Range 6 .
31-0	Read Latency Range 6	Read	“0x00”	Lower 32-bits of Read Latency Range 6 .

12.

Read Latency Range 7

The Read Latency Range 7 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 7. .

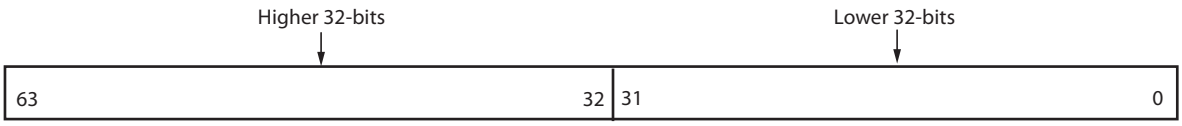

Figure 17: **Read Latency Range 7**

Table 24: **Read Latency Range 7 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range7	Read	“0x00”	Higher 32-bits of Read Latency Range7 .
31-0	Read Latency Range7	Read	“0x00”	Lower 32-bits of Read Latency Range 7 .

13.

Read Latency Range 8

The Read Latency Range 8 gives the information of the number of read transactions by/to a particular master/slave that falls in the read latency range 8. .

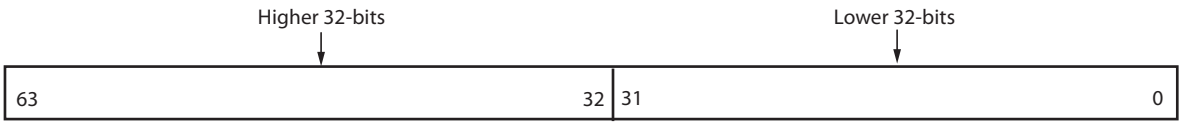

Figure 18: **Read Latency Range 8**

Table 25: **Read Latency Range 8 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 8	Read	“0x00”	Higher 32-bits of Read Latency Range 8 Register.
31-0	Read Latency Range 8	Read	“0x00”	Lower 32-bits of Read Latency Range 8 Register.

14.

Read Latency Range 9

The Read Latency Range 9 gives the information of the number of read transactions by/to a particular master/slave that falls above the read latency range 8. .

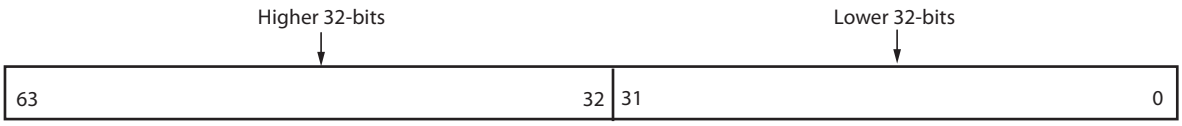

Figure 19: **Read Latency Range 9**

Table 26: **Read Latency Range 9 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Latency Range 9	Read	“0x00”	Higher 32-bits of Read Latency Range 9 .
31-0	Read Latency Range 9	Read	“0x00”	Lower 32-bits of Read Latency Range 9 .

15.

Write Latency Range 1 Register

The Write Latency Range 1 gives the information of the number of write transactions by/to a particular master/slave that falls in the write latency range 1. .

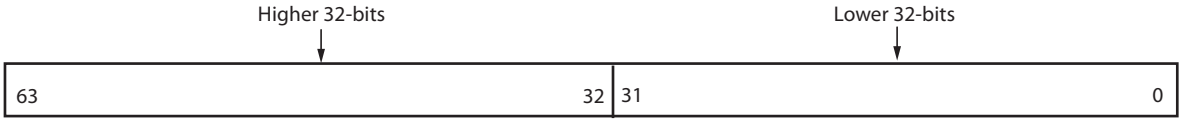

Figure 20: **Write Latency Range 1**

Table 27: **Write Latency Range 1 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Latency Range 1	Read	“0x00”	Higher 32-bits of Write Latency Range 1 .
31-0	Write Latency Range 1	Read	“0x00”	Lower 32-bits of Write Latency Range 1 .

16.

Write Latency Range 2

The Write Latency Range 2 gives the information of the number of write transactions by/to a particular master/slave that falls in the write latency range 2. .

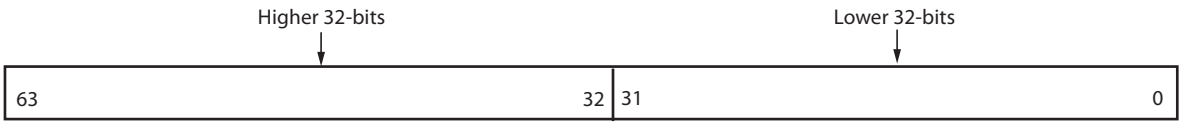

Figure 21: **Write Latency Range 2**

Table 28: **Write Latency Range 2 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Latency Range 2	Read	“0x00”	Higher 32-bits of Write Latency Range 2 .
31-0	Write Latency Range 2	Read	“0x00”	Lower 32-bits of Write Latency Range 2 .

17.

Write Latency Range 3

The Write Latency Range 3 gives the information of the number of write transactions by/to a particular master/slave that falls above the write latency range 2 interval. .

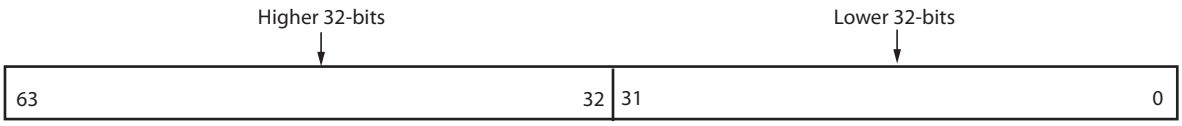

Figure 22: **Write Latency Range 3**

Table 29: **Write Latency Range 3 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Latency Range 3	Read	“0x00”	Higher 32-bits of Write Latency Range 3 .
31-0	Write Latency Range 3	Read	“0x00”	Lower 32-bits of Write Latency Range 3 .

18.

Write Latency Range 4

The Write Latency Range 4 gives the information of the number of write transactions by/to a particular master/slave that falls in the write latency range 4. .

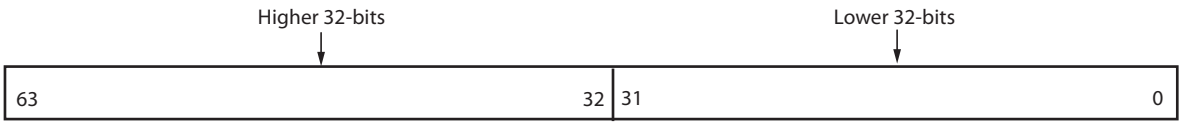

Figure 23: **Write Latency Range 4**

Table 30: **Write Latency Range 4 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Latency Range 4	Read	“0x00”	Higher 32-bits of Write Latency Range 4 .
31-0	Write Latency Range 4	Read	“0x00”	Lower 32-bits of Write Latency Range 4 .

19.

Write Latency Range 5

The Write Latency Range 5 gives the information of the number of write transactions by/to a particular master/slave that falls above the write latency range 4. .

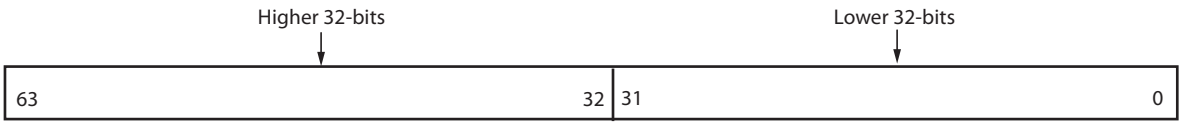

Figure 24: **Write Latency Range 5**

Table 31: **Write Latency Range 5 Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Latency Range 5	Read	“0x00”	Higher 32-bits of Write Latency Range 5 .
31-0	Write Latency Range 5	Read	“0x00”	Lower 32-bits of Write Latency Range 5 .

20.

Write Transaction Count Register

The Write Transaction Count gives the information of the number of write transactions by/to a particular master/slave.

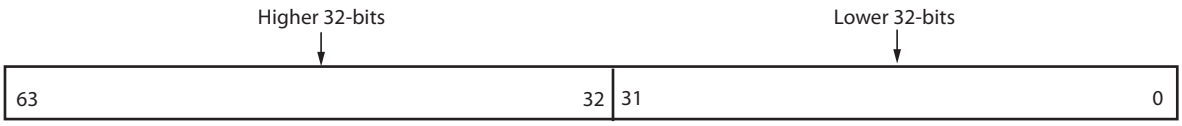

Figure 25: **Write Transaction Count**

Table 32: **Write Transaction Count Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Num_Wr_Reqs	Read	“0x00”	Higher 32-bits of Write Transaction Count
31-0	Num_Wr_Reqs	Read	“0x00”	Lower 32-bits of Write Transaction Count

21.

Read Transaction Count Register

The Read Transaction Count gives the information of the number of Read transactions by/to a particular master/slave. .

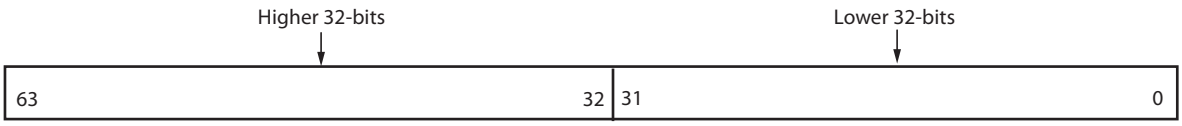

Figure 26: **Read Transaction Count**

Table 33: **Read Transaction Count Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Num_Rd_Reqs	Read	“0x00”	Higher 32-bits of Read Transaction Count
31-0	Num_Rd_Reqs	Read	“0x00”	Lower 32-bits of Read Transaction Count

22.

Write Byte Count

The Write Byte Count gives the information of the number of bytes that are written by/to a particular master/slave.

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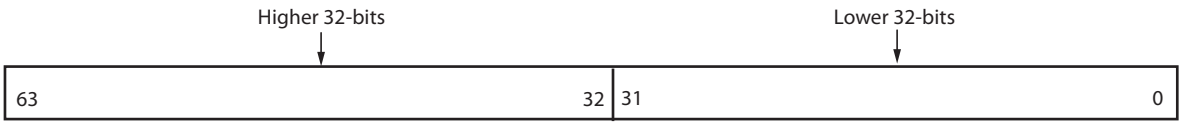

Figure 27: **Write Byte Count**

Table 34: **Write Byte Count Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Write Byte Count	Read	“0x00”	Higher 32-bits of Write Byte Count
31-0	Write Byte Count	Read	“0x00”	Lower 32-bits of Write Byte Count

23.

Read Byte Count

The Read Byte Count gives the information of the number of bytes that are read from/by a particular slave/master.

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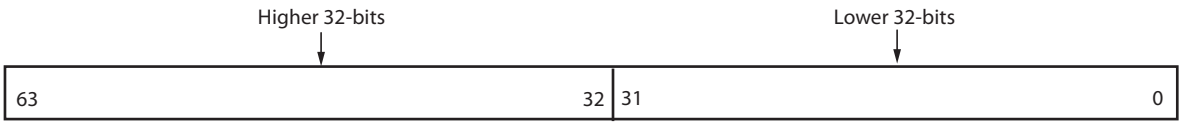

Figure 28: **Read Byte Count**

Table 35: **Read Byte Count Bit Definitions**

Bit	Name	Access	Reset value	Description
63-32	Read Byte Count	Read	“0x00”	Higher 32-bits of Read Byte Count
31-0	Read Byte Count	Read	“0x00”	Lower 32-bits of Read Byte Count

24.

Other Metrics computed

- **Total Read Latency** - This along with Num_Rd_Reqs is used in computing the Average Read Latency.
- **Total Write Latency** - This along with Num_Wr_Reqs is used in getting the Average Write Latency.
- **Slv_Wr_Idle_Cnt** - this gives the number of idle cycles caused by the slave during a Write transaction.
- **Mst_Rd_Idle_Cnt** - This gives the number of idle cycles caused by the master during a read transaction.
- **Num_BValids** - This gives the number of BValids given by a slave to the master. This count helps in checking the responses against the number of requests given.
- **Num_WLasts** - This gives the number of WLasts given by the master. This count should exactly match the number of requests given by the master. This helps in debugging of the system.
- **Num_RLasts** - This gives the number of RLasts given by the slave to the master. This count helps in checking the responses against requests. This count should exactly match the number of requests given by the master.
- **Num_Wr_Bursts_Len0** - This gives the count of the number of write requests given with a burst length of 1.
- **Num_Rd_Bursts_Len0** - This gives the count of the number of read requests given with a burst length of 1.

Procedure (Sequence of steps)

- Instantiate the performance monitor core in the EDK system.
- Configure the core based on the agents connected to the monitor slots to this core and their operating frequencies.
- CORE_CLK should be the fastest clock in the design (or of the interconnect).
- Program the configuration registers.
- Write to Metric_Selector_Registers based on the kind of metrics we are interested in and the targeted agent.
- Finally enable the metrics and global counter (control register).
- Give control to the actual application.
- Once the application is complete, disable the metrics and global counters by writing '0' to the control registers.
- Read the metrics registers and global clock counter register.
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-

Design Implementation

Target Technology

The intended target technology is the Virtex-6 and Spartan-6 family FPGAs.

Device Utilization and Performance Benchmarks

Core Performance

Because the AXI Performance Monitor is a module that will be used with other design pieces in the FPGA, the resource utilization and timing numbers reported in this section are estimates only. When the AXI Performance Monitor is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the design will vary from the results reported here.

The AXI Performance Monitor resource utilization benchmarks for a variety of parameter combinations measured with Virtex6 FPGA as the target device are shown in Table 37.

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The AXI Performance Monitor resource utilization benchmarks for a variety of parameter combinations measured with Spartan6 FPGA as the target device are shown in Table 37.

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Reference Documents

The following documents contain reference information important to understanding the AXI Ethernet Lite MAC design:

1. AXI4 AMBA AXI Protocol Version: 2.0 Specification

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx® ISE® Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK).

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Revision History

Date	Version	Description of Revisions
9/21/11	1.0	Initial Xilinx release

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