XAPP856 (v1.2) May 19, 2007

SFI-4.1 16-Channel SDR Interface with Bus Alignment

Author: Greg Burton

Summary

This application note describes an SFI-4.1 interface, a 16-channel, source-synchronous LVDS interface operating at single data rate (SDR). The transmitter (TX) requires 16 LVDS pairs for data and one LVDS pair for the forwarded clock. The transmitter operates at 4:1 serialization on each of the 16 data channels. The receiver (RX) also requires 16 LVDS pairs for data and one LVDS pair for the source-synchronous clock input. The receiver operates at 1:4 deserialization on each of the 16 data channels. The timing of the receiver is described in depth and characterized in hardware.

Introduction

The design described in the application note targets a Virtex™-5 FPGA, taking advantage of the ChipSync™ features available in every I/O of all Virtex-5 devices. These features include the ability to dynamically adjust the delay of the clock path in the receiver with 75 ps resolution.

Using this dynamic delay feature, the receiver in this application note escapes the limitations of static setup/hold timing by creating its own dynamic setup/hold timing. The interface calibrates out process variations by finding the optimal setup/hold timing for each individual device.

Figure 1 shows a Virtex-5 SFI-4.1 interface talking to an SFI-4 interface in another device that can be either an ASIC or an FPGA with support for a 16-channel SDR interface. Since this is a source-synchronous link, the receivers of both devices receive their clock from the TX side of the other device. The clock sources for the transmitters could come from a number of places in the backend systems, such as an oscillator on the PCB. Because each of the 16 data channels on the serial side of the interface runs at 4:1 serialization, the data width on the parallel side of the SDR interface is 64 bits.

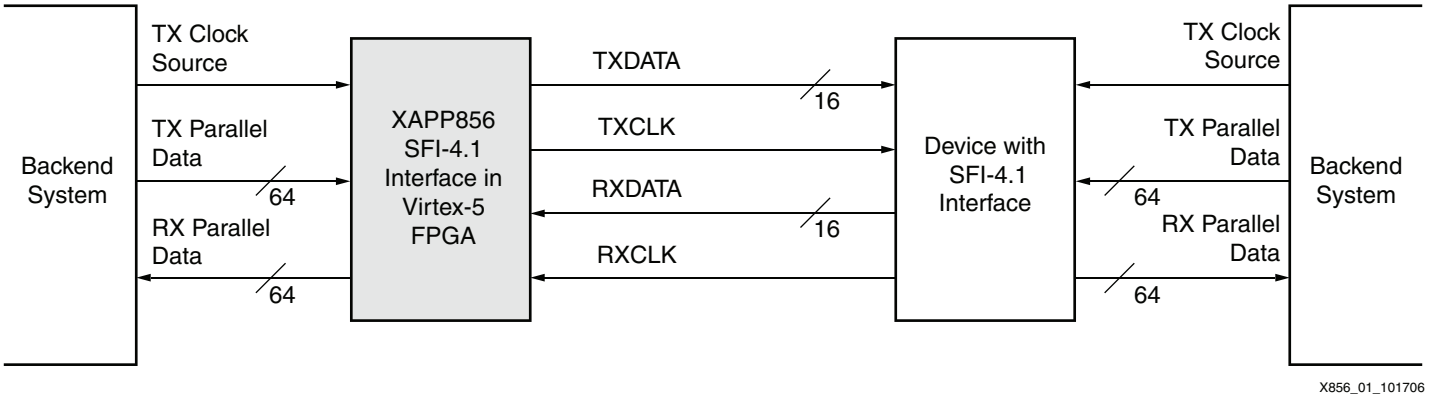


Figure 1: **Full-Duplex, 16-Channel SFI-4.1 Link between a Virtex-5 Device and Another Device with a 16-Channel SFI-4.1 Interface**

The stand-alone SFI-4.1 interface described in this application note does not include user constraints (no UCF). To evaluate the performance of this interface in hardware, a separate bit error rate tester (BERT) is also available for download (Figure 2).

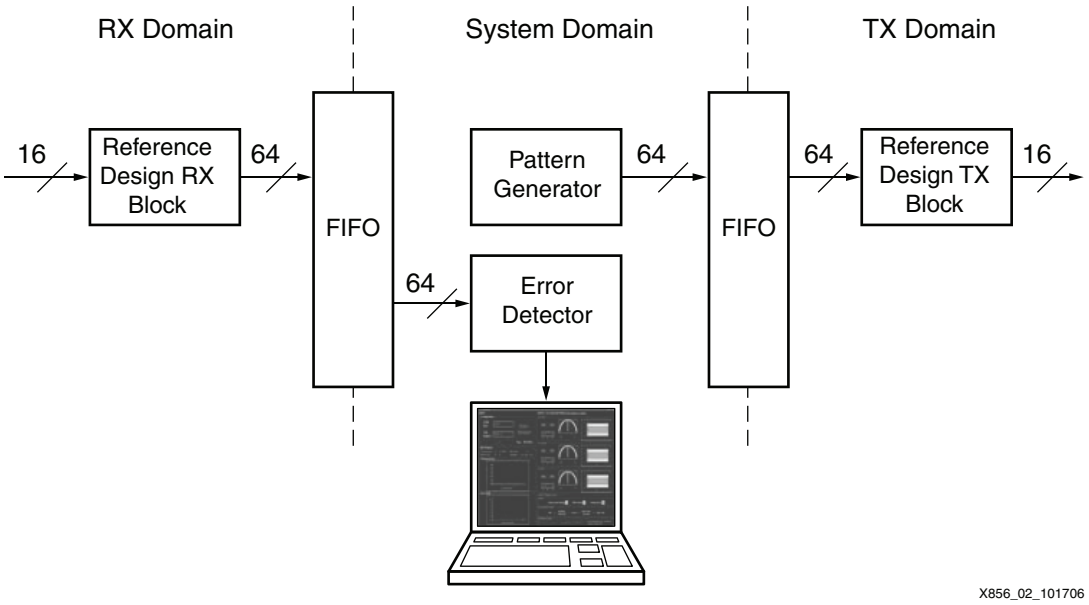


Figure 2: **BERT Testbench for Hardware Verification of the SFI-4.1 Interface**

The BERT is a revision-controlled testbench and includes the latest version of the SFI-4.1 interface. The Virtex-5 SFI-4.1 transmitter is looped back to the receiver in the same Virtex-5 device on an ML550 Networking Interfaces Board. The BERT communicates statistics about the interface performance to a graphical user interface on a PC. The BERT statistics are used extensively in the sections of this document concerned with hardware performance.

The design hierarchy of the interface itself is shown in Figure 3. The transmitter is very simple and contains almost no logic. The receiver contains logic that performs dynamic alignment on the clock channel.

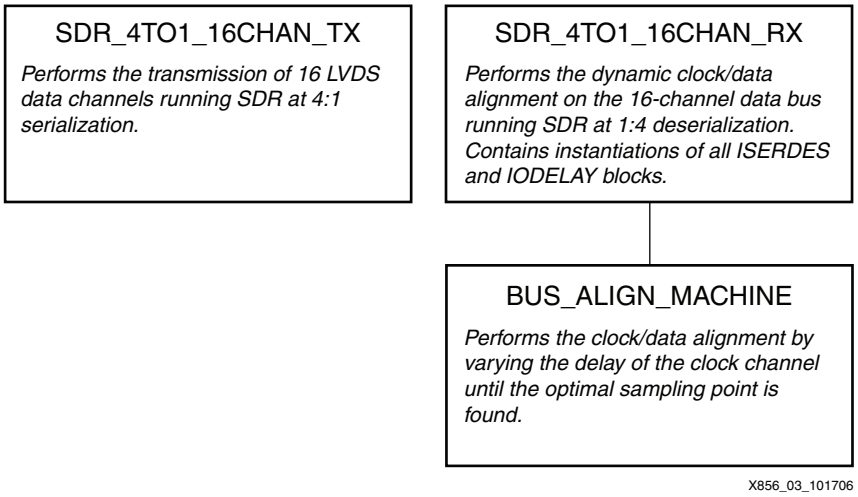


Figure 3: **Design Hierarchy of the Interface (TX and RX)**

SFI-4.1 Transmitter

The SDR transmitter consists of only one module: SDR_4TO1_16CHAN_TX. The module takes 64 bits of data on the parallel side, performs a 4:1 serialization, and transmits 16 channels of LVDS data on the serial side. The port list is shown in Table 1.

Table 1: **SDR_4TO1_16CHAN_TX Module Port Definitions**

Port Name	I/O	Definition
DATA_TX_P[15:0]	Output	16 data channels (P)
DATA_TX_N[15:0]	Output	16 data channels (N)
CLOCK_TX_P	Output	Forwarded clock (P)
CLOCK_TX_N	Output	Forwarded clock (N)
TXCLK	Input	TX clock source
TXCLKDIV	Input	TX clock source divided by 4
DATA_TO_OSERDES[63:0]	Input	Parallel side data from backend system
RESET	Input	Reset synchronous to the TX domain

No logic is used in the transmitter because all required functionality is contained within the OSERDES. The OSERDES is part of the ChipSync technology and is found in every I/O of all Virtex-5 devices. The OSERDES can be programmed to perform any serialization up to 10:1 and do single or double data rate transmission. Figure 4 shows a single channel of the SFI-4.1 TX.

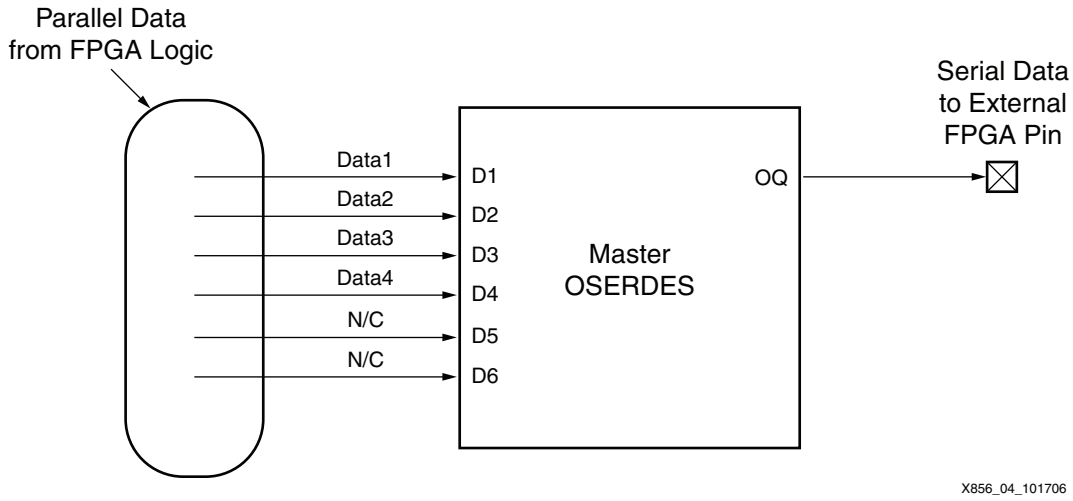


Figure 4: **OSERDES for a Single Data Channel with 4:1 Serialization**

The transmitter interface (Figure 5) consists of 16 OSERDES like the one shown in Figure 4. Because this interface is source synchronous, the clock must also be forwarded using the ODDR module.

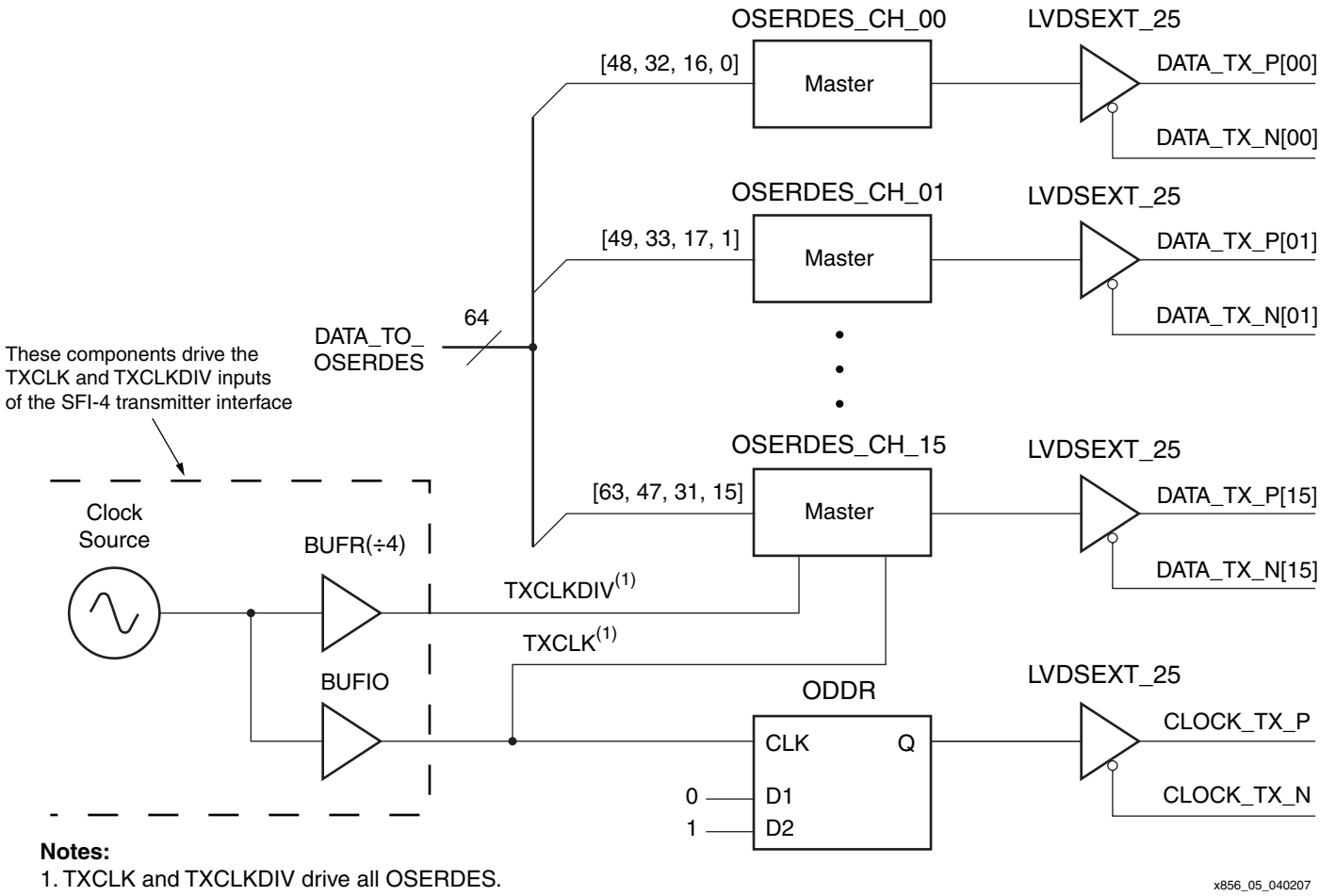


Figure 5: **Block Diagram of the TX Interface**

There is no training pattern allowed in the SFI-4.1 specification, so the transmitter begins transmitting user data immediately following reset. The receiver design must accommodate this limitation. The clock channel is transmitted 180° offset from the data channels. If it is desired that the clock be transmitted in phase with the data channels, the D1 and D2 inputs of the ODDR module in Figure 5 can be swapped.

Table 2 shows the device utilization statistics for the TX interface implemented in a Virtex-5 device. Since there is no logic in the transmitter, no look-up tables (LUTs) or slices are used. Table 2 shows one BUFIO and one BUFR being used. This design cannot be implemented using BUFGs and a DCM, because the required performance of SFI-4.1 exceeds the specifications of the DCM and global clock networks. The differences between the clocking schemes are discussed in "Interface Clocking."

Table 2: **SFI-4.1 TX Interface Utilization Statistics**

Component	Quantity	Usage Description
Slice Flip-Flop	0	Registered MUX output of DATA_TO_OSERDES
Slice	0	128/4 FFs per slice = 32 slices
LUT	0	–
IOB	34	17 LVDS output pairs (16 data, 1 clock)
OSERDES	16	One OSERDES for every LVDS data pair
BUFIO	1	TXCLK
BUFR	1	TXCLKDIV

Interface Clocking

In the block diagram of the SDR transmitter shown in Figure 5, the clock networks are shown driven by BUFIO and BUFR. When BUFIO and BUFR are used to generate the serial and parallel clocks, the phase relationship between the two clocks is guaranteed by design to meet the input requirements of the OSERDES (and ISERDES). Another valid way of driving the clock networks is to use global clocks combined with a DCM to divide by four. This scheme also provides phase-matched clock outputs, guaranteed by design to meet the input requirements of the OSERDES. The two clocking schemes are shown in Figure 6.

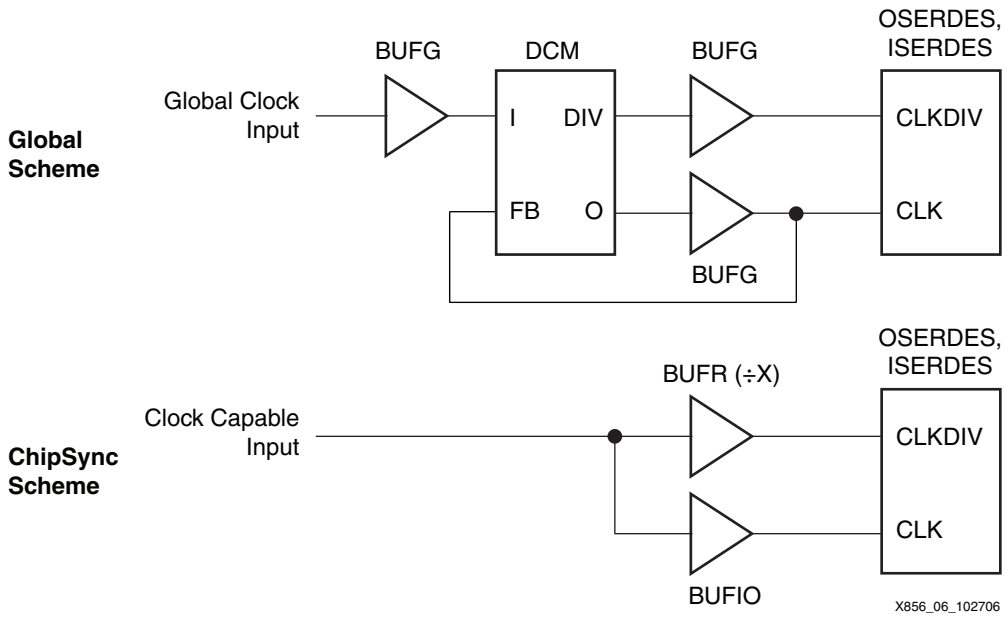


Figure 6: **Global and Regional Clocking Schemes in Virtex-5 FPGAs**

Which clocking scheme is the best to use? The BUFIO/BUFR networks maximize performance at the expense of some convenience. BUFIO and BUFR are regional clocks that cannot span the entire chip like a global clock. This difference means that transferring data between the regional and global domains must be a part of the designer's task and can simply mean adding a FIFO between the clock domains. BUFIO networks only span one clock region (equivalent to one bank).

Global clocks have lower performance than BUFIO, but are more convenient to use. If a clock is placed on a global network, it can reach any component in the entire device. To show the performance advantage of BUFIO, Table 3 shows snapshots of several timing parameters, some of which are included in the timing budget calculations for source synchronous interfaces.

Table 3: **Comparison of Global and I/O Clock Performance by Speed Grade**

	-3	-2	-1	Units
Maximum Frequency				
BUFG	550	500	450	MHz
BUFIO	710	710	644	MHz
Duty Cycle Distortion				
BUFG DYCD	150	150	150	ps
BUFIO DYCD	100	100	100	ps
Sampling Error				
BUFG T_{SAMP}	450	500	550	ps
BUFIO T_{SAMP}	350	400	450	ps

Table 3: **Comparison of Global and I/O Clock Performance by Speed Grade *(Continued)***

	-3	-2	-1	Units
Clock Tree Skew				
BUFG skew for XC5VLX50T	270	270	270	ps
BUFIO skew for all devices	50	50	50	ps

In each case, BUFIO has an advantage over BUFG, and collectively those advantages are significant. These parameters are used in the timing budget calculation section "Interface Timing Budget," page 15. For the most current specifications, consult the data sheet at www.xilinx.com.

Considering the maximum performance specification for BUFIO and BUFG, only BUFIO is capable of driving an SFI-4.1 design that is required to reach clock speeds between 600 and 700 MHz. Even in the highest speed grade, BUFG falls short of that requirement. Because both the transmitter and receiver of this design are required to be implemented using BUFIO clock networks, all I/Os in the transmitter must be constrained to a single bank, and all I/Os in the receiver must be constrained to a single bank.

The interface does not include the FIFO logic necessary to transfer the parallel data to/from the backend system domain. However, the BERT design discussed in "Introduction," page 1 (see Figure 2, page 2) shows how to transfer data to/from the RX and TX clock domains by using FIFO18_36 primitives. A FIFO36_72 primitive can also be used.

SFI-4.1 Receiver

The SFI-4.1 receiver consists of two core modules: SDR_4TO1_16CHAN_RX and BUS_ALIGN_MACHINE. The receiver is more complex than the transmitter because it includes a dynamic alignment algorithm implemented in the FPGA fabric. The SDR_4TO1_16CHAN_RX module takes 16 channels of data on the serial side, optimizes the timing relationship of the data bus with the clock, performs 1:4 deserialization, and presents 64 bits of data on the parallel side. The port list is shown in Table 4.

Table 4: **SDR_4TO1_16CHAN_RX Module Port Definitions**

Port Name	I/O	Definition
DATA_RX_P[15:0]	Input	16 data channels (P).
DATA_RX_N[15:0]	Input	16 data channels (N).
CLOCK_RX_P	Input	Forwarded clock (P).
CLOCK_RX_N	Input	Forwarded clock (N).
INC_PAD	Input	Pulsing this pin causes the IDELAY tap setting of the clock channel to increment by 1.
DEC_PAD	Input	Pulsing this pin causes the IDELAY tap setting of the clock channel to decrement by 1.
DATA_FROM_ISERDES[63:0]	Output	Parallel side data to backend system.
RESET	Input	Reset synchronous to the RX domain.
IDLY_RESET	Input	Reset synchronous to the RX domain that only resets the IDELAY tap settings of the clock channel.
IDELAYCTRL_RESET	Input	Reset synchronous to the TX domain that only resets the IDELAYCTRL module.
CLK200	Input	Reference clock to IDELAYCTRL module.

Table 4: **SDR_4TO1_16CHAN_RX Module Port Definitions *(Continued)***

Port Name	I/O	Definition
TAP_00, TAP_01, TAP_03, TAP_04, TAP_05, TAP_06, TAP_07, TAP_08, TAP_09, TAP_10, TAP_11, TAP_12, TAP_13, TAP_14, TAP_15	Output[5:0]	Each of these 6-bit signals contains the current IDELAY tap value of the 16 data channels. Equal to zero for all data channels because the clock channel is the only dynamically delayed path.
TAP_CLK[5:0]	Output	The 6-bit signal containing the current IDELAY tap value of the clock channel.
TRAINING_DONE	Output	Flag indicating alignment is complete.
RXCLK	Output	RX Source Sync Clock.
RXCLKDIV	Output	RX Source Sync Clock divided by 4.
IDELAY_READY	Output	Flag indicating IDELAYCTRL is calibrated.

Most of the logic used in the receiver is contained within the ISERDES. The ISERDES, which is part of the ChipSync technology, is found in I/Os of all Virtex-5 devices. The ISERDES can be programmed to do any deserialization up to 1:10 and do single or double data rate reception. Figure 7 shows a single channel of the RX.

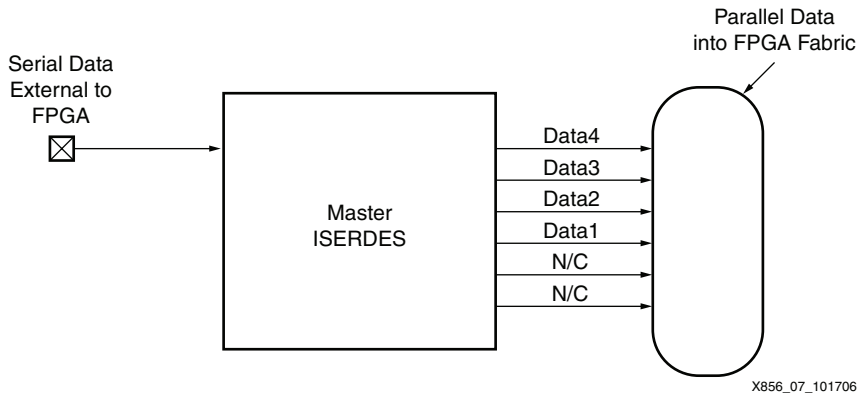
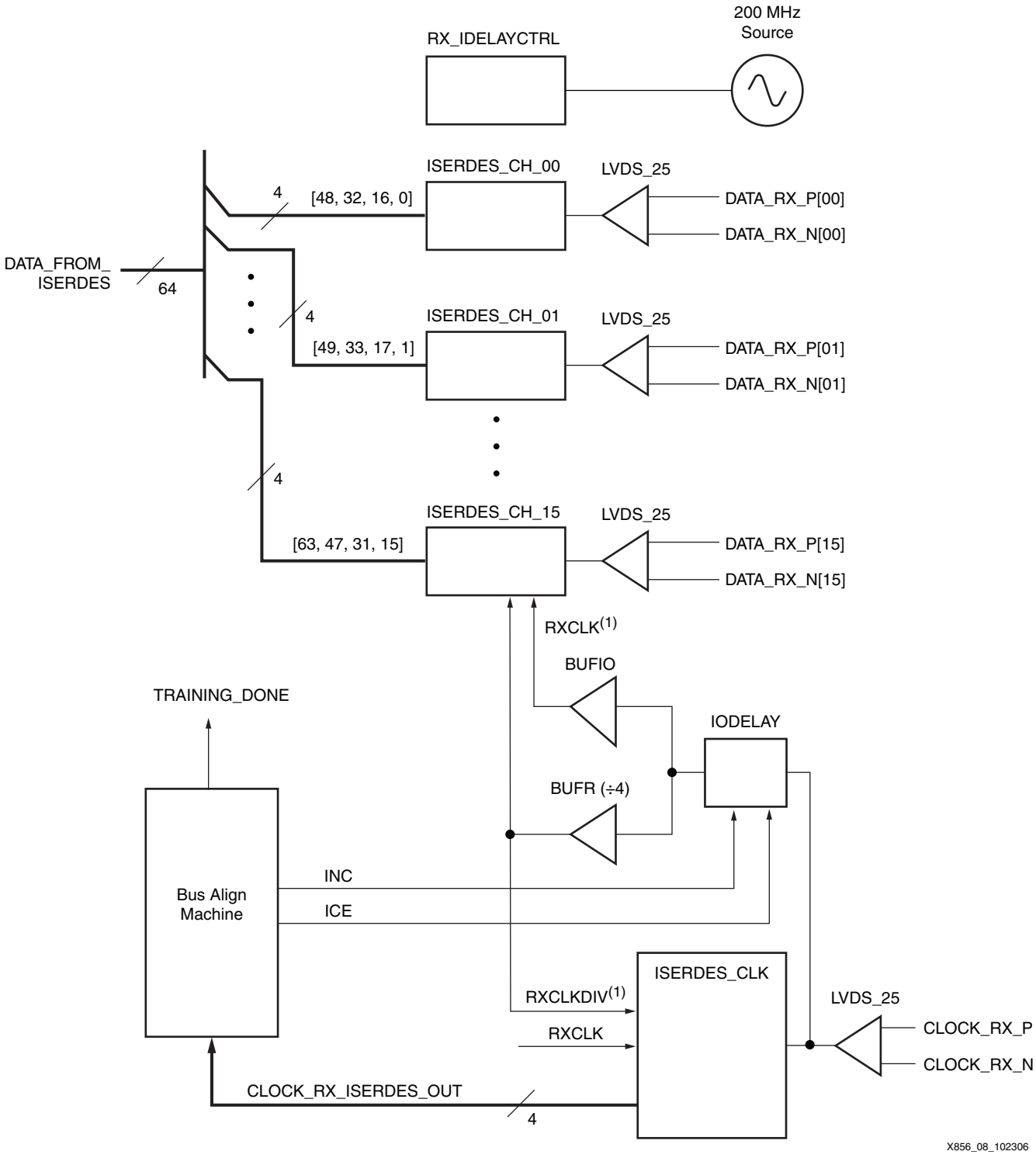


Figure 7: **ISERDES for a Single Data Channel with 1:4 Deserialization**

The receiver interface (Figure 8) consists of 16 ISERDES pairs. Because this interface is source synchronous, the clock source comes from the transmitter. The clock is buffered in the receiver by a BUFIO component and divided to the parallel clock rate by a BUFR component.



Notes:

1. RXCLK and RXCLKDIV go to all ISERDES.

Figure 8: **RX Interface Block Diagram**

Each ISERDES in Figure 8 contributes 4 bits to the 64-bit parallel data bus. The data outputs of each ISERDES are not contiguous within the 64 bit bus, because the 64-bit parallel data bus is divided into four 16-bit words that are striped across the 16 SERDES channels. Each ISERDES has a single bit from each of the four 16-bit words (for example, Channel 0 has bits 0, 16, 32, and 48). By striping 16-bit words across the 16 channels, the continuity of those words are

guaranteed by design without the need for bit rotation of the parallel data outputs. This is required in an SFI-4 design because there is no training pattern allowed at initialization. Without a training pattern, the BITSLIP feature of the ISERDES is not an option. Word alignment must be guaranteed by design. Both the OSERDES and ISERDES are designed to maintain synchronization across channels, such that words striped across multiple ISERDES are continuous.

Because there is no training pattern, the clock channel must play a key role in the initial training process. The data channels continuously stream user data that an algorithm cannot reliably use to perform dynamic alignment, as is done in XAPP855 and XAPP860. The clock channel, however, does contain known content. By treating the clock channel as just another data channel and deserializing it at a ratio of 1:4, the information in the oversampled clock bits can be used to perform dynamic alignment. This is why the forwarded clock in Figure 8 takes two separate paths: one to the BUFIO and BUFR clock networks and one to an ISERDES. This procedure is discussed in detail in "Dynamic Timing and BUS_ALIGN_MACHINE," page 13.

The IDELAYCTRL module in Figure 8 is shown as having no connection to the rest of the receiver. Actually, IDELAYCTRL is required to calibrate the IODELAY blocks in the path of each data channel. A single IDELAYCTRL block is sufficient to calibrate all 16 data channels, since all channels are in the same bank.

The BUS_ALIGN_MACHINE generates two control signals that adjust the timing of the clock channel. INC and ICE cause the IODELAY to increment or decrement the delay in the clock path by a fixed amount of ~75 ps (if a 200 MHz reference clock is used).

Table 5 shows the device utilization statistics for the RX interface implemented in a Virtex-5 device. These figures exclude the counter used to track the IODELAY settings on the clock channel; in most instances, the counter can be removed after the interface is integrated and verified in a specific environment. The majority of the LUTs utilized are consumed by the BUS_ALIGN_MACHINE, which is the core of the receiver alignment algorithm. As in the TX interface, the RX interface consumes one BUFIO and one BUFR for clocking.

Table 5: **DDR RX Interface Utilization Statistics**

Component	Quantity	Usage Description
Slice Flip-Flop	30	Multiple uses
Slice	25	Multiple uses
LUT	58	Multiple uses
IOB	34	17 LVDS input pairs (16 data, 1 clock)
ISERDES	17	One ISERDES for every LVDS data pair and clock
BUFIO	1	RXCLK
BUFR	1	RXCLKDIV

Receiver Interface Dynamic Timing

The timing of the receiver interface is broken into two parts:

- The suboptimal timing inherent in the data and clock paths
- The optimal timing created by the receiver when adjusting dynamic delays on the clock channels at initialization.

Inherent Timing

An inventory of all propagation delays in the clock and datapaths must be taken to derive the inherent setup/hold times. The clock and datapaths for a single channel of this interface are shown in Figure 9. The ISE Timing Analyzer breaks down the paths into the timing parameters shown. The clock and data channels ideally are perfectly phase-aligned at the input pins (there

is, of course, skew that is considered in "Interface Timing Budget," page 15). All components in the path have both a minimum and maximum value to account for process variations. Referring back to Figure 8, the clock channel followed two paths: one through the IODELAY and one through the ISERDES. The path through the ISERDES is not represented explicitly in Figure 9 because it is identical to the datapath.

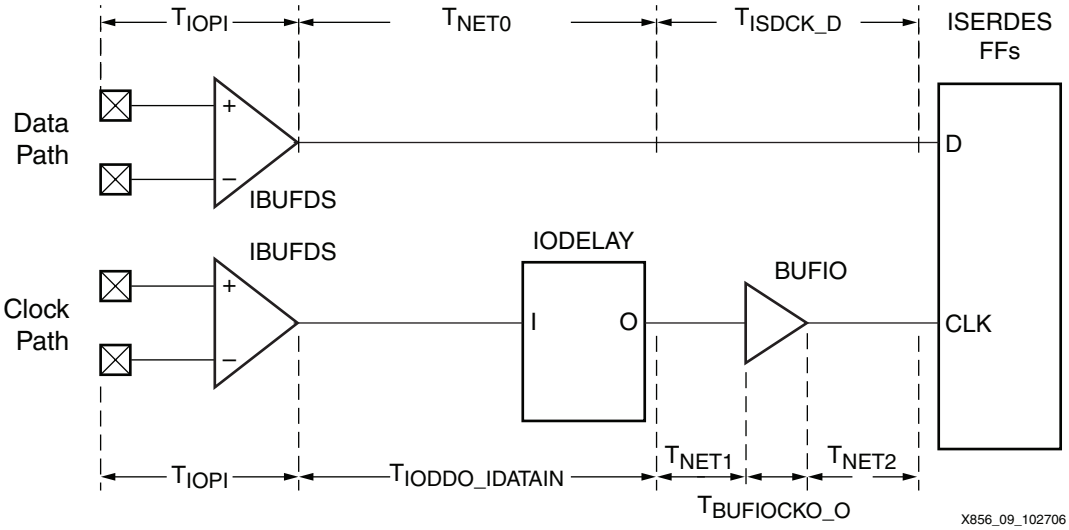


Figure 9: **Timing Components of RX Data and Clock Paths**

Figure 10 shows the timing analyzer settings used to generate the information in this report. Each of the timing parameters is described in Table 6 and Table 7. The minimum and maximum values of the individual timing parameters for the clock and datapaths are shown in Table 8 and Table 9.

Note: All raw timing numbers referenced in this document are subject to minor changes in subsequent revisions of the ISE tools.

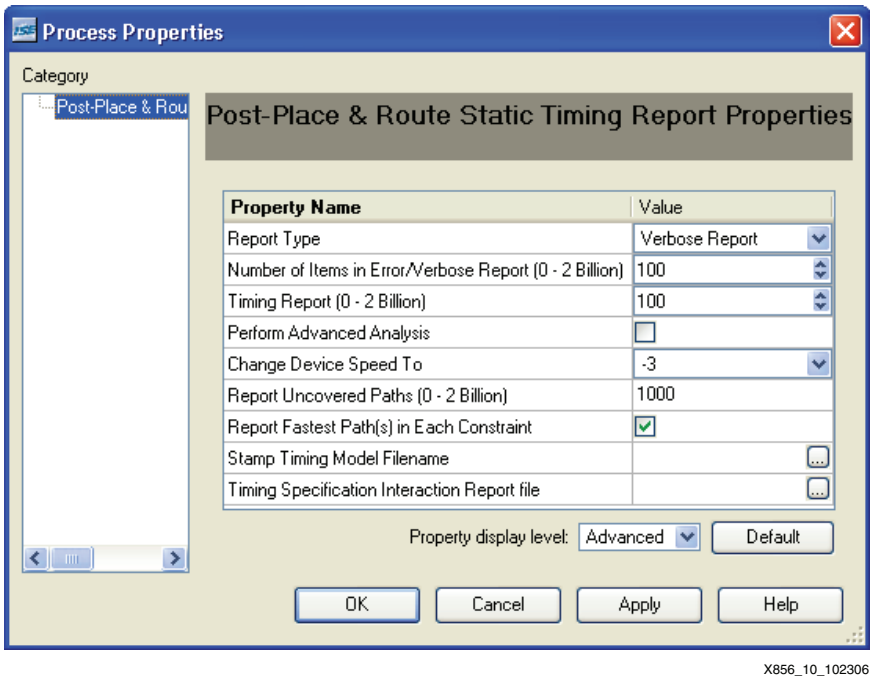


Figure 10: **ISE Timing Analyzer Properties Used in this Document**

Table 6: **Datapath Timing Definitions**

Timing Parameter	Description
T_{IOPI}	Delay from the IOB pad through the LVDS input buffer to the I pin of the IOB pad
T_{NET0}	Delay from the I pin of IOB pad to the D input of the ISERDES
T_{ISDCK_D}	Delay from the D input of the ISERDES to the sampling registers in the ISERDES (setup and hold times of ISERDES)

Table 7: **Clock Path Timing Definitions**

Timing Parameter	Description
T_{IOPI}	Delay from the IOB pad through the LVDS input buffer to the I pin of the IOB pad
$T_{IODDO\_IDATAIN}$	Delay from I pin of IOB pad to the O output of the IODELAY block
T_{NET1}	Delay from the O output of the IODELAY block to the I pin of BUFIO
$T_{BUFIOCKO\_O}$	Clock to out delay of BUFIO
T_{NET2}	Clock distribution delay from BUFIO output to the clock input of data ISERDES

Table 8: **Datapath Delay Inventory for a -1 Speed Grade XC5VLX50T Device**

Timing Parameter	Maximum Datapath Delay	Minimum Datapath Delay
T_{IOPI}	1.076 ns	0.756 ns
T_{NET0}	0.0 ns	0.0 ns
T_{ISDCK_D}	0.027 ns	–0.075 ns
TOTAL	1.103 ns	0.681 ns

Table 9: **Clock Path Delay Inventory for a -1 Speed Grade XC5VLX50T Device**

Timing Parameter	Maximum Clock Path Delay	Minimum Clock Path Delay
T_{IOPI}	1.150 ns	0.820 ns
$T_{IODDO\_IDATAIN}$	0.671 ns	0.671 ns
T_{NET1}	0.254 ns	0.190 ns
$T_{BUFIOCKO\_O}$	1.130 ns	0.894 ns
T_{NET2}	0.404 ns	0.319 ns
TOTAL	3.609 ns	2.894 ns

According to the inherent timing prediction, the data is going to arrive before the clock by an amount determined by Equation 1 and Equation 2. Equation 1 calculates that data arrives before the clock by at least 1.791 ns in a -1 device. Equation 2 calculates that data arrives before the clock by at most 2.928 ns. Equation 3 shows a timing window that covers all -1 devices under all conditions. This timing window describes the inherent timing of the data and clock paths. Assuming skew-matched PCB traces for all sixteen data channels and the clock channel, then it can be assumed that all 16 channels in the receiver have roughly the same timing window.

$$\text{Setup Time} = \text{Max Data Delay} - \text{Min Clock Delay} = 1.103 - 2.894 = -1.791 \text{ ns} \quad \textit{Equation 1}$$

$$\text{Hold Time} = \text{Max Clock Delay} - \text{Min Data Delay} = 3.609 - 0.681 = 2.928 \text{ ns} \quad \textit{Equation 2}$$

$$\text{Timing Window} = 2.928 - 1.791 = 1.137 \text{ ns} \quad \textit{Equation 3}$$

Figure 11 shows the timing windows for all speed grades of an XC5VLX50T device as well as the locations of hardware measurements of inherent timing relationships (to validate the calculations). The hardware measurements show the SDR interface data arriving before the clock within the ranges of the respective speed grades. Table 10 provides the specifics for each hardware measurement (device serial number, speed grade, and clock arrival time).

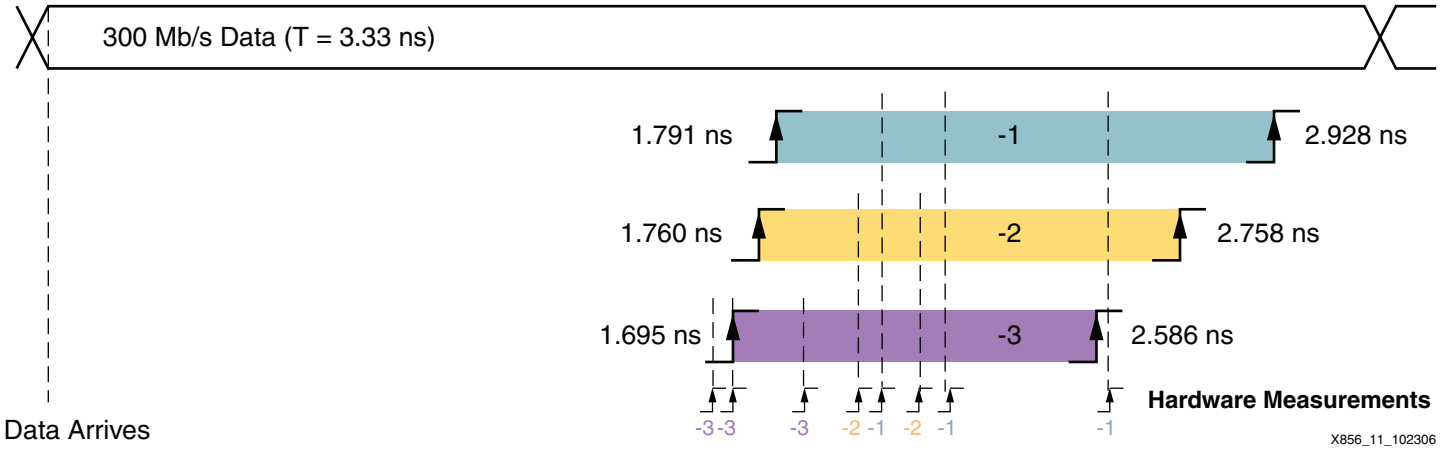


Figure 11: **Timing Windows Show Uncertainty in Clock/Data Relationship as Calculated by Timing Analyzer**

Table 10: **Hardware Measurements for XC5VLX50T Devices (All Speed Grades)**

S/N	Speed Grade	Clock Arrival After Data (ns)
2199	-1	2.069
2194	-1	2.221
2219	-1	2.596
001	-2	1.994
002	-2	2.146
003	-2	2.146
004	-3	1.619
005	-3	1.844
006	-3	1.694

Dynamic Timing and BUS_ALIGN_MACHINE

In "Inherent Timing," page 9, the inherent timing of the interface was calculated for all speed grades and validated with a hardware measurement. In that case, the inherent timing was sufficient because the data rate is only 300 Mb/s (Figure 11). What happens when the data rate is increased such that the hold edge of the data window begins to shrink (Figure 12)?

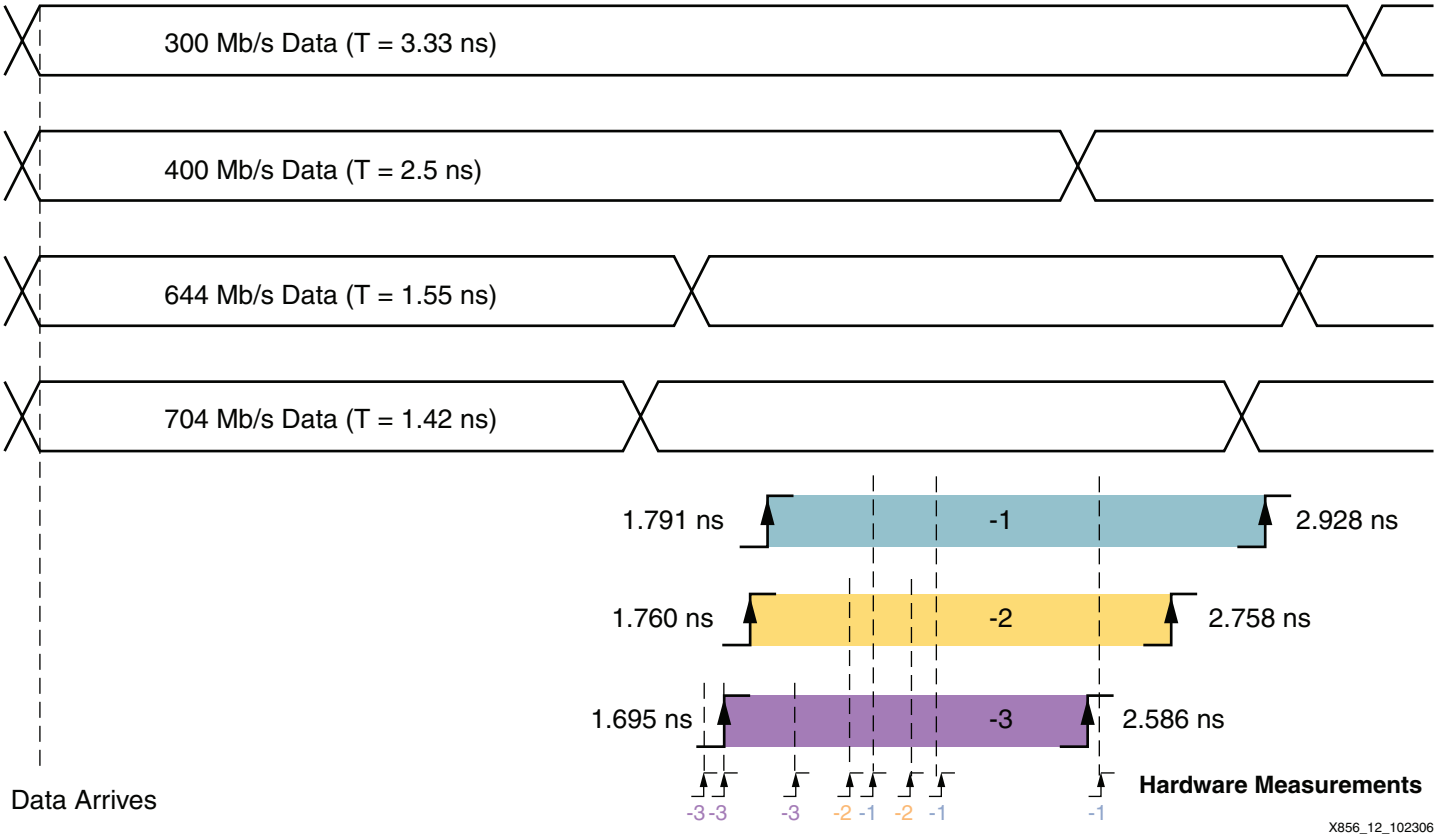


Figure 12: **Inherent Timing Windows Shown in Relation to Multiple Data Rates**

At 400 Mb/s, the inherent timing relationship is no longer adequate to meet timing because there are cases when the sampling clock edge is in the middle of the data transition. The solution to the suboptimal, inherent timing is dynamic timing. The BUS_ALIGN_MACHINE module in the receiver positions the sampling edge of the clock at the center of the data eye by adding delay to the clock path.

The principle of bus alignment is to treat the entire data bus as a single entity and adjust the clock channel to the most optimal sampling position for the bus. No delay adjustments are made to individual data channels to compensate for skew, such that any skew between data channels directly counts against the interface timing budget.

The difficulty in this implementation is finding the center of the data eye without a training pattern at initialization. To do so, the following assumption is made: in an SFI-4.1 interface where the clock and data bus are skew-matched as closely as possible, the center of the data eye coincides with the rising edge of the clock (assuming 50% duty cycle distortion on the clock). Under this assumption, the clock can be treated as a pseudo data channel and can be *deserialized* by sampling itself. The sampled clock bits can be monitored while increasing the clock delay until the rising edge is found, indicating that the clock is sampling at the center of the data bus eye.

The steps of the bus-alignment procedure are shown in Figure 13. The algorithm's task is simple. Add delay to the clock channel until a rising edge is observed. Given the initial timing shown in Figure 13, the clock must first pass a falling edge before it detects the rising edge. The

initial timing could also be such that the rising edge is found first. If all possible initial timing relationships are considered, the maximum delay that could be needed on the clock channel is one period of the clock, and the minimum delay that could be needed is 75 ps, or 1 IDELAY tap.

There are several advantages to applying delay to the clock channel rather than the data channels. First, the need for a training pattern is eliminated. Second, interrogating the clock channel is easier than interrogating a data channel because there is no jitter for the algorithm to anticipate. Finally, a clock pattern does not suffer any degradation passing through the IDELAY chain, whereas a data pattern collects a finite amount of pattern jitter in each IDELAY tap.

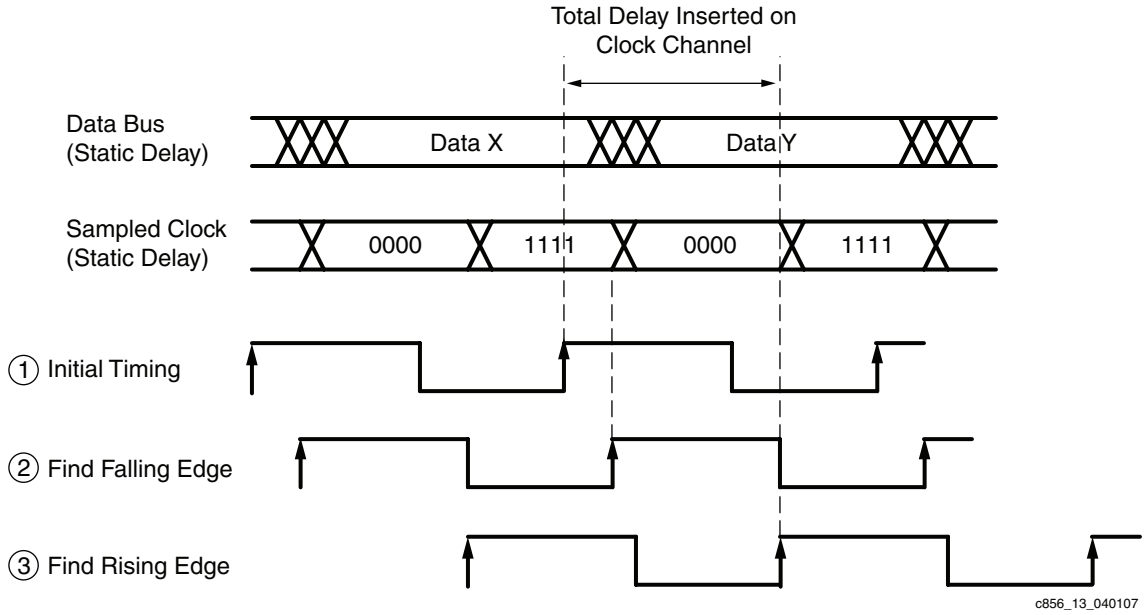


Figure 13: **Dynamic Bus Alignment Procedure in the BUS_ALIGN_MACHINE Module**

The FSM in the BUS_ALIGN_MACHINE module used to implement bus alignment is shown in Figure 14. The FSM treats three possible scenarios, loosely described as:

- when the first clock sample is a 1
- when the first clock sample is a 0
- when the first clock sample is unstable

All scenarios end by finding the rising edge of the clock, which is the center of the data eye.

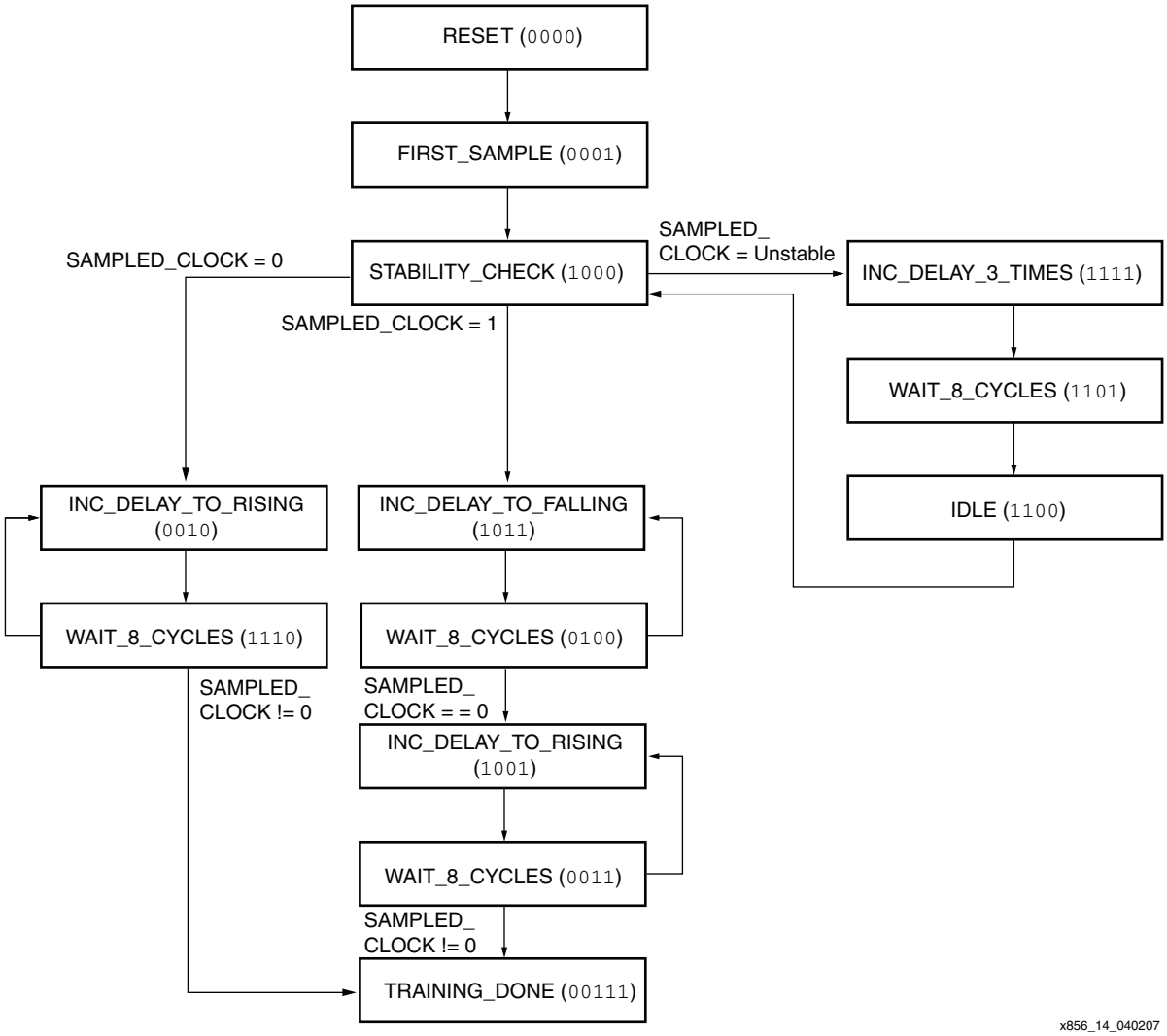


Figure 14: **Dynamic Bus Alignment Procedure in the BUS_ALIGN_MACHINE Module**

Interface Timing Budget

In addition to sampling the data as closely as possible to the center of the data eye, the actual size of the data eye is important. By accurately predicting the size of the data eye in the receiver, the overall performance ceiling of the interface can be inferred. The ideal data eye width is the period of the data rate (for example, T_{Bit_Period} = 1.43 ns for 700 Mb/s). Both the transmitter and receiver circuits have sources of error that subtract from the ideal data eye. The equation for the eye width at the output of the transmitter is shown in Equation 4.

$$DATA\_EYE\_WIDTH\_TX = T_{PERIOD} - T_{JITTER} - T_{BUFIOSKEW} - T_{PKGSKEW} \quad \textit{Equation 4}$$

T_{JITTER} is the peak-to-peak jitter of the clock source driving the transmitter data bus and forwarded clock. Skew must be subtracted from the timing budget because the dynamic alignment algorithm aligns the clock to the *entire* data bus, not each individual channel. In the transmitter, skew on the clock network that drives the data bus and forwarded clock ($T_{BUFIOSKEW}$) and skew in the device package ($T_{PKGSKEW}$) count against the transmitter timing budget. Duty cycle distortion of the clock network does not cause data eye closure and need not be included as a source of error.

Equation 5 calculates the width of the data eye at the receiver flip-flops. Ideally, the eye width at the receiver is the same as the eye width at the output of the transmitter, but there are sources of error in the transmission medium and receiver circuitry. T_{SAMP_BUFIO} is the receiver sampling

error due to drift caused by voltage and temperature variations. The receiver implementation eliminates the need to consider pattern jitter in the IDELAY chain because IDELAY is only used on the clock channel. For a clock pattern, $T_{IDELAYPAT\_JIT}$ is 0 ps/tap peak to peak. For a data pattern with long and short run lengths of zeroes and ones (simulated by PRBS23), $T_{IDELAYPAT\_JIT}$ is a finite value that must be considered in the timing budget. Skew must be counted again in the receiver.

$$DATA\_EYE\_WIDTH\_RX = DATA\_EYE\_WIDTH\_TX - T_{BOARD\_JITTER} - T_{PCBTRACE\_SKEW} - T_{BUFIOSKEW} - T_{PKGSKEW} - T_{SAMP\_BUFIO} - T_{QUANTIZATION\_ERR} \quad \text{Equation 5}$$

T_{BOARD_JITTER} includes jitter induced by receiver input capacitance and the parasitics of the physical data path on the PCB. T_{BOARD_JITTER} must be determined by simulation, as it varies as a function of frequency and for receivers of different types and vendors. On the ML550, with a -2 speed-grade Virtex-5 device, the T_{BOARD_JITTER} is measured at roughly 200 ps at 700 Mb/s (assuming data content equivalent to PRBS23). $T_{QUANTIZATION\_ERR}$, or quantization error, is caused by the granularity of the IDELAY tap chain. Working with 75 ps increments, it is not possible to utilize the entire data eye, because inevitably some valid eye width is lost between two taps. The value for this loss is 75 ps. As long as the receiver eye width calculated using Equation 5 is greater than or equal to 0, the interface operates correctly over process, voltage, and temperature.

For example, Equation 6 and Equation 7 show the timing budget calculation for the SFI-4.1 interface running at 700 Mb/s in a -1 speed grade device on an ML550 evaluation board. Refer to the data sheet for the most current values. The TX interface is looped back to the RX interface on the same Virtex-5 FPGA, as shown in Figure 2, page 2.

$$DATA\_EYE\_WIDTH\_TX = 1430\ ps - 25\ ps - 50\ ps - 150\ ps = 1205\ ps \quad \text{Equation 6}$$

$$DATA\_EYE\_WIDTH\_RX = 1205\ ps - 200\ ps - 25\ ps - 50\ ps - 150\ ps - 450\ ps - 75\ ps = 255\ ps \quad \text{Equation 7}$$

Changes in voltage and temperature cause the data channels of the interface to drift relative to the clock. If the SFI-4.1 interface were to transfer user data for a long period of time over all specified conditions of temperature and voltage, Equation 7 states that there would be at least 255 ps (three or four IDELAY taps) of data window remaining valid during all fluctuations of temperature and voltage. Compare this calculation to the measurements in the 700 Mb/s case in Table 11, page 18. There are nine taps that are error free under all conditions. In "Appendix," page 21, there are three -1 devices tested at 700 Mb/s, and each has 6, 9, and 9 taps, respectively, that are error free under all conditions.

At a given temperature and voltage setting, the data valid window is much larger because there is no drift when temperature and voltage are constant. The size of the data valid window under constant conditions is 255 ps + T_{SAMP_BUFIO}, which in this case is at least 705 ps (nine or ten IDELAY taps). Compare this calculation to the measurements of any single condition for the 700 Mb/s case in Table 11, page 18. In the worst case (–5% supply), there are 14 taps that are error free.

The skew specifications used in these calculations represent the worst possible skew for any set of I/Os in a single bank used to implement an interface. When a designer reaches the implementation phase of the SFI-4.1 Interface design and selects I/O location constraints, Timing Analyzer can be used to determine the exact skew of the interface. The actual skew is smaller or equal to the worst-case specification calculated in Equation 6 and Equation 7.

Interface Characterization

By following the procedure illustrated in Figure 13, page 14, the bus-alignment algorithm should never insert more than approximately one bit time of delay on the clock channel. The most IDELAY taps are inserted when the clock initially samples just after the center of the data eye, as in the 300 Mb/s case in Figure 12, page 13. The algorithm must move all the way through the rest of the first eye to find the first transition (0.5 bit time) and then move halfway into the next eye to center the sampling point (0.5 bit time). This process produces a maximum total delay insertion of 1.0 bit times, which is clear in Figure 15.

The actual performance of the bus-alignment algorithm is characterized as a function of data rate in Figure 15. For all data rates, the expectation is that the tap setting of the clock channel in the SFI-4.1 receiver does not exceed approximately 1.0 bit times of delay. This graph only shows the data for a single device. Comparing the 1.5 bit time mask to the actual settings, it is clear that the algorithm remains within the 1.0 bit time limit.

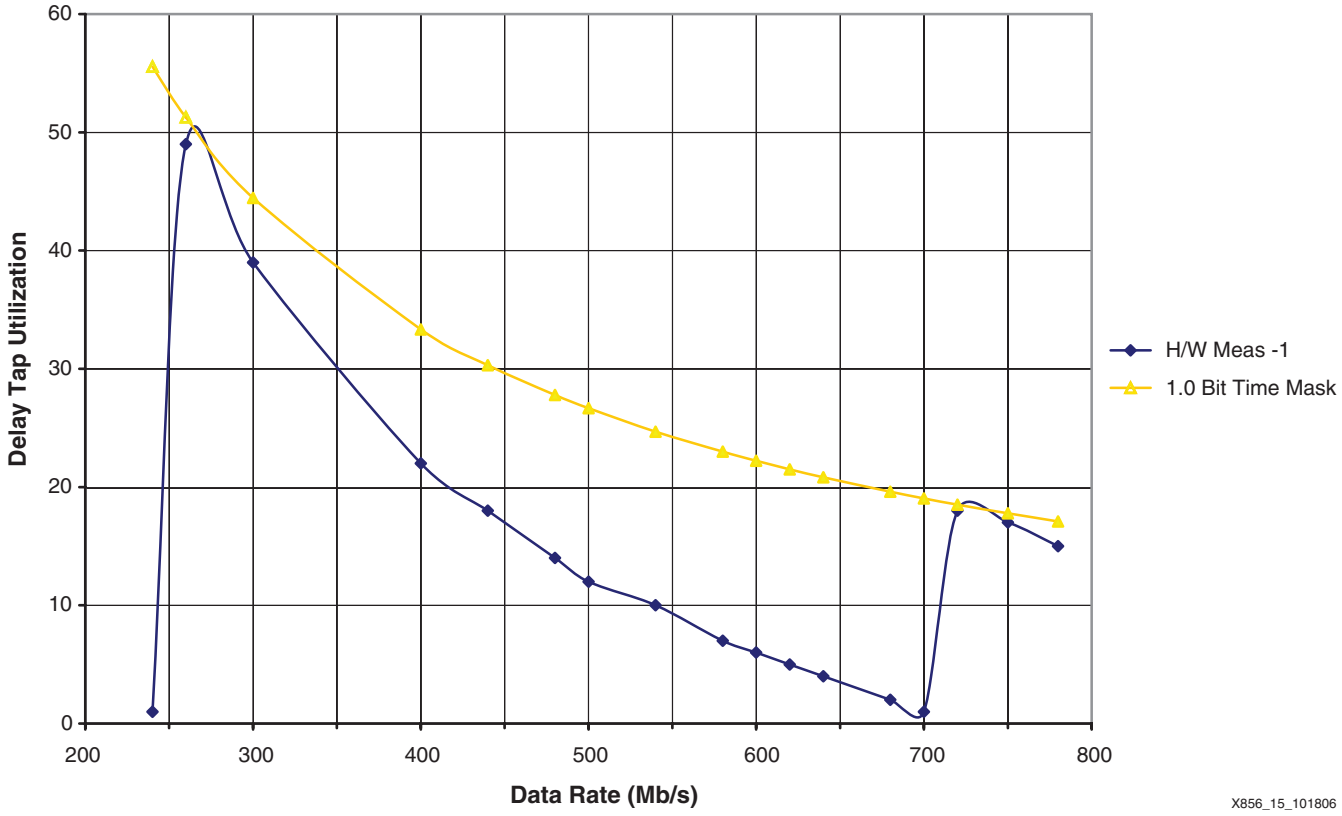


Figure 15: **Measured IODELAY Tap Settings on Clock Channel vs. Data Rate**

The tap settings in Figure 15 generally decrease linearly with shrinking bit periods, except in the case of 260 Mb/s and 720 Mb/s data rates. These data rates are "seams" in the inherent timing of this particular device. On one side of the seam, the tap setting is the minimal value of one, and on the other side of the seam, the tap setting is the maximum value of taps (totalling one bit period). The reason for this non-linear change in tap setting is the inherent timing that the bus-alignment algorithm starts with. At 240 Mb/s, the clock is sampling just slightly before the center of the data eye (indicated by the falling edge of the clock), such that the algorithm does not need to insert more than a single tap of delay to get to the center of the data eye. At 260 Mb/s, the slightly shorter bit period has moved the initial sampling point of the clock just past the center of the data eye, such that the bus-alignment algorithm must move through one full bit period to find the next data eye (and the falling edge of the clock).

These *seams* could represent a word alignment problem because from one reset to another the algorithm could choose two different data eyes (for example, Tap 1 or Tap 18 at 720 Mb/s). However, these *seams* are not an issue with this implementation because data is divided into

16-bit words and striped across the 16 channels. Regardless of which data eye is chosen by the algorithm, the continuity of the 16-bit words is always preserved. As long as the algorithm gets to the center of any data eye, the receiver will see a stream of uncorrupted 16-bit words.

Because the receiver alignment logic only runs once immediately after reset, the resulting dynamic timing must be adequate to ensure error-free operation over the specified voltage and temperature variations that can occur over time. The data-valid window at the receiver input must be wide enough to withstand these variations (receiver drift). Table 11 shows the data-valid window at the ISERDES registers in the DDR receiver. The eyes shown are collective eyes of all 16 channels. The BERT testbench configuration loops back the SFI-4.1 transmitter to the SFI-4.1 receiver. Using pattern generators and error detectors programmed to send and receive a pseudorandom bit sequence (PRBS23), the width of the data-valid window is evaluated using pseudorandom data that closely resembles real user data.

Table 11: **Measurement of Receiver Drift under Extreme Conditions for Multiple Data Rates**

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
Case: 620 Mb/s																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 4																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
Case: 700 Mb/s																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 18																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 11: **Measurement of Receiver Drift under Extreme Conditions for Multiple Data Rates *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
Case: 750 Mb/s																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 16																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Notes:
1. Where “0” is the reference tap determined by the bus-align machine under nominal conditions at 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by the bus-align machine under nominal conditions at 25°C.
3. Device under test is S/N 2194, -1 speed grade.

In all test cases shown in Table 11, the bus-align machine accurately places the sampling point in the center of the data eye (indicated by the "C" in each test case).

After the dynamic timing is established for a given test case under nominal conditions, the device is subjected to extremes of temperature and voltage to stress the receiver timing. For all data rates up to 750 Mb/s, the dynamic timing established after reset under nominal conditions is sufficient to meet timing over all specified extreme conditions (the column with the "C" passes traffic error free under all conditions).

The full datapath of the testbench consists of:

TX → 5" FR-4 → SAMTEC QSE Conn → 12" Ribbon Cable → SAMTEC QSE Conn → 5" FR-4 → RX

Performance is achieved in accordance with the section “Interface Timing Budget,” page 15. Interface performance is not solely a question of the LVDS driver performance specification, but rather a question of adequate timing margin to withstand production and environmental variations. From Table 11, the total amount of variation experienced over temperature and voltage is roughly 450 ps (6 taps at 75 ps per tap). This number should be comparable to the specification for receiver sampling error (T_{SAMP_BUFIO}) shown in DS202, *Virtex-5 Data Sheet*.

Resetting the Interface

Several dependencies determine the order in which circuits should be reset in the interface. The receiver cannot begin the alignment algorithm if the transmitter is not sending the clock. The transmitter must be reset before the receiver, and time must be allowed for the clock to propagate across the link before the receiver comes out of reset. The receiver also cannot begin the alignment algorithm until IDELAYCTRL has recovered from reset, which could takes hundreds of cycles. The recommended reset timing for the interface is shown in Figure 16. This reset timing is implemented in the BERT testbench for this interface.

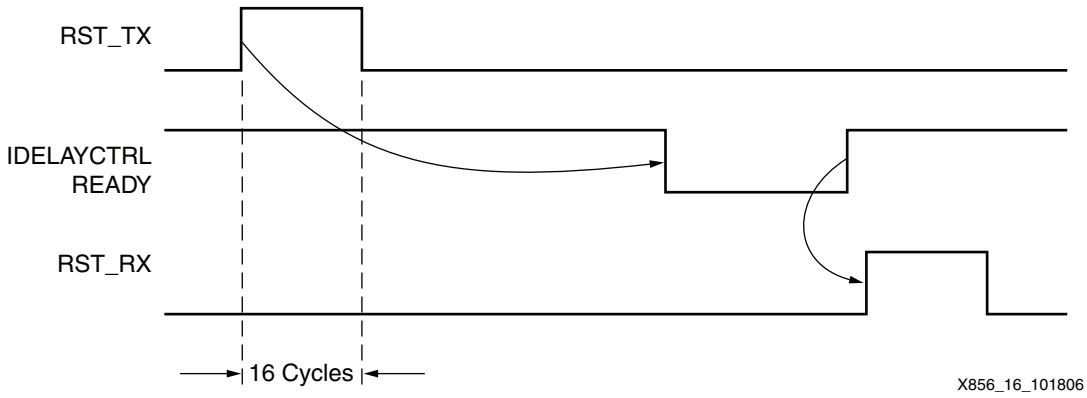


Figure 16: **Recommended Interface Reset Timing**

In the testbench, the TX reset (RST_TX) is used to reset all TX circuitry and also IDELAYCTRL. The IDELAYCTRL reset is asynchronous so driving it with RST_TX is acceptable. The minimum pulse width of IDELAYCTRL reset is 50 ns ($T_{IDELAYCTRL\_RPW}$). For that reason, resets are held High for 16 clock cycles. IDELAYCTRL reset does not need to be driven specifically by RST_TX—it can be an entirely independent reset as long as it adheres to the timing in Figure 16 (with respect to RST_RX). The RX reset (RST_RX) is used to reset all RX circuitry and is asserted when the IDELAYCTRL READY flag goes High, indicating that the IODELAY blocks are calibrated.

The timing of the READY flag in Figure 16 is a potential hazard. Most likely, READY remains High while IDELAYCTRL is being reset because it takes many cycles for IDELAYCTRL to deassert the READY flag. It is easy then to make the mistake of resetting the receiver too early. To avoid this hazard, the RX reset should be asserted only after seeing a deassertion and reassertion of the READY flag.

Conclusion

Based on the design and characterization described in this document, the SFI-4.1 16-Channel SDR reference design meets and exceeds the performance targets in Table 12 under all conditions of process, voltage and temperature. However, to meet these targets over voltage and temperature, the timing budget must be guaranteed according to the analysis in "Interface Timing Budget," page 15. See "Appendix" for further justification of the maximum performance recommendations in Table 12.

Table 12: **Performance of SFI-4.1 Interface**

Speed Grade	Maximum Performance
-1	644 Mb/s(1)
-2	710 Mb/s(1)
-3	710 Mb/s(1)

Notes:

1. These performance targets are dictated by the TBUFIO_MAX_FREQ specification in DS202, *Virtex-5 Data Sheet*. Although this reference design shows significant performance margin, the BUFIO clock networks are only guaranteed to the rates in this table.

Appendix

Refer to "Interface Characterization," page 17 for explanations about how to interpret the data in this appendix. These tables show *collective* data eyes for the entire interface over process, voltage, and temperature (PVT). Three devices from each speed grade were selected for this characterization.

The calibrated center position of the eye (marked by the "C" in Table 14 through Table 16) refers to the calibrated delay setting of the clock channel. Analysis of Table 14, page 22 through Table 16, page 29 shows that the center tap setting for slow and fast parts differ significantly at the same data rate (because the BUS_ALIGN_MACHINE algorithm adjusts for differences in speed).

All data in this appendix is collected using the BERT testbench shown in Figure 2, page 2. The data pattern is PRBS23 and the device/package is XC5VLX50T-FF1136. The transmission path for the cases shown in Table 14 through Table 16 is repeated for convenience:

TX → 5" FR-4 → SAMTEC QSE Conn → 12" Ribbon Cable → SAMTEC QSE Conn → 5" FR-4 → RX

A summary of these characterization results is shown in Table 13. Each of the nine parts were tested at 620, 700, and 750 Mb/s. When the interface is error free on all channels under all extreme conditions of temperature and voltage, the particular test case is designated by a P. A test case is marked FAIL when the interface suffered errors on any channel under any particular condition of voltage and temperature.

Table 13: **Summary of Interface Characterization Results**

Device (S/N)	Speed Grade	620 Mb/s	700 Mb/s	750 Mb/s
2199	-1	P	P	P
2194	-1	P	P	P
2219	-1	P	P	P
001	-2	P	P	P
002	-2	P	P	P
003	-2	P	P	P
004	-3	P	P	P
005	-3	P	P	P
006	-3	P	P	P

Table 14: **Measurement of Receiver Drift under Extreme Conditions at 620 Mb/s**

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2199, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 5																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 2194, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 4																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 14: **Measurement of Receiver Drift under Extreme Conditions at 620 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2219, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	P	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
25°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 19																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bus-align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by the bus-align machine under nominal conditions at 25°C.
3. If the center tap setting is too low to measure the full RX data eye, the width of an eye further along in the delay chain is measured and used to fill in part of the table.

Table 15: **Measurement of Receiver Drift under Extreme Conditions at 700 Mb/s**

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2199, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 1																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 2194, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 18																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 15: **Measurement of Receiver Drift under Extreme Conditions at 700 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2219, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 13																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 001, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 2																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 15: **Measurement of Receiver Drift under Extreme Conditions at 700 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 002, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 19																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 003, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
Center Tap Setting	Tap 19																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 15: **Measurement of Receiver Drift under Extreme Conditions at 700 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 004, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 7																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 005, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 4																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 15: **Measurement of Receiver Drift under Extreme Conditions at 700 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 006, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 6																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bus-align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by the bus-align machine under nominal conditions at 25°C.
3. If the center tap setting is too low to measure the full RX data eye, the width of an eye further along in the delay chain is measured and used to fill in part of the table.

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 750 Mb/s**

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2199, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 17																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 2194, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 16																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 750 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 2219, Speed Grade: -1																							
25°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 10																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 001, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 17																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 750 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 002, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 16																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 003, Speed Grade: -2																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F	F
Center Tap Setting	Tap 16																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 750 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 004, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, -5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F	F
Center Tap Setting	Tap 5																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						
S/N 005, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
0°C, +5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 2																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 750 Mb/s *(Continued)***

Condition	IODELAY Taps[1]																						
	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
S/N 006, Speed Grade: -3																							
25°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F
25°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, -5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, -5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
Center Tap Setting	Tap 4																						
Conclusion	Error free under all conditions when calibrated under nominal conditions to position C																						

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bus-align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by the bus-align machine under nominal conditions at 25°C.
3. If the center tap setting is too low to measure the full RX data eye, the width of an eye further along in the delay chain is measured and used to fill in part of the table.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/01/06	1.0	Initial Xilinx release.
04/09/07	1.1	To use the SFI-4.1 standard, a transmitter must transmit a clock with its rising edge centered in the TX data bit period (180° phase difference). In the first version of this application note, the clock and data are phase-aligned (0° phase difference). Because the TX needed to be changed, the RX alignment algorithm has been changed to operate under the new assumption that the rising edge of the incoming clock is centered in the incoming data eye.
05/19/07	1.2	Clarified clock and data channel phases on page 4.