

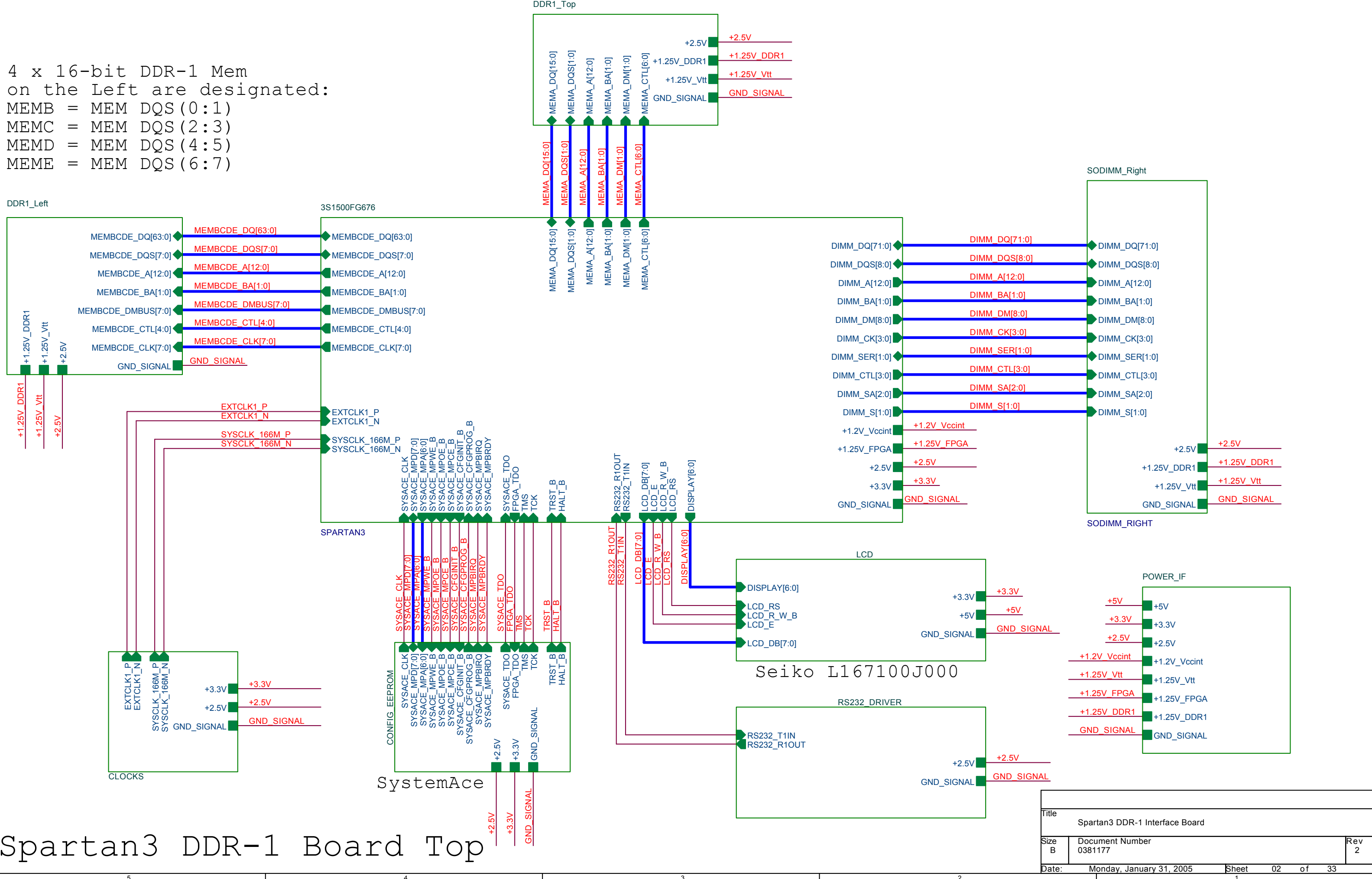
Sheet# Rev# Description

Revision Notes are on Sheet 33

Sheet#	Rev#	Description	Part #	Ref. Des. #:
1	6	Notes Page		
2	2	Top Hierarchical Block Diagram		
3	2	Clock Sources: Epson EC2121CA-166M OSC, SMA's	C452	Q5
4	2	SystemAce Controller & CF Socket, JTAG Conn.		
5	2	DDR-1 Micron MT46V16M16P-75 - MEM Top	D12	R738
6	1	DDR-1 Mem Top Termination Resistors	DD1	SW6
7	3	DDR-1 Micron MT46V16M16P-75 - MemL 01		
8	1	DDR-1 MemL 01 Termination Resistors	J6	U14
9	2	DDR-1 Micron MT46V16M16P-75 - MemL 23	L4	
10	1	DDR-1 MemL 23 Termination Resistors		
11	2	DDR-1 Micron MT46V16M16P-75 - MemL 45	P42	Y2
12	1	DDR-1 MemL 45 Termination Resistors		
13	2	DDR-1 Micron MT46V16M16P-75 - MemL 67		
14	3	DDR-1 MemL 67 Termination Resistors		
15	3	DDR-1 SODIMM 200-pin Socket "Right"		
16	1	DDR-1 SODIMM Termination Resistors		
17	1	LCD I/F Connector, MC74LCX541D level shifters, 7-Segment Display		
18	2	RS232 I/F MAX3316ECUP 2.5V & DB9F Serial Conn (entire pages is DNA)		
19	2	3S1500FG676 BANK0 MemL A[12:0] I/F, SYSCLK INPUT, 2XHEADER I/F, Vcco=+2.5V		
20	2	3S1500FG676 BANK1 Mem Top I/F, Vcco=+2.5V		
21	2	3S1500FG676 BANK2 SODIMM Socket I/F, Vcco=+2.5V		
22	2	3S1500FG676 BANK3 SODIMM Socket I/F, Vcco=+2.5V		
23	2	3S1500FG676 BANK4 SODIMM Socket I/F, SYSACE I/F, Vcco=+2.5V		
24	2	3S1500FG676 BANK5 LCD I/F, RS232 I/F, Vcco=+2.5V		
25	2	3S1500FG676 BANK6 MemL I/F, Vcco=+2.5V		
26	2	3S1500FG676 BANK7 MemL I/F, Vcco=+2.5V		
27	4	3S1500FG676 Config Bank, XCONFIG Conn., Mode Sw, Prog PB Sw		
28	2	3S1500FG676 Power Pins: GND, Vccaux (+2.5V), Vccint (+1.2V)		
29	2	Power: +2.5V, +1.25V Vtt, +1.25V DDR1		
30	5	Power: +3.3V, +1.2V Vccint, +1.25V FPGA		
31	2	Decoupling Caps: +1.25V Vtt, +1.25V FPGA, +1.25V DDR1		
32	6	Decoupling Caps: +5V, +3.3V, +2.5V, +1.2V Vccint		
33	6	Rev. Notes		

Title		
Spartan3 DDR-1 Interface Board		
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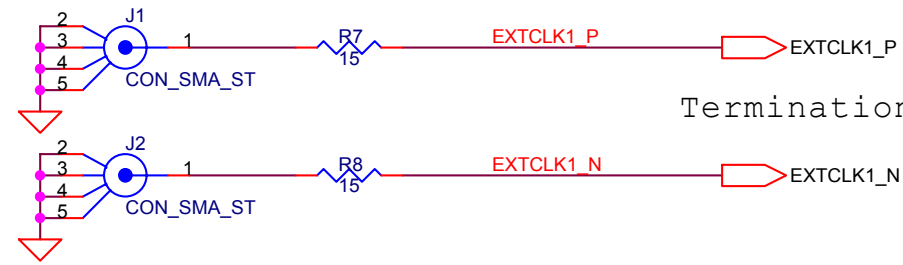
4 x 16-bit DDR-1 Mem  
 on the Left are designated:  
 MEMB = MEM DQS (0:1)  
 MEMC = MEM DQS (2:3)  
 MEMD = MEM DQS (4:5)  
 MEME = MEM DQS (6:7)



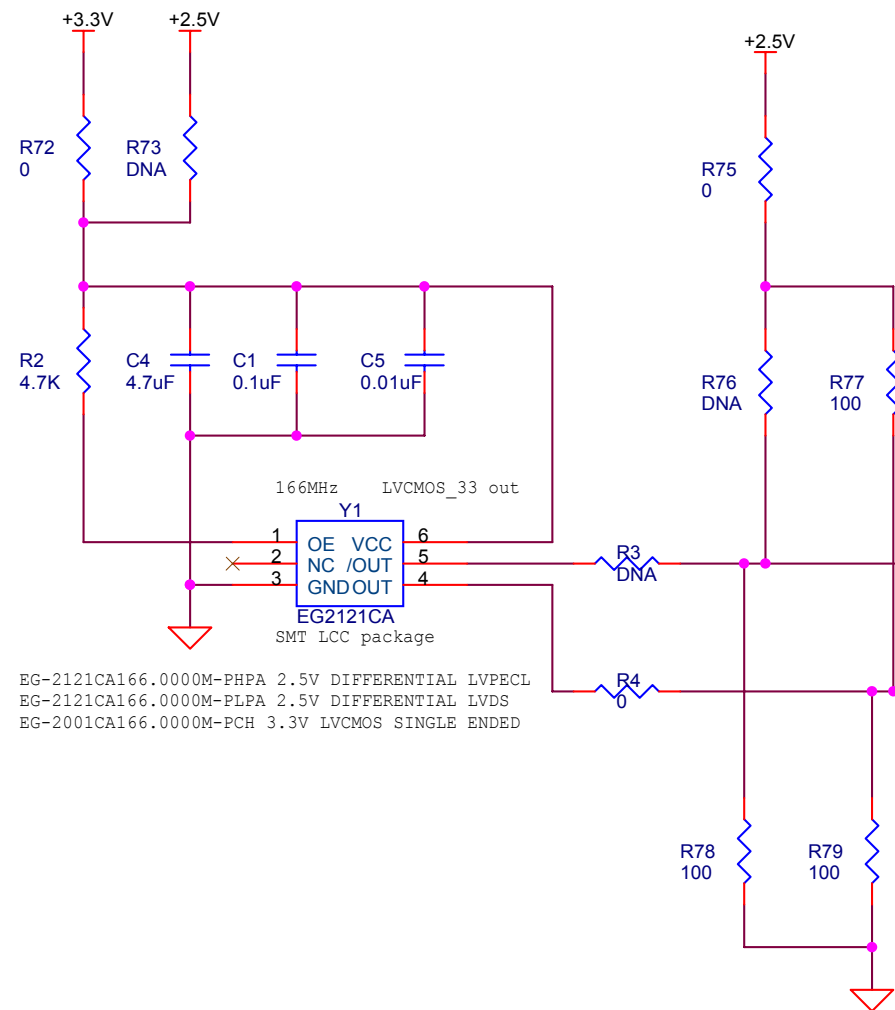
# Spartan3 DDR-1 Board Top

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Differential Inputs for Test Equip. clock



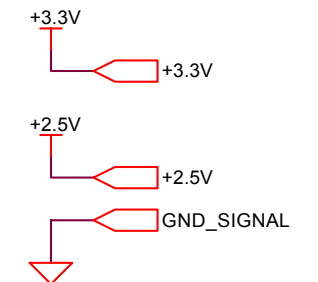
Termination resistors at FPGA Bank4 (Sheet 23)



EG-2121CA166.0000M-PHPA 2.5V DIFFERENTIAL LVPECL  
 EG-2121CA166.0000M-PLPA 2.5V DIFFERENTIAL LVDS  
 EG-2001CA166.0000M-PCH 3.3V LVCMOS SINGLE ENDED

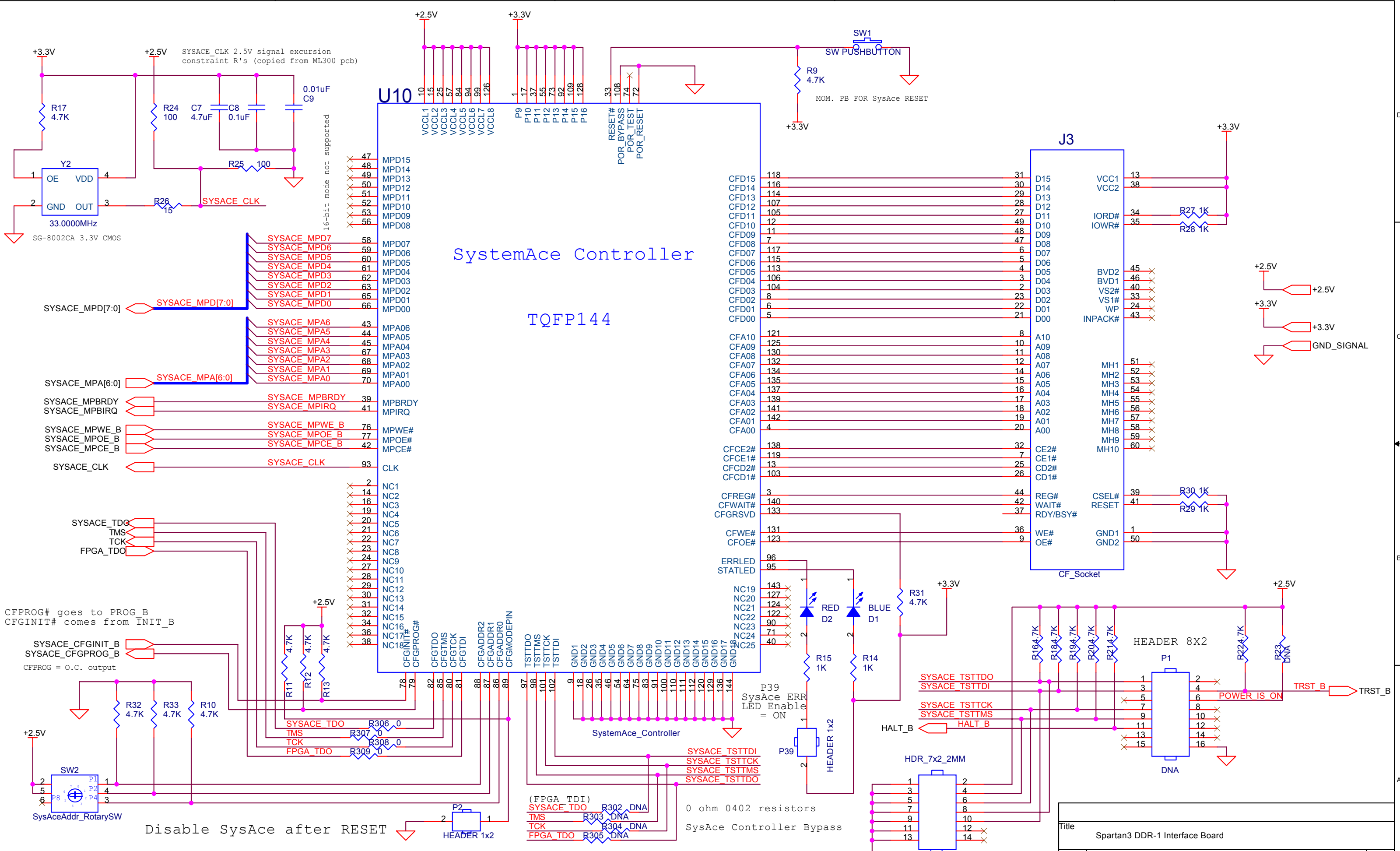
Oscillator	Osc. Power	Resistor Configuration
EG-2121CA 2.5V DIFF'L LVPECL Connect the diff'l P & N outputs No bias network required	+2.5V	R73 0 ohms R72 DNA R4 0 ohms R3 0 ohms R76, R77, R78, R79 all DNA
EG-2001CA 3.3V LVCMOS SINGLE ENDED Connect the SINGLE ENDED "P" output Bias the S.E. output to 2.5V center Pulldown unused diff'l N clock sig	+3.3V	R72 0 ohms R73 DNA R4 0 ohms R3 DNA R77 100 ohms R79 100 ohms R78 100 ohms

50 ohm LVPECL term. R's at FPGA Bank0 (Sheet 19)  
 100 ohm LVDS parallel term. R at FPGA Bank0 (Sheet 19)



CLOCKS

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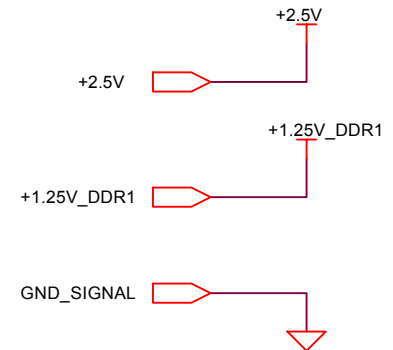
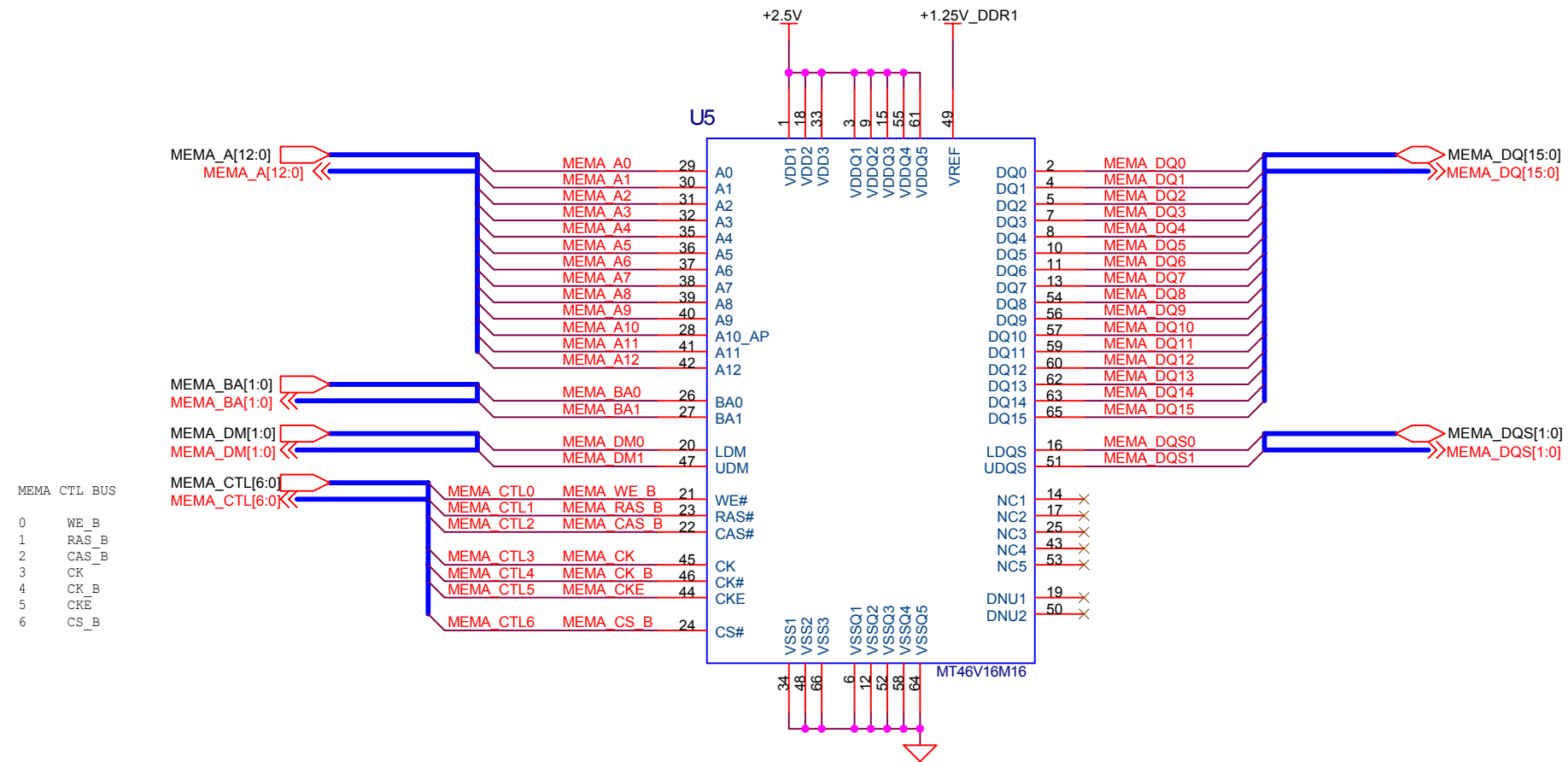


CONFIG via SystemAce CF

Normal=R306,R307,R308,R309 In, R302,R303,R304,R305 Out  
Bypass=R302,R303,R304,R305 In, R306,R307,R308,R309 Out

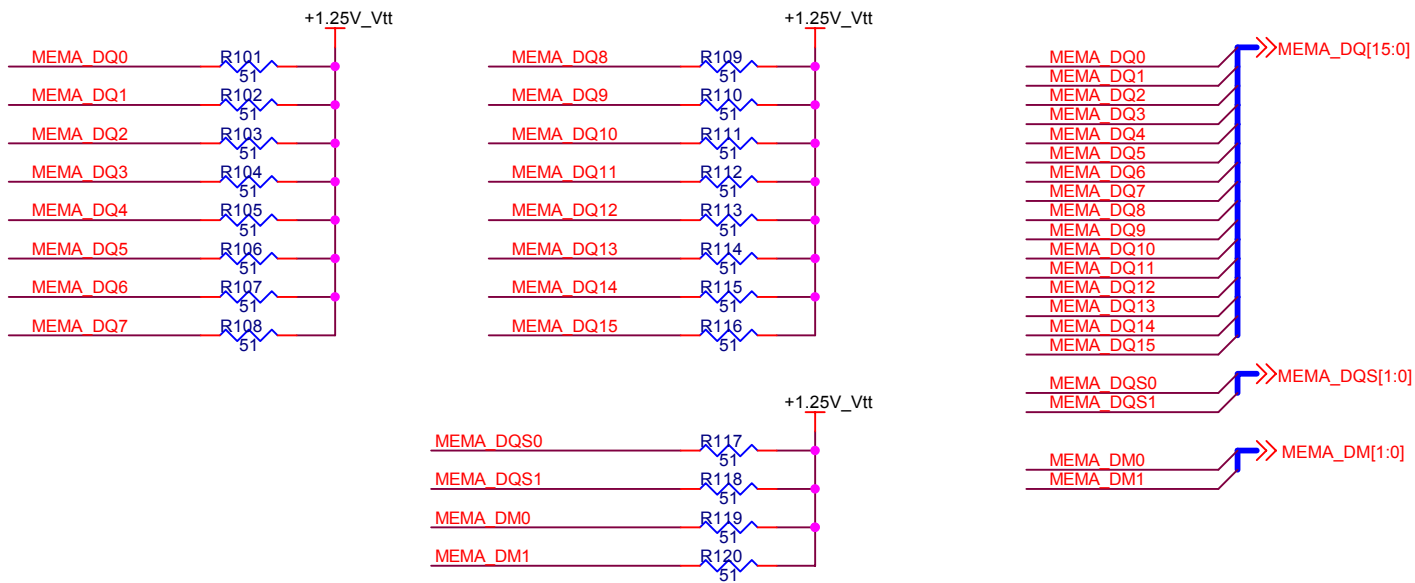
Title		
Spartan3 DDR-1 Interface Board		
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# Single DDR-1 Memory on Top is designated MEMA

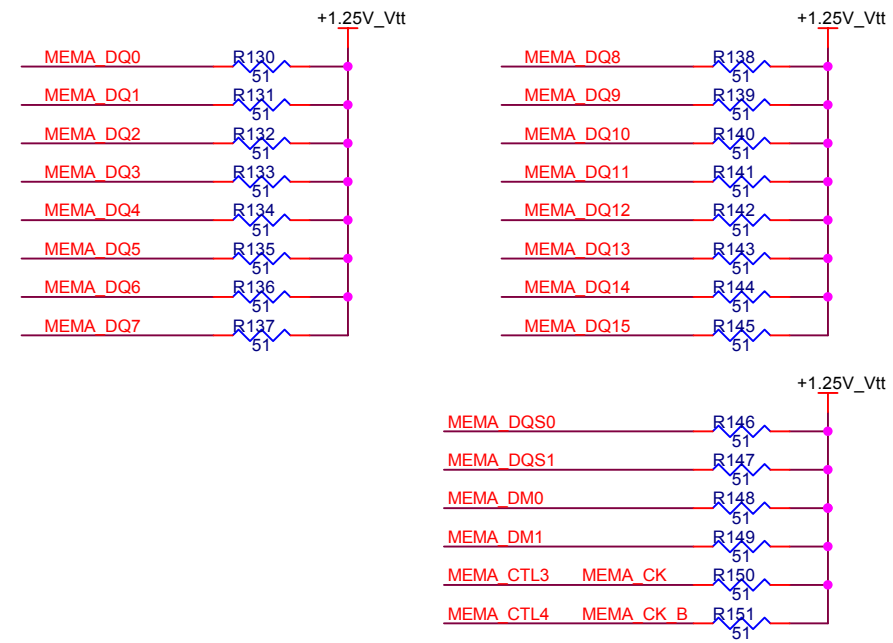


MT46V16M16TG-6P Single DDR-1 Memory on Top (MEM\_Top)

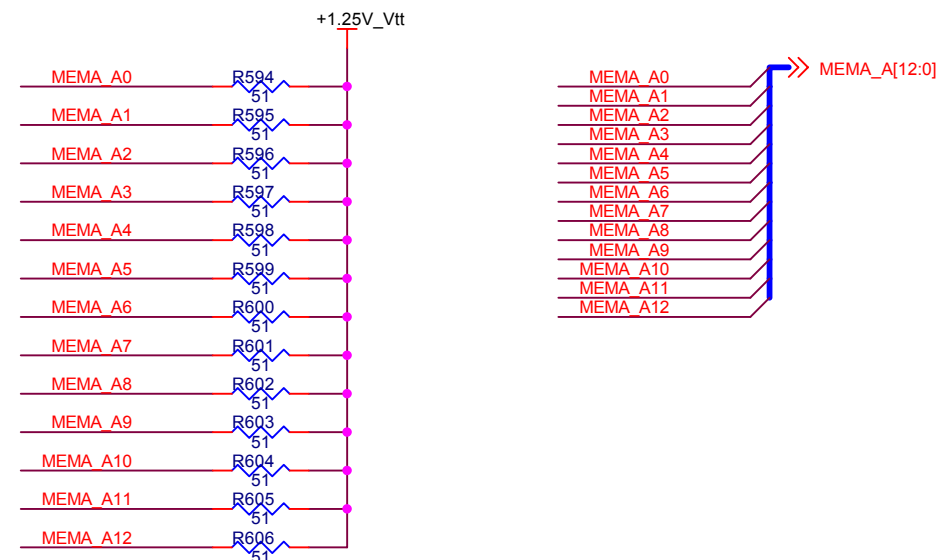
Title		
Spartan3 DDR-1 Board		
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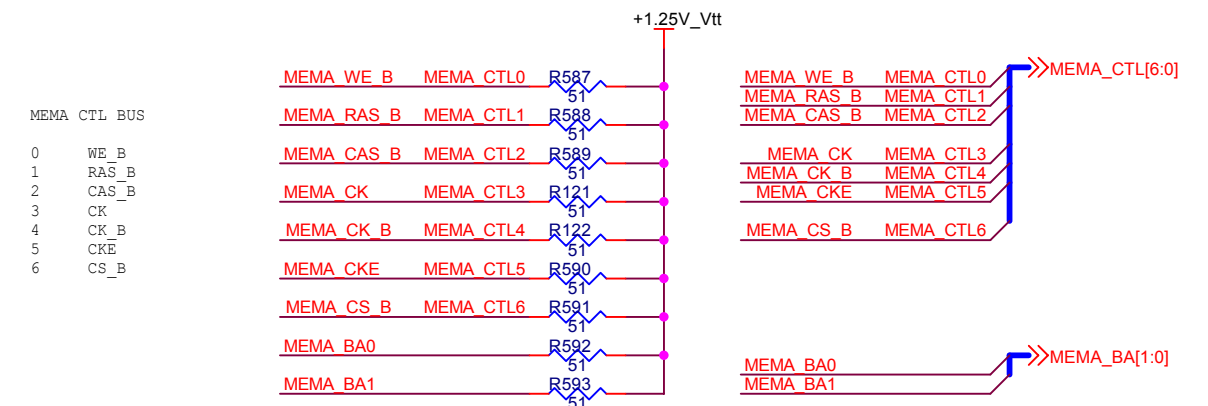
Place these resistors close to the FPGA



Place these resistors close to the MEMA



Common address signals  
Place these resistors close to the MEMA

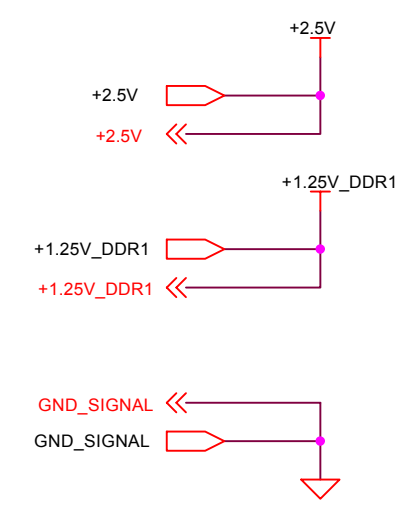
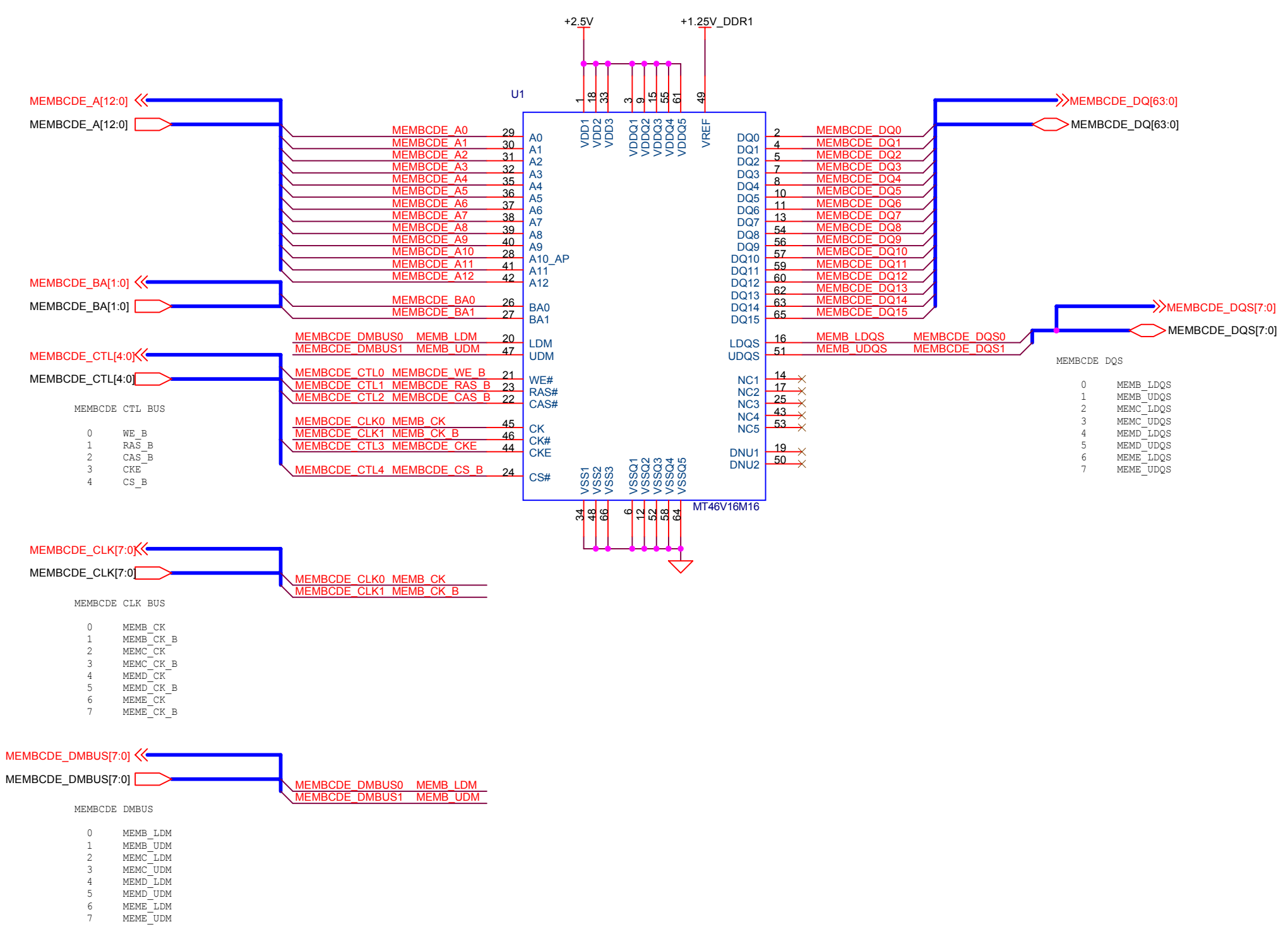


Common control signals  
Place these resistors close to the MEMA

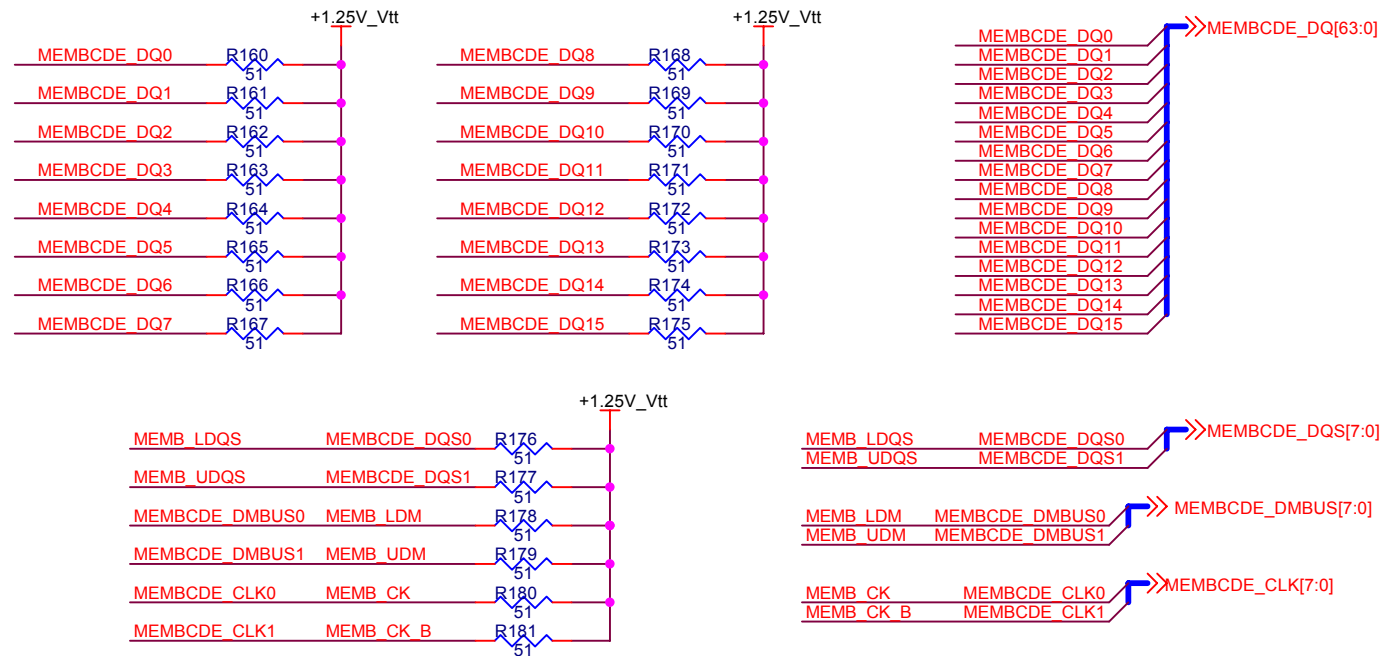
# MEMA MT46V16M16TG-6P (Top) Termination Resistors



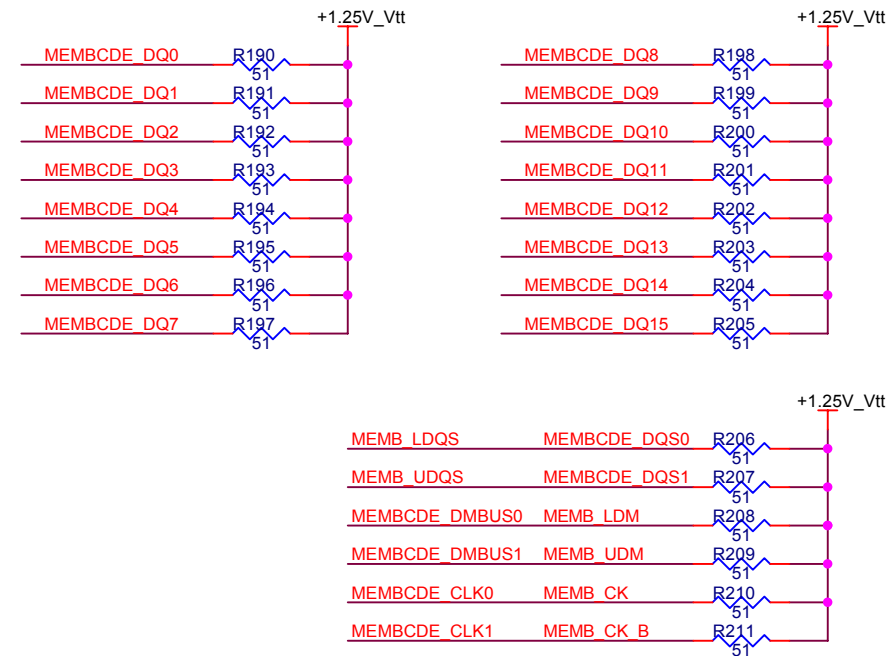
Title Spartan3 DDR-1 Board		
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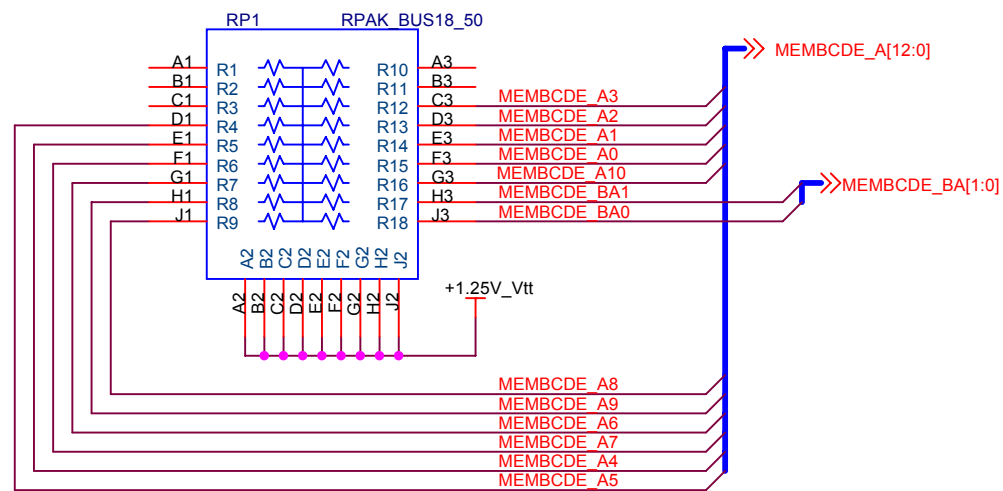
MT46V16M16TG-6P DDR-1 Memory on Left MEMB = MEM DQS (0:1)



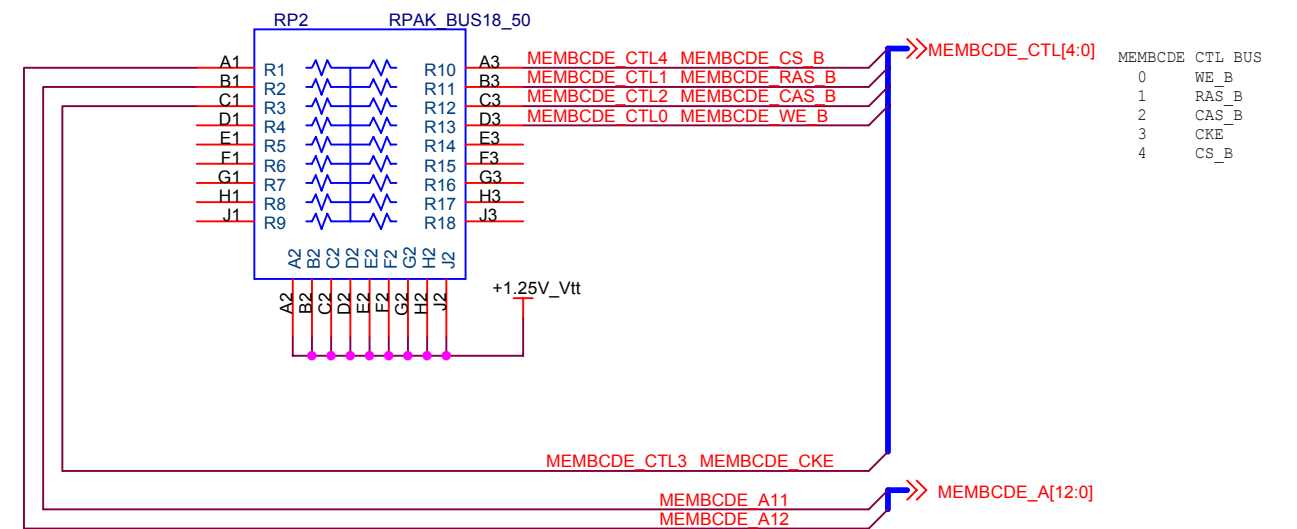
Place these resistors close to the FPGA



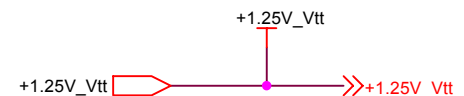
Place these resistors close to the MEMB/U1

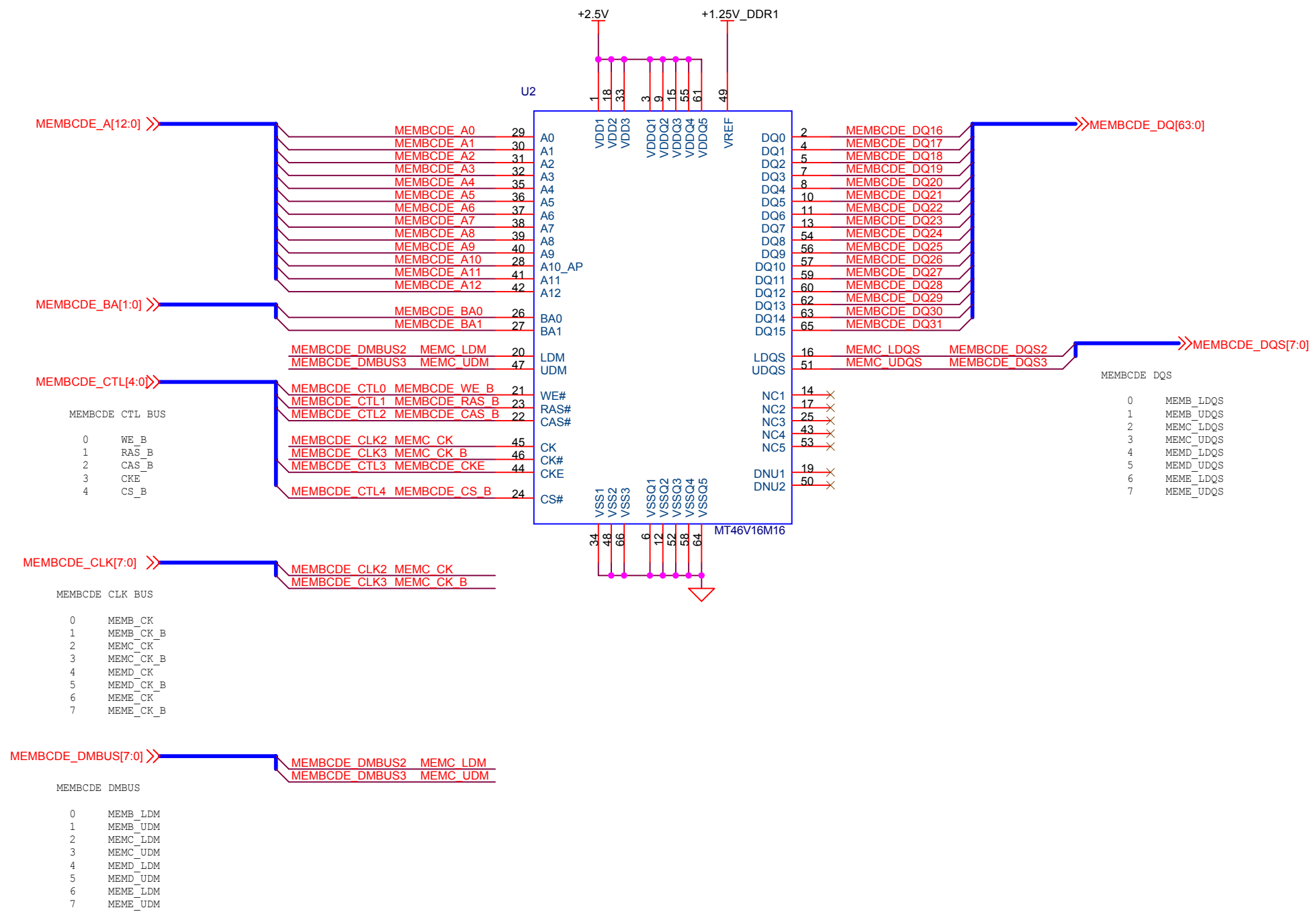


Common address signals  
Place this Rpak at end of bus "T"



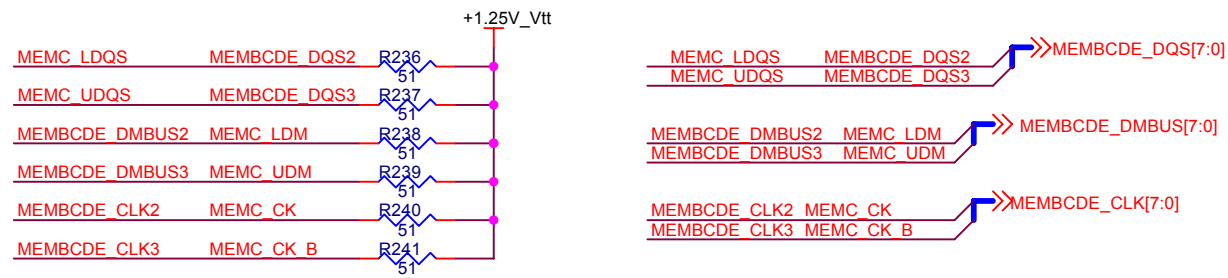
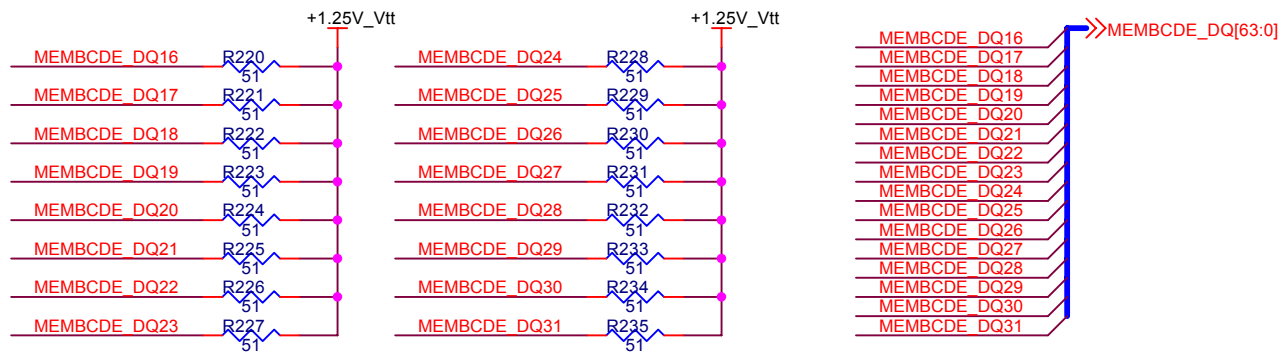
Common control signals  
Place this Rpak at end of bus "T"



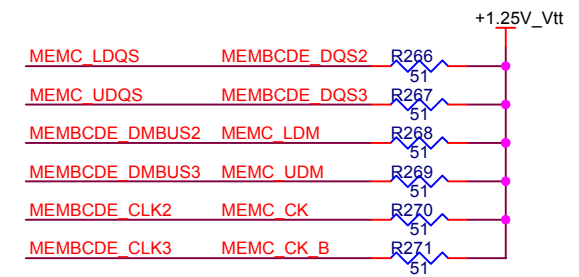
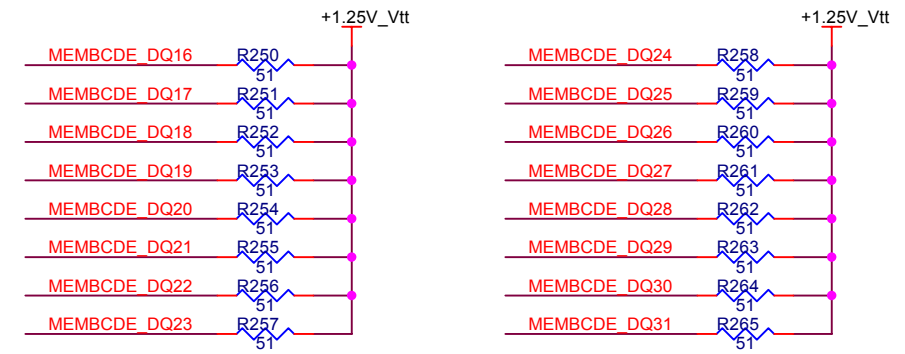


MT46V16M16TG-6P DDR-1 Memory on Left MEMC = MEM DQS (2:3)

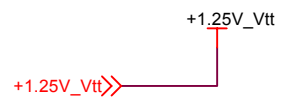
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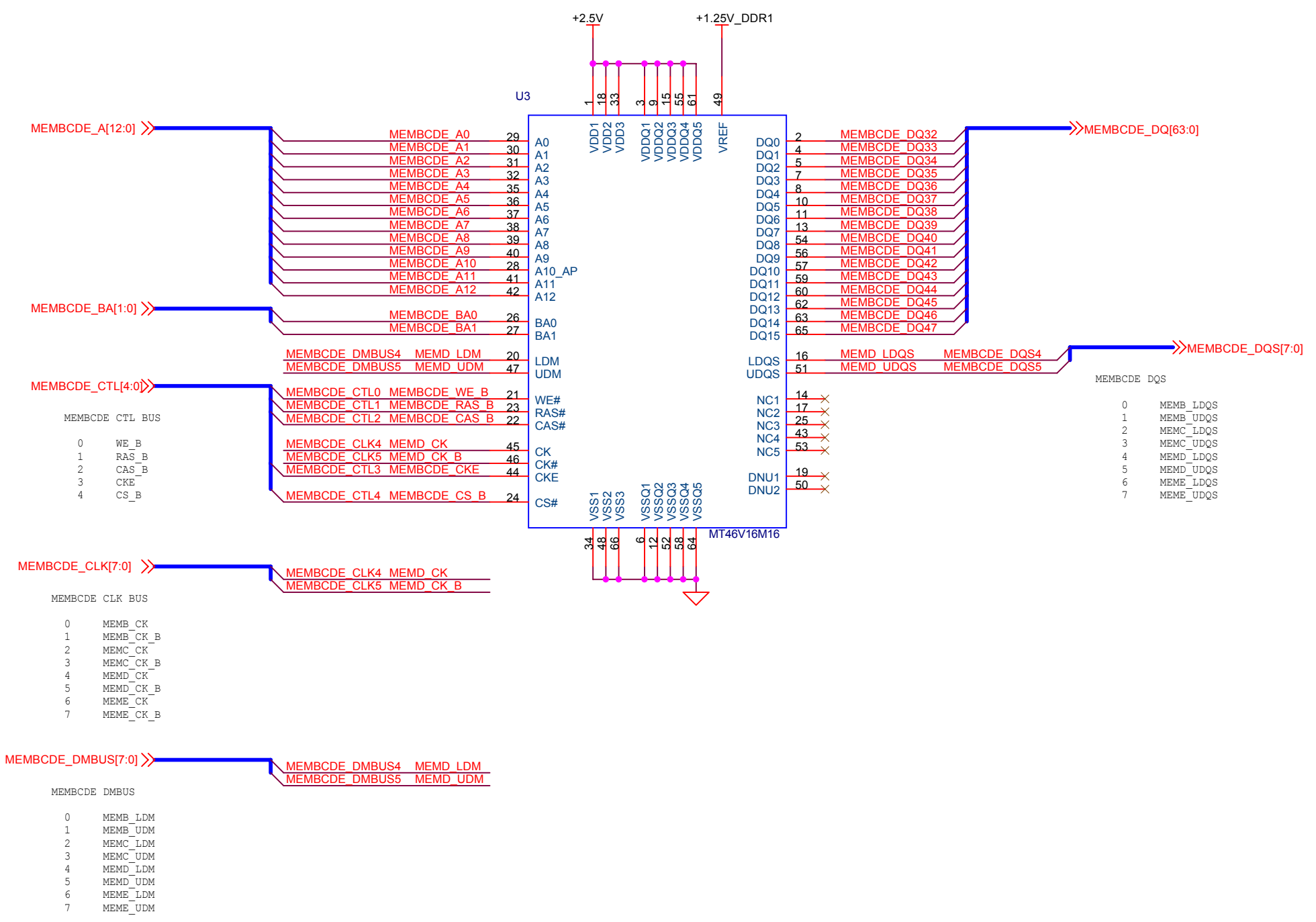


Place these resistors close to the FPGA



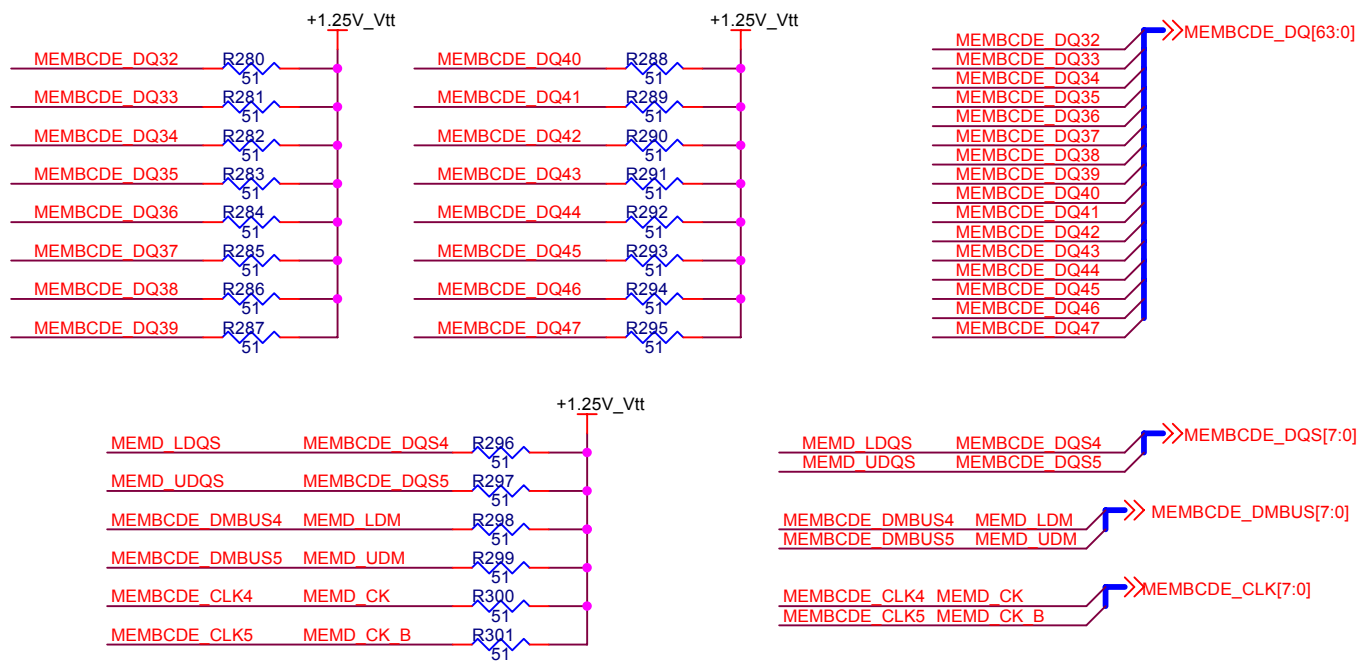
Place these resistors close to the MEMC



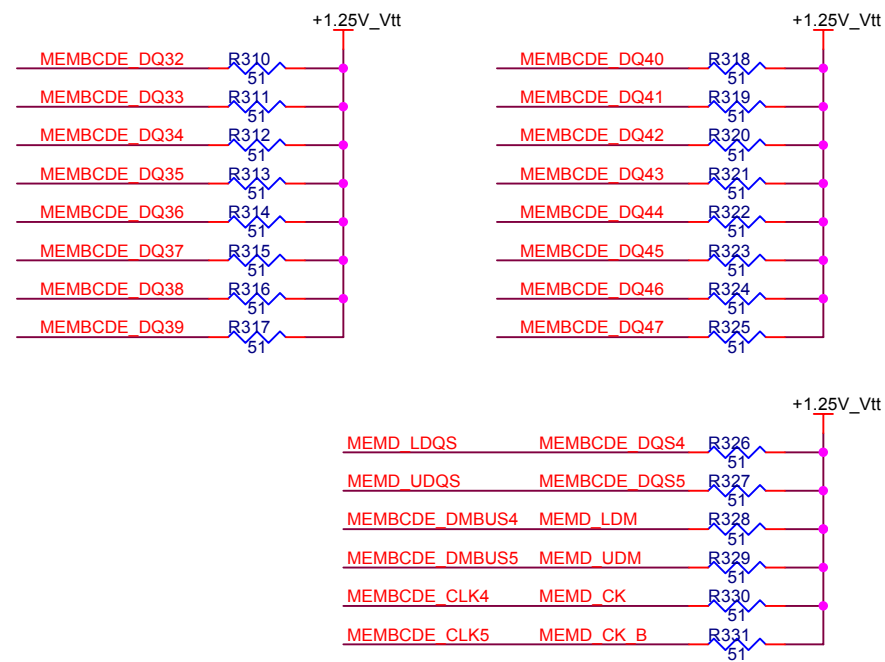


MT46V16M16TG-6P DDR-1 Memory on Left MEMD = MEM DQS (4:5)

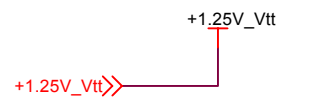
Title		
Spartan3 DDR-1 Board		
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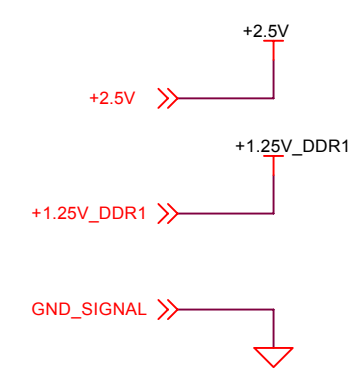
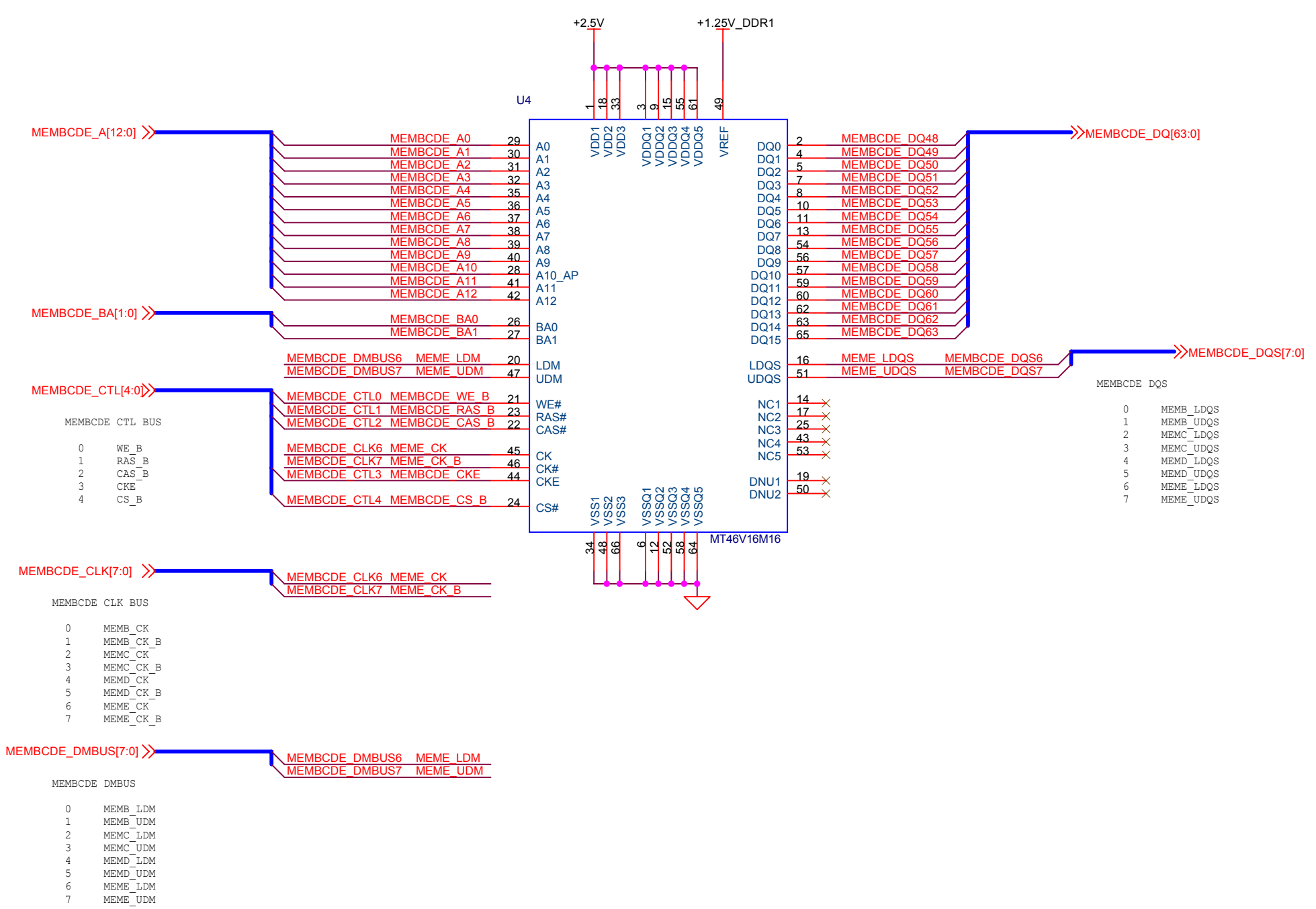


Place these resistors close to the FPGA

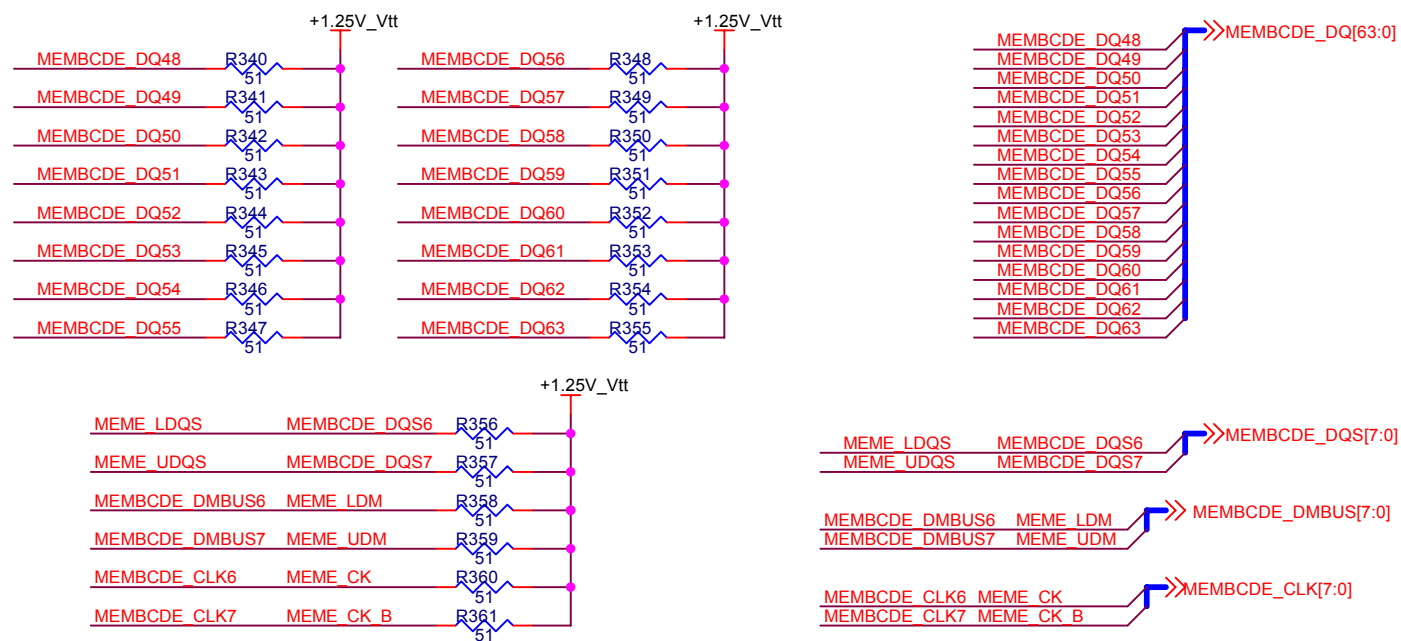


Place these resistors close to the MEMD

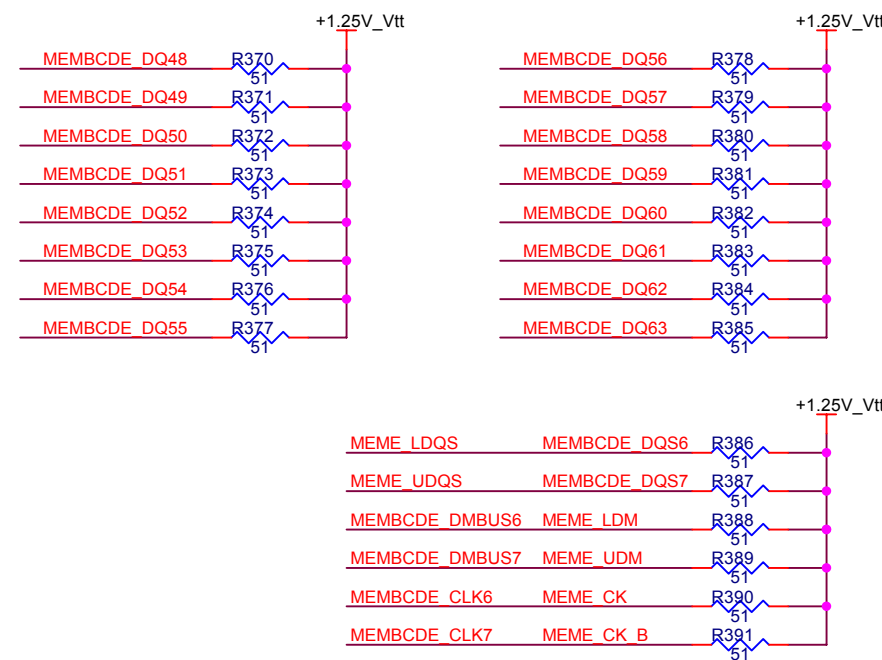




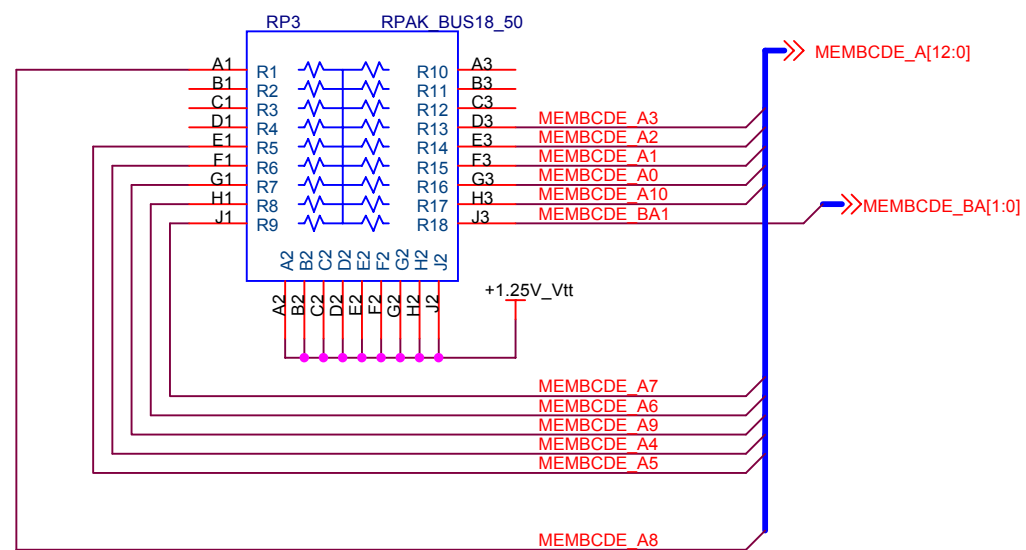
MT46V16M16TG-6P DDR-1 Memory on Left MEME = MEM DQS (6:7)



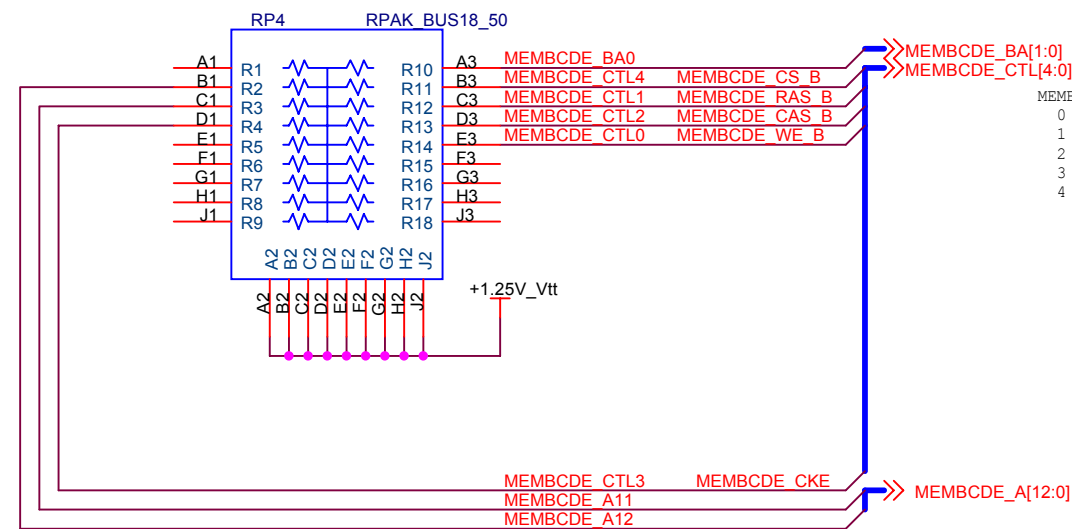
Place these resistors close to the FPGA



Place these resistors close to the MEME/U4



Common address signals  
Place this Rpak at end of bus daisy-chain



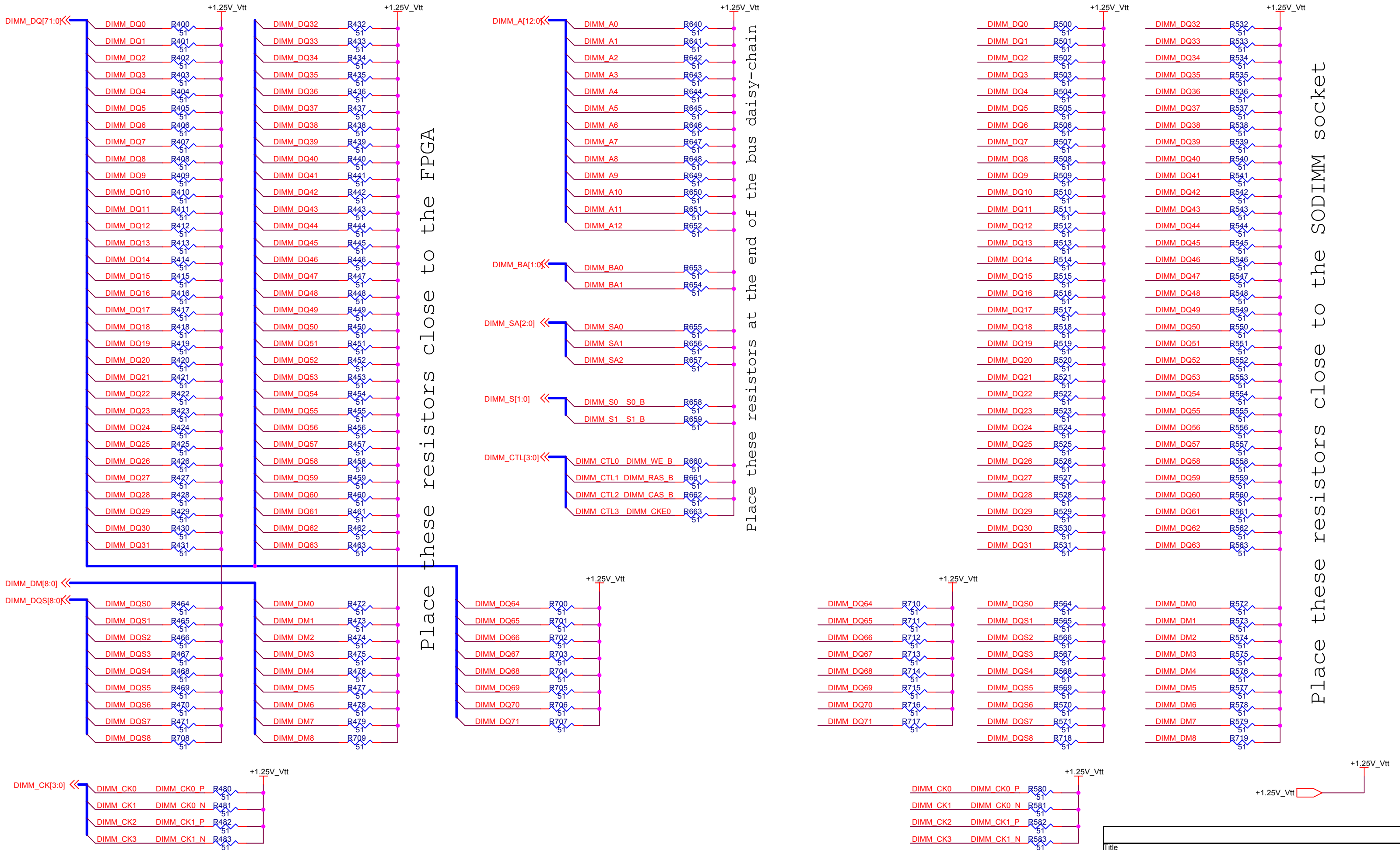
Common control signals  
Place this Rpak at end of bus daisy-chain

MEME MT46V16M16TG-6P (Left) "Upper" Termination Resistors



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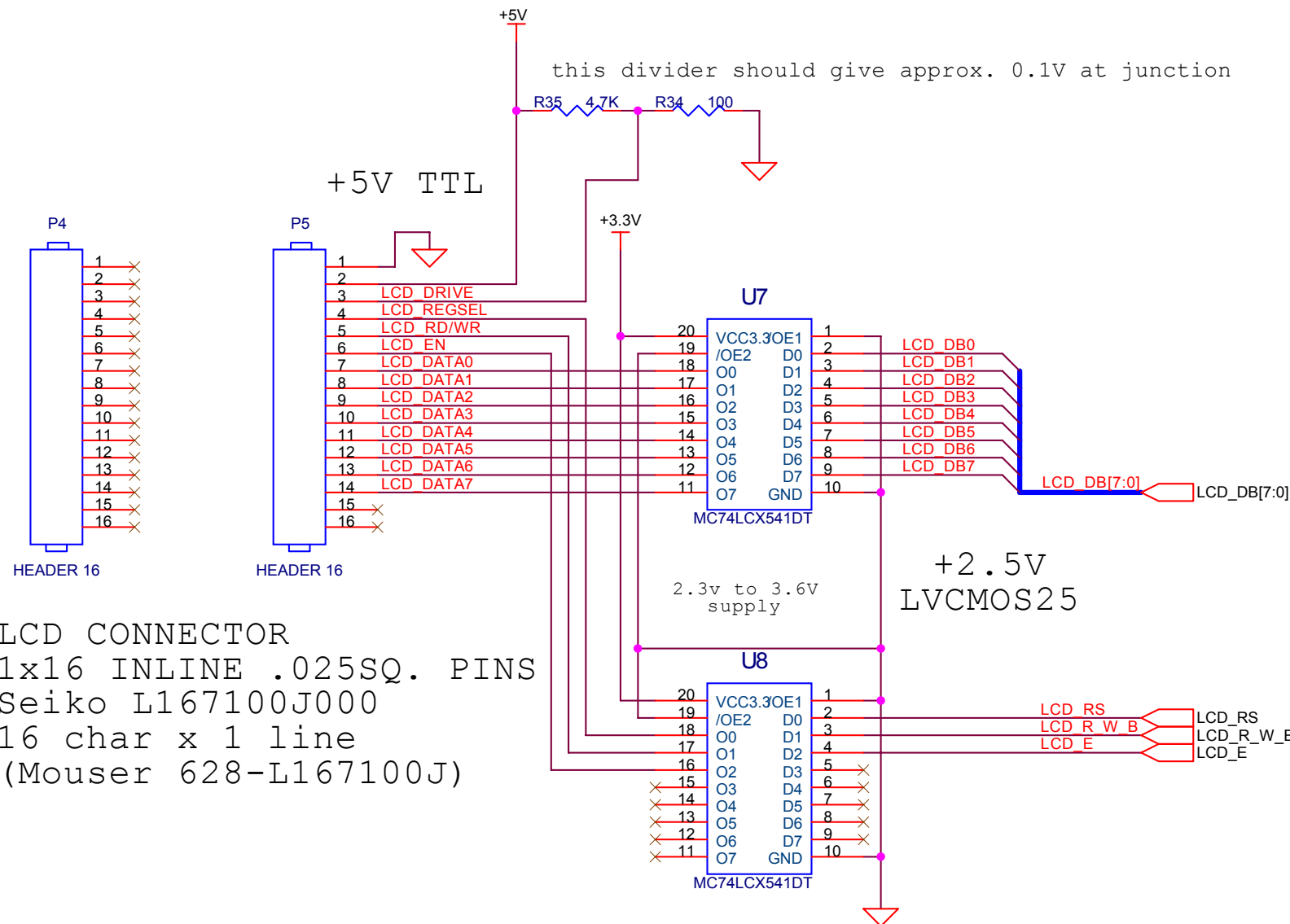




# MT4VDDT1664HY 128MB Memory Termination Resistors

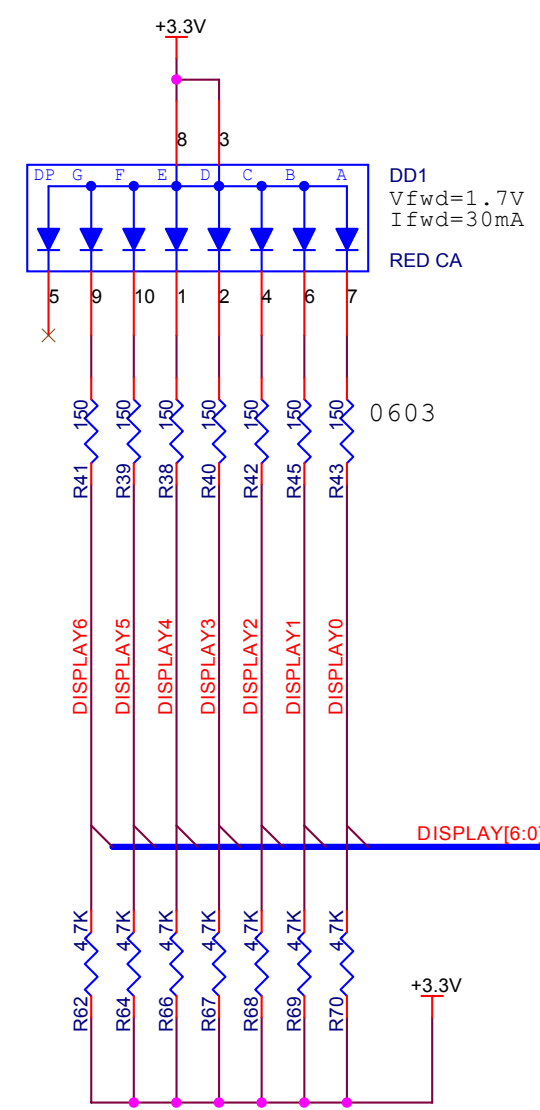
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This LCD requires two rows of 16 pins to support it physically  
 Place the 1x16 SIP headers 31mm apart per the LCD spec sheet

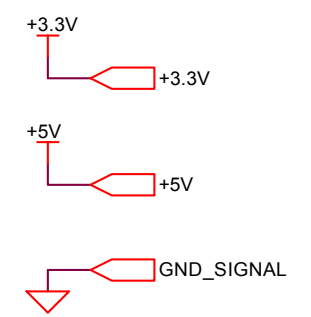
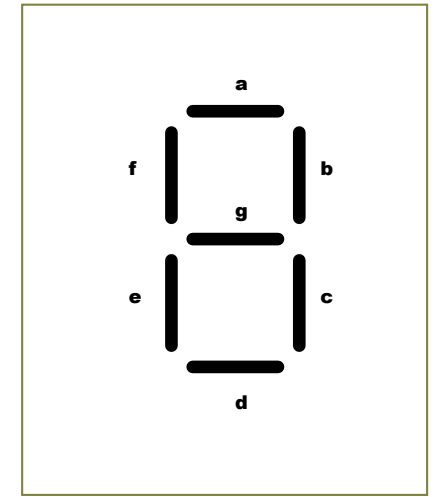


LCD CONNECTOR  
 1x16 INLINE .025SQ. PINS  
 Seiko L167100J000  
 16 char x 1 line  
 (Mouser 628-L167100J)

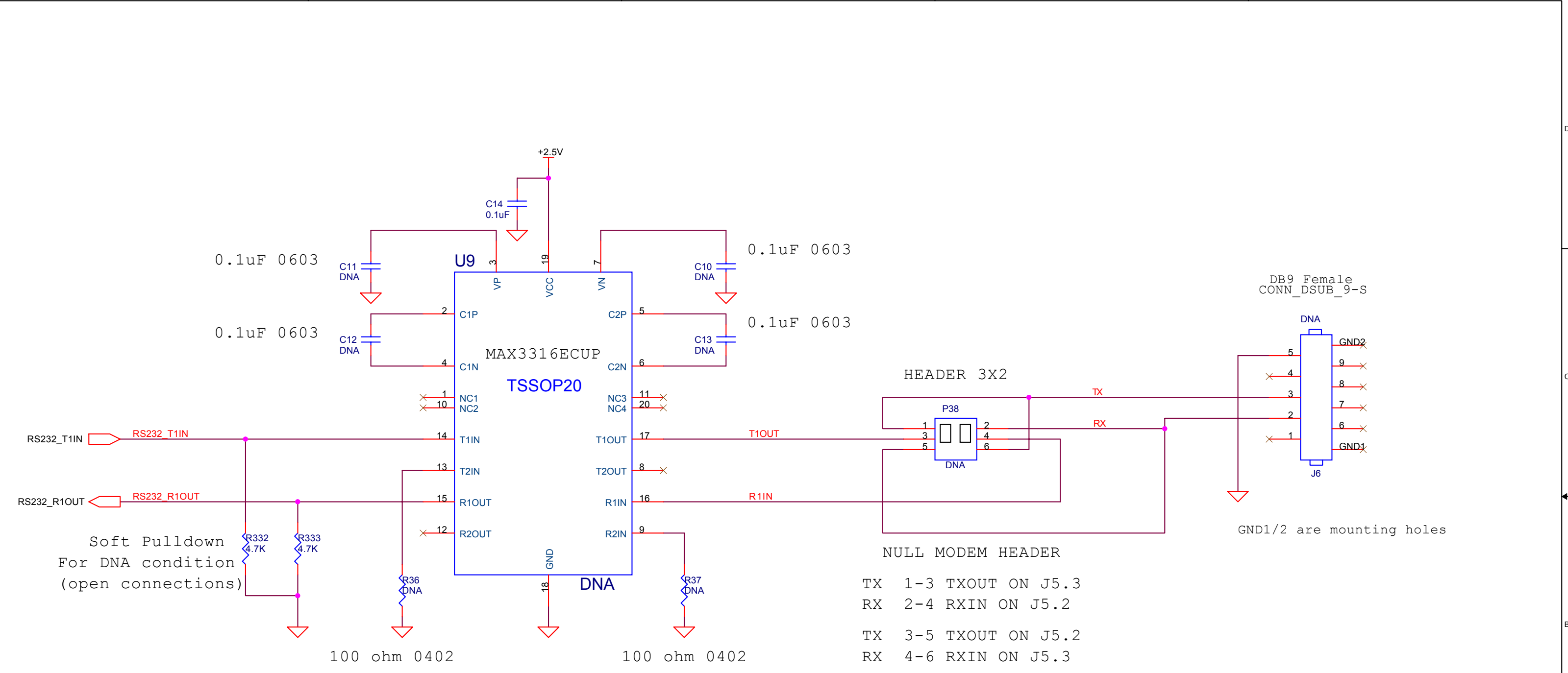
LCD



4.7K 0402 Pullups to keep display turned off at power on



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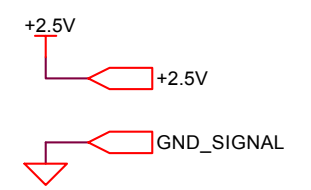


NULL MODEM HEADER

TX 1-3 TXOUT ON J5.3  
 RX 2-4 RXIN ON J5.2

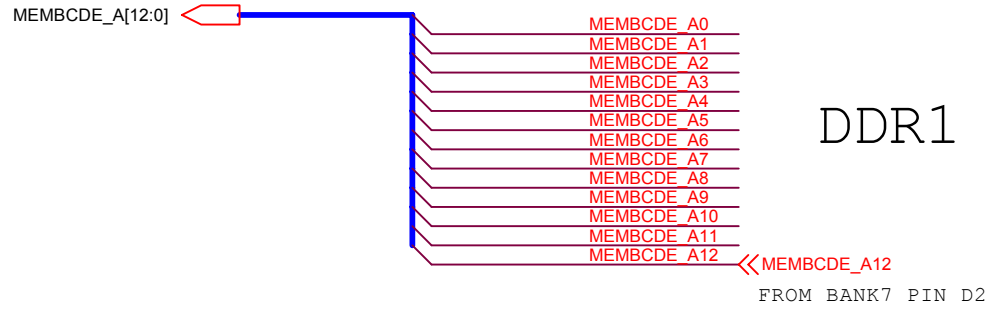
TX 3-5 TXOUT ON J5.2  
 RX 4-6 RXIN ON J5.3

RS232 Components are not installed, and will not be tested



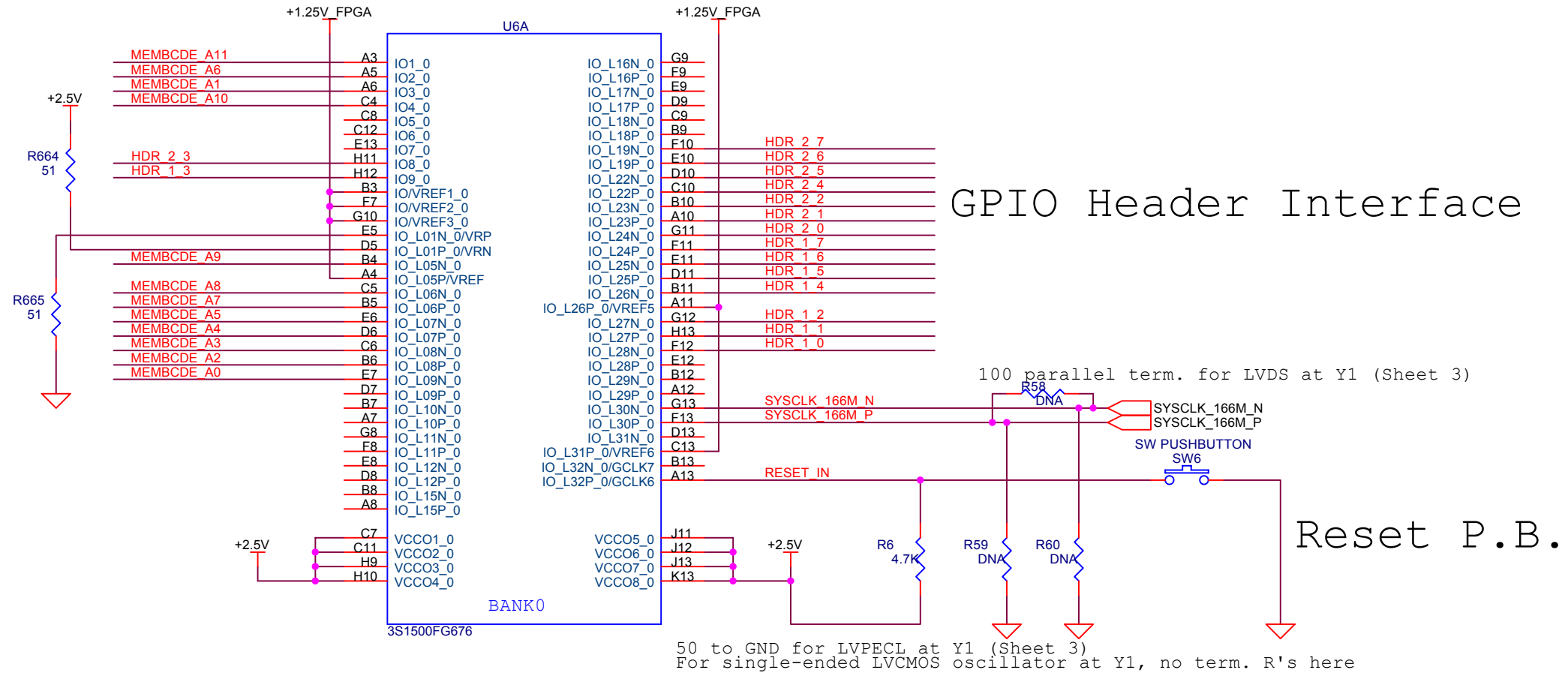
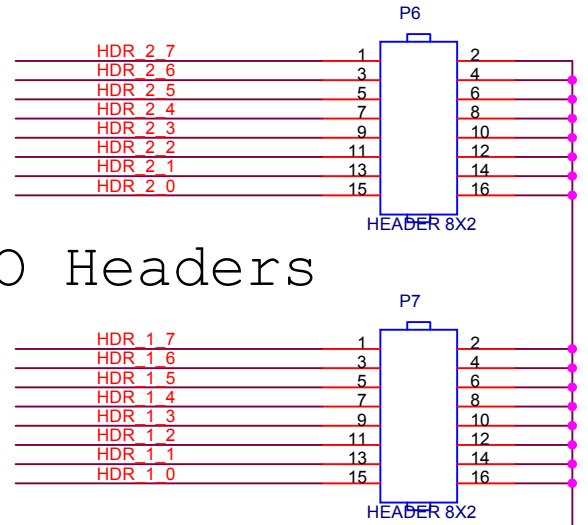
# RS232 DRIVER

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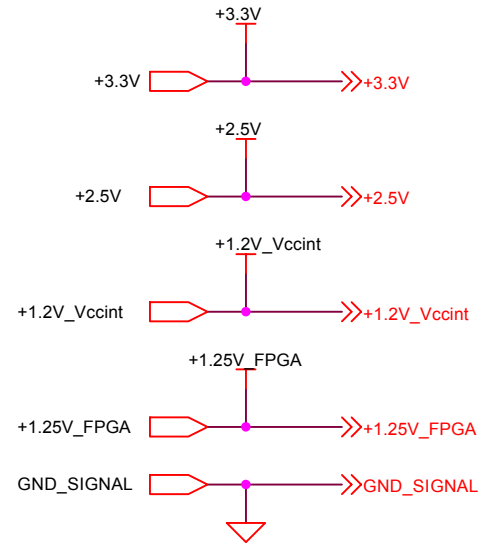


## DDR1 x4 (MEMB - MEME) "Left" Side Interface

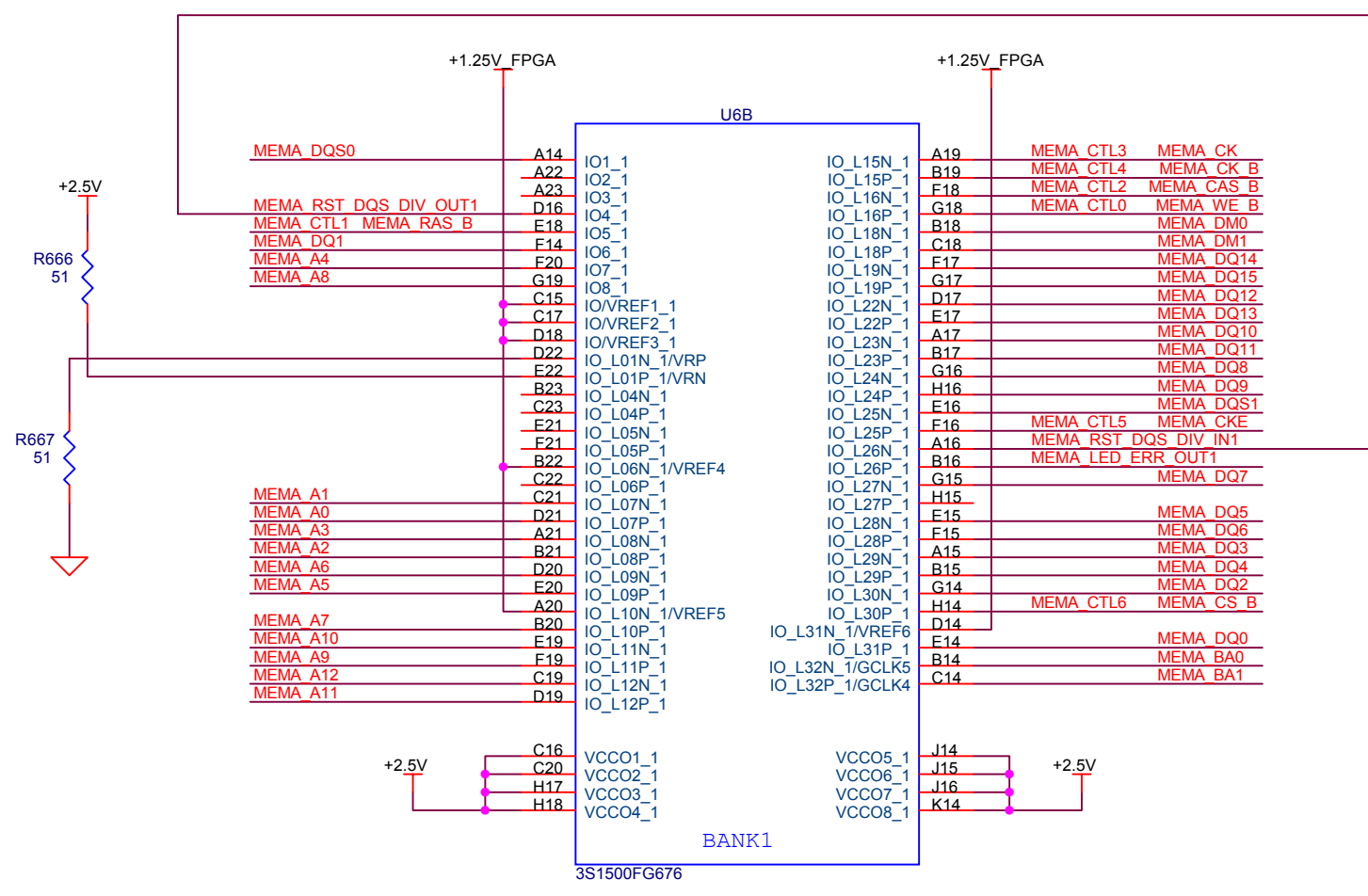
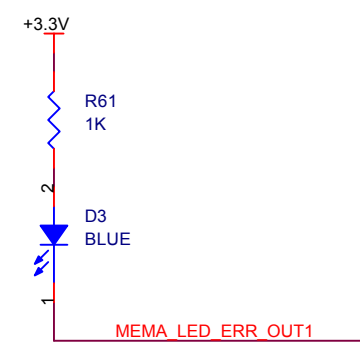
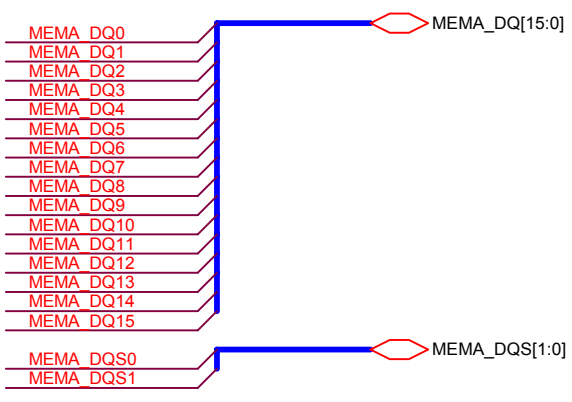
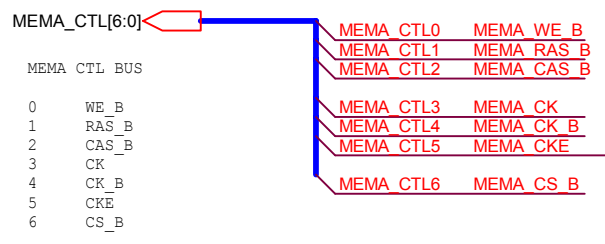
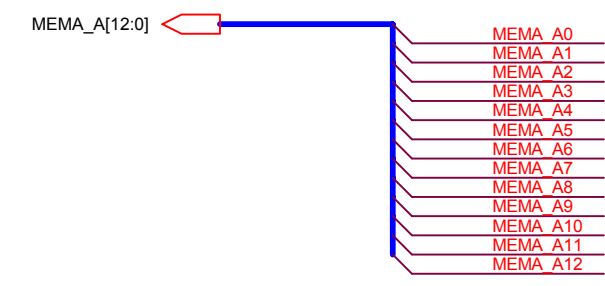
### GPIO Headers



## DDR1 x4 (MEMB - MEME) "Left" Side Interface Osc. Y1 Clock Interface Reset P.B. Interface GPIO Header Interface

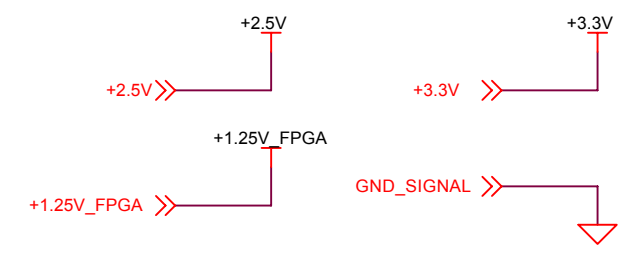


4 x 16-bit DDR-1 Mem  
on the Left are designated:  
MEMB = MEM DQS (0:1)  
MEMC = MEM DQS (2:3)  
MEMD = MEM DQS (4:5)  
MEME = MEM DQS (6:7)



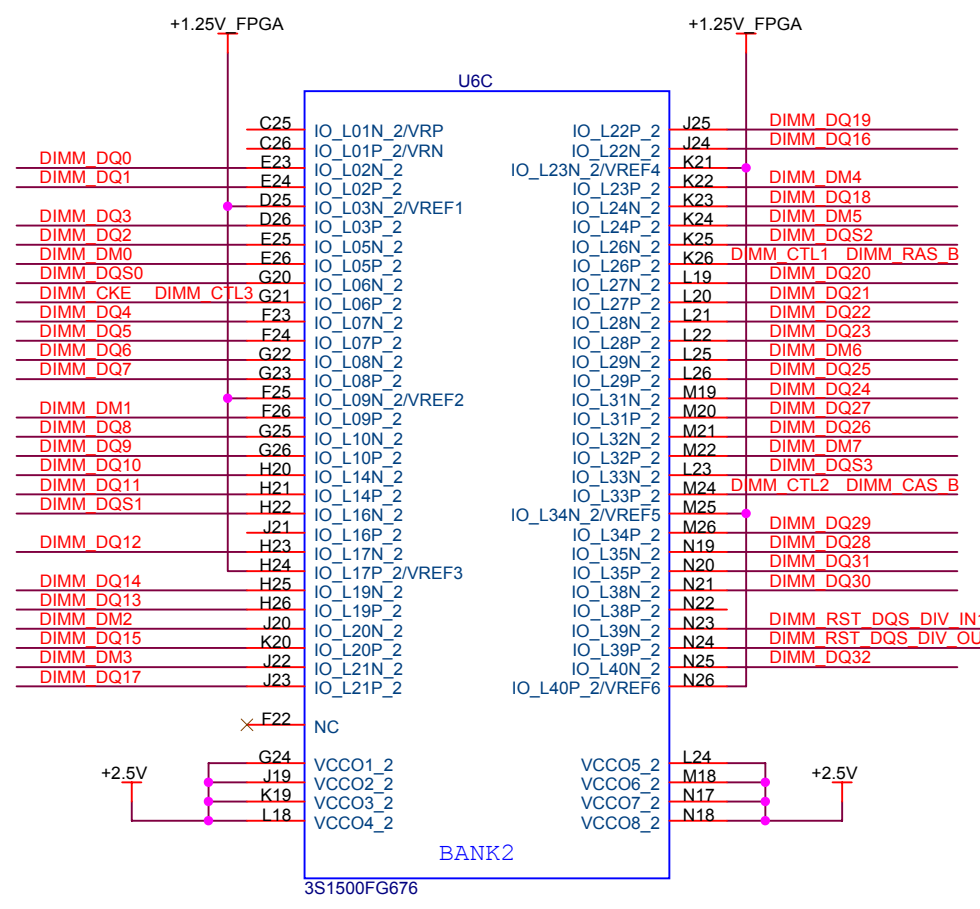
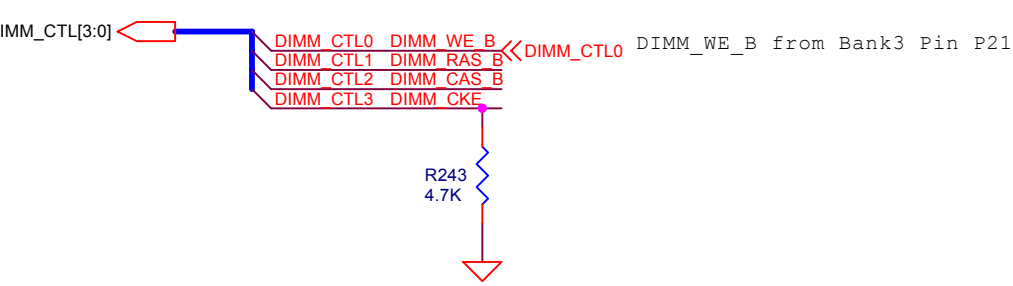
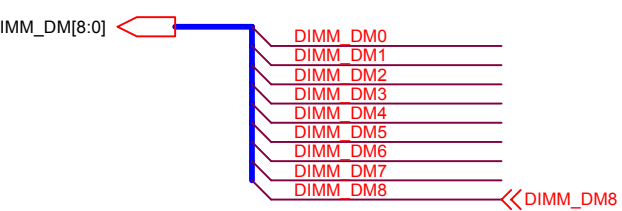
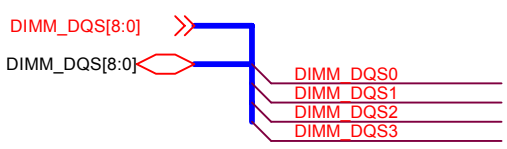
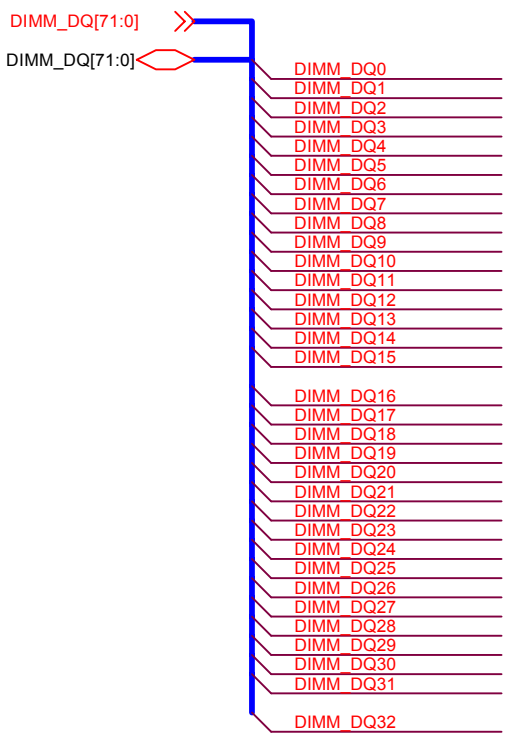
### DDR1 x 1 "Top" Interface

"Top" Memory DQS loop wire



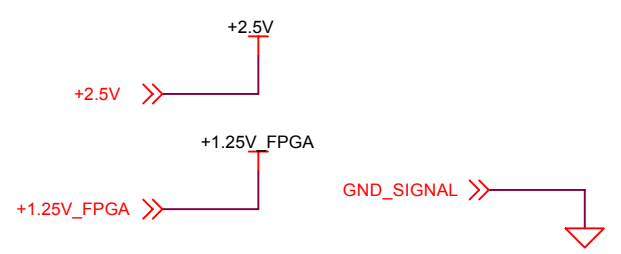
3S1500FG676 Bank1

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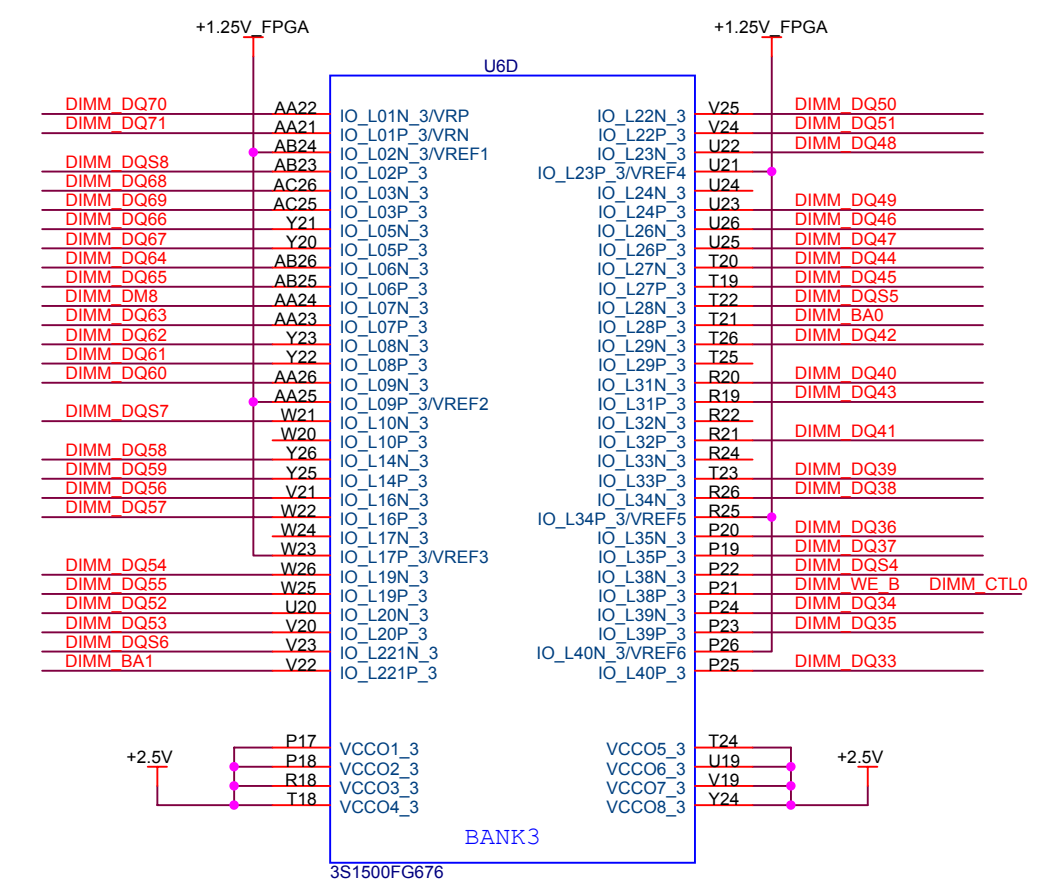
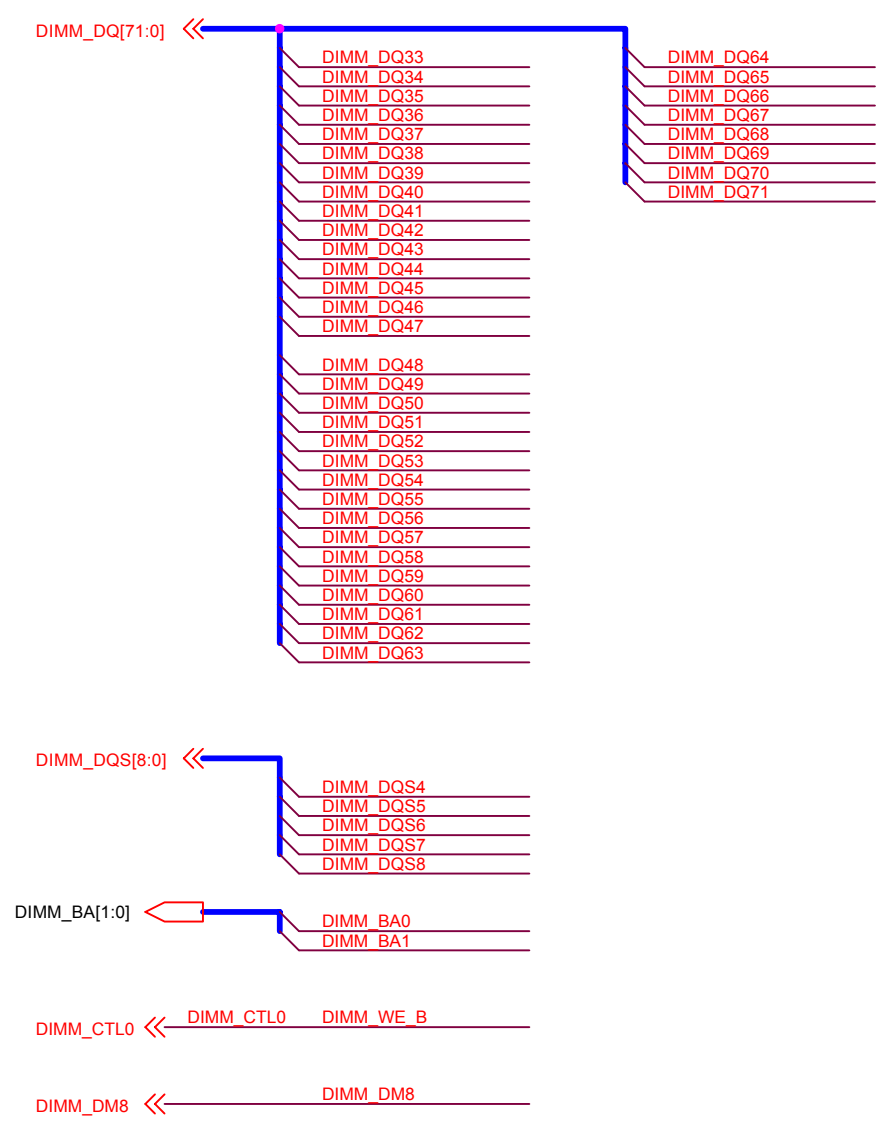
SODIMM DQS loop wire

### DDR1 SODIMM "Right" Side Interface

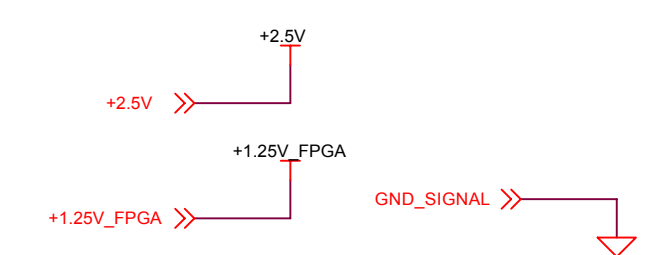


3S1500FG676 Bank2

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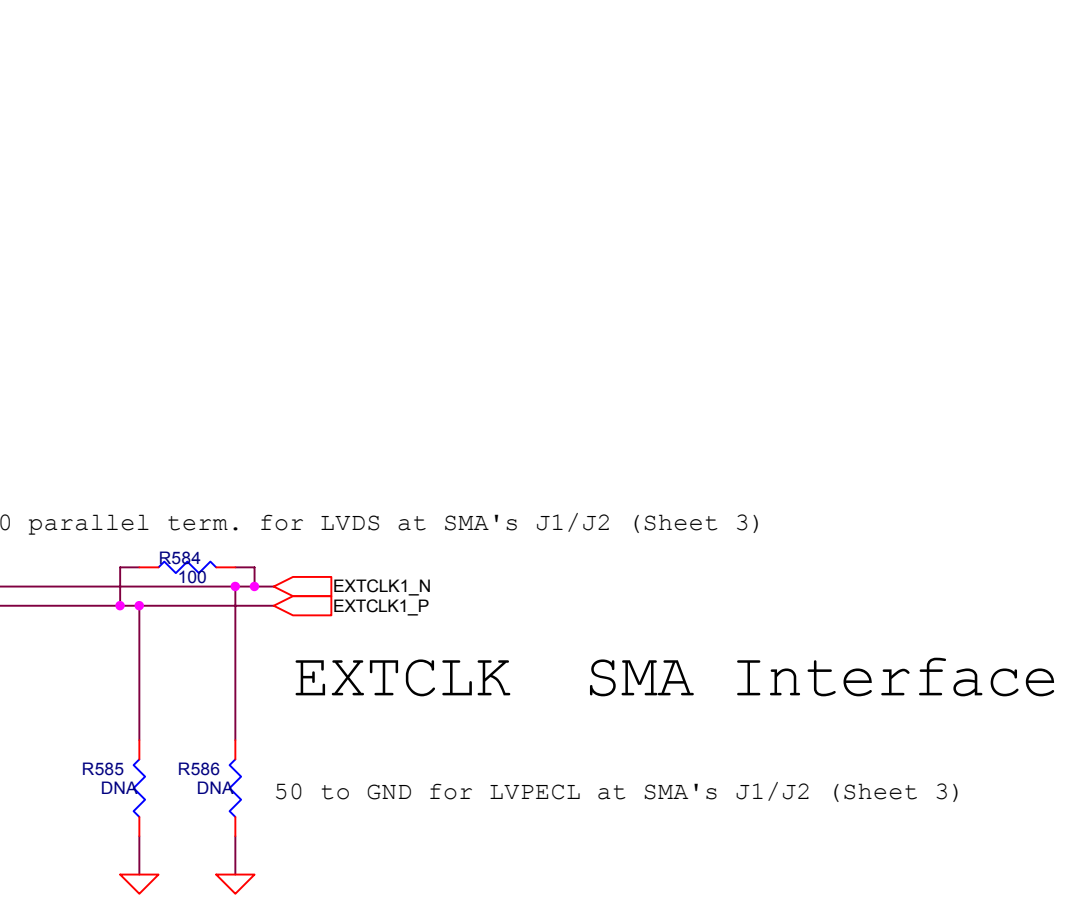
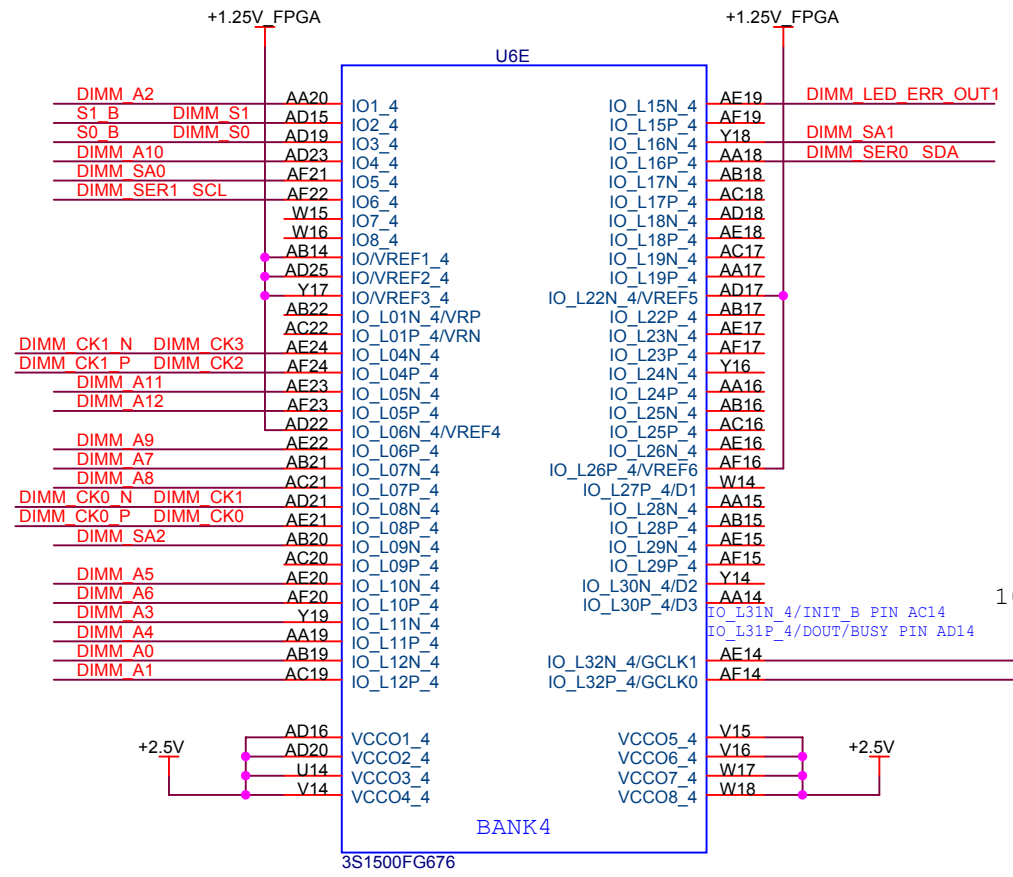
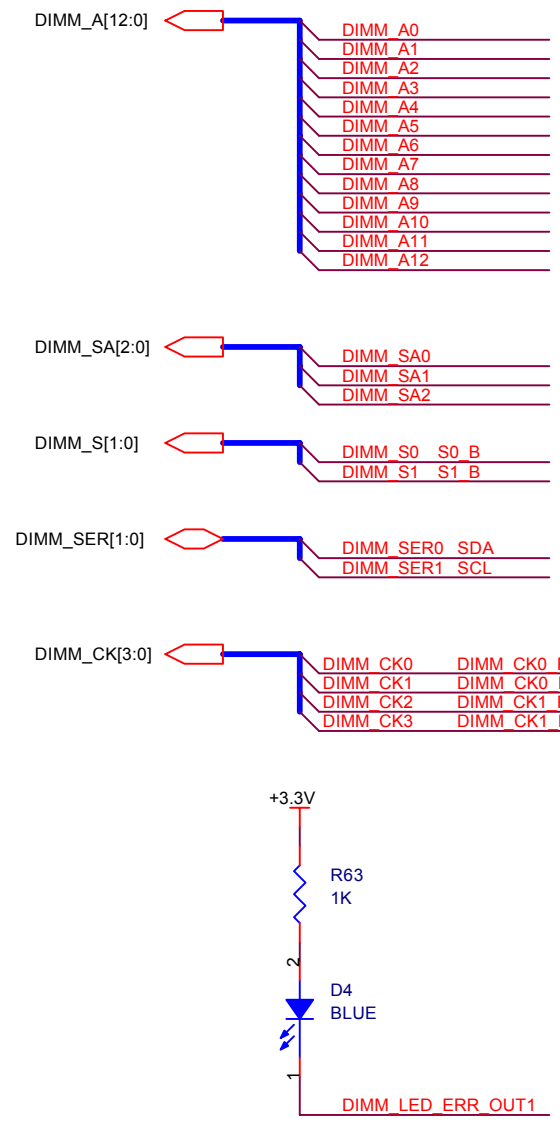
## DDR1 SODIMM "Right" Side Interface



3S1500FG676 Bank3

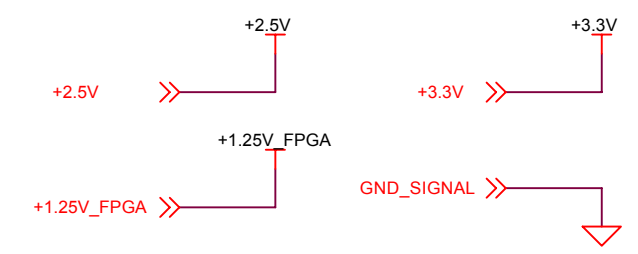
Title Spartan3 DDR-1 Board		
Size B	Document Number 0381177	Rev 2
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# DDR1 SODIMM Interface



For single-ended LVCMOS oscillator at Y1, no term. R's here

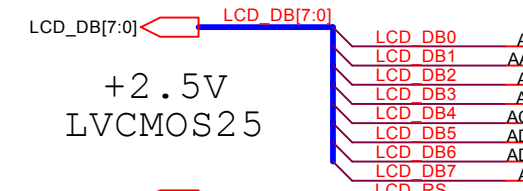
# DDR1 SODIMM "Right" Side Interface EXTCLK SMA Interface



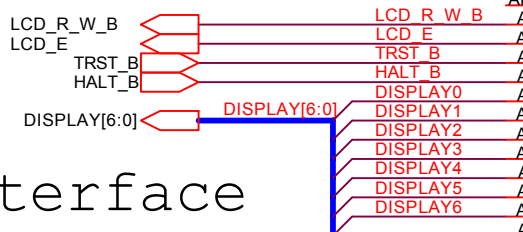
3S1500FG676 Bank4

Title Spartan3 DDR-1 Board		
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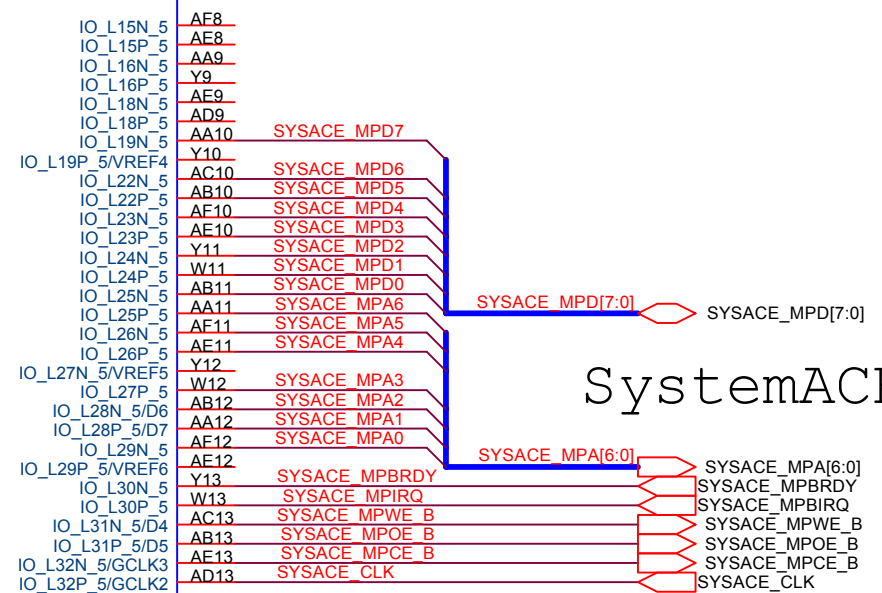
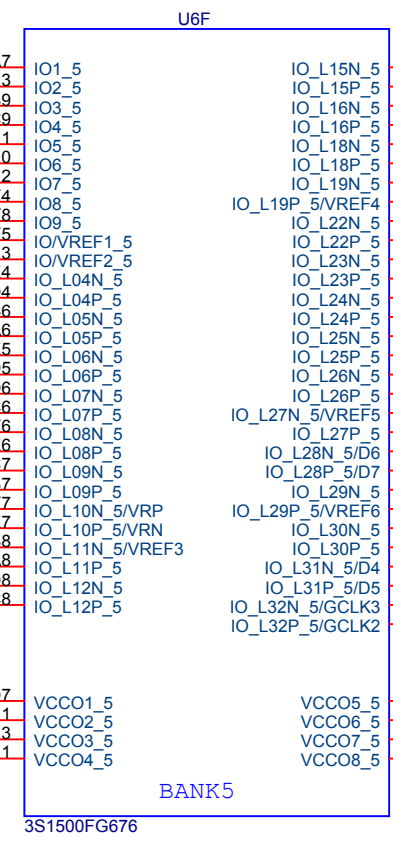
LCD Interface



7-Seg. Display Interface

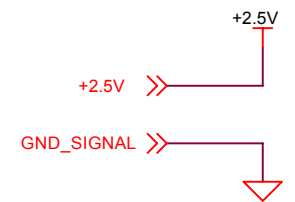


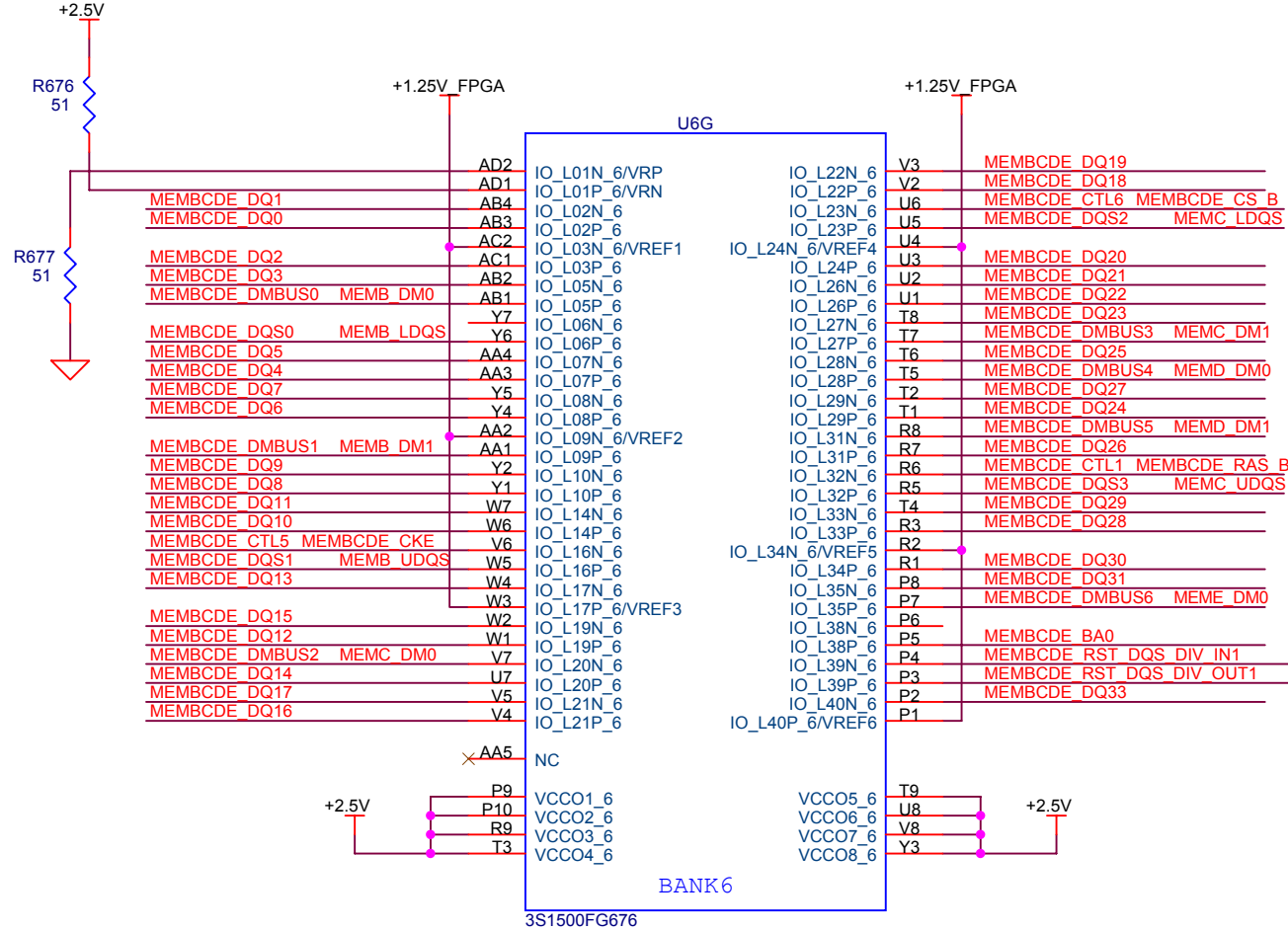
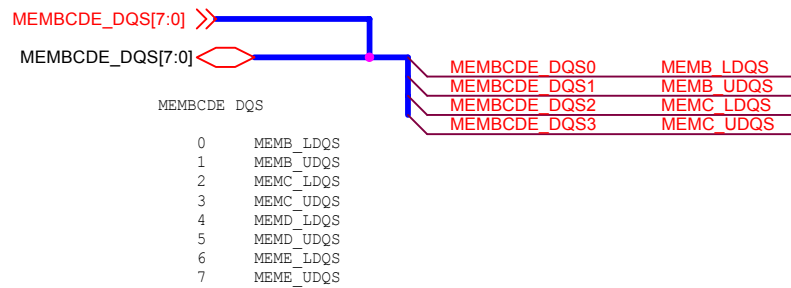
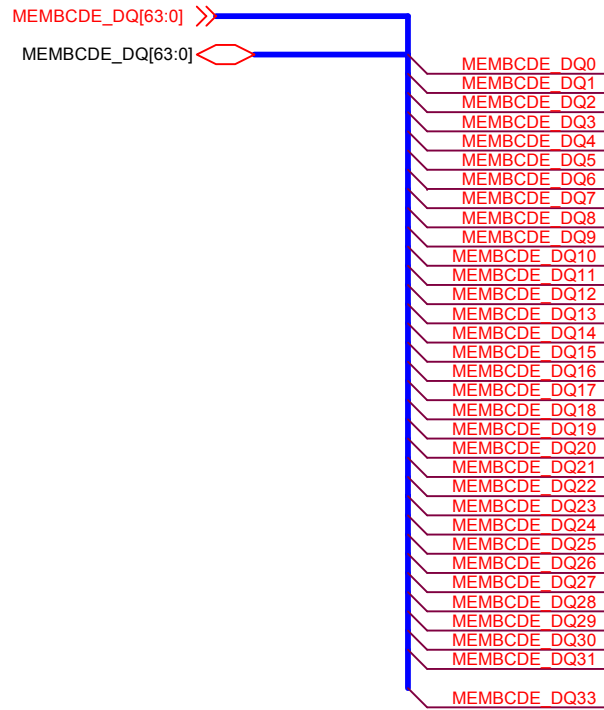
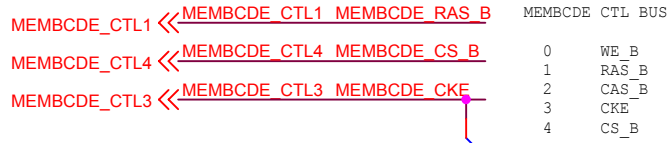
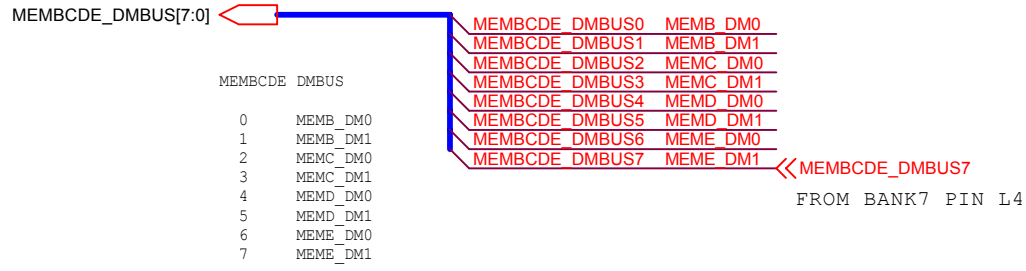
RS232 Interface



SystemACE Interface

LCD Interface  
 7-Seg. Display Interface  
 RS232 Interface  
 SystemACE Interface

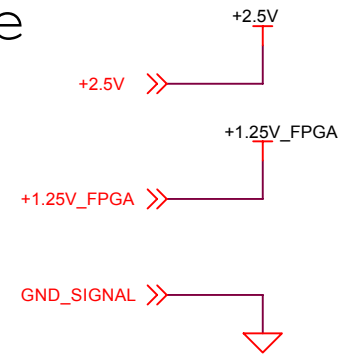




"Left" MEM BCDE DQS loop wire

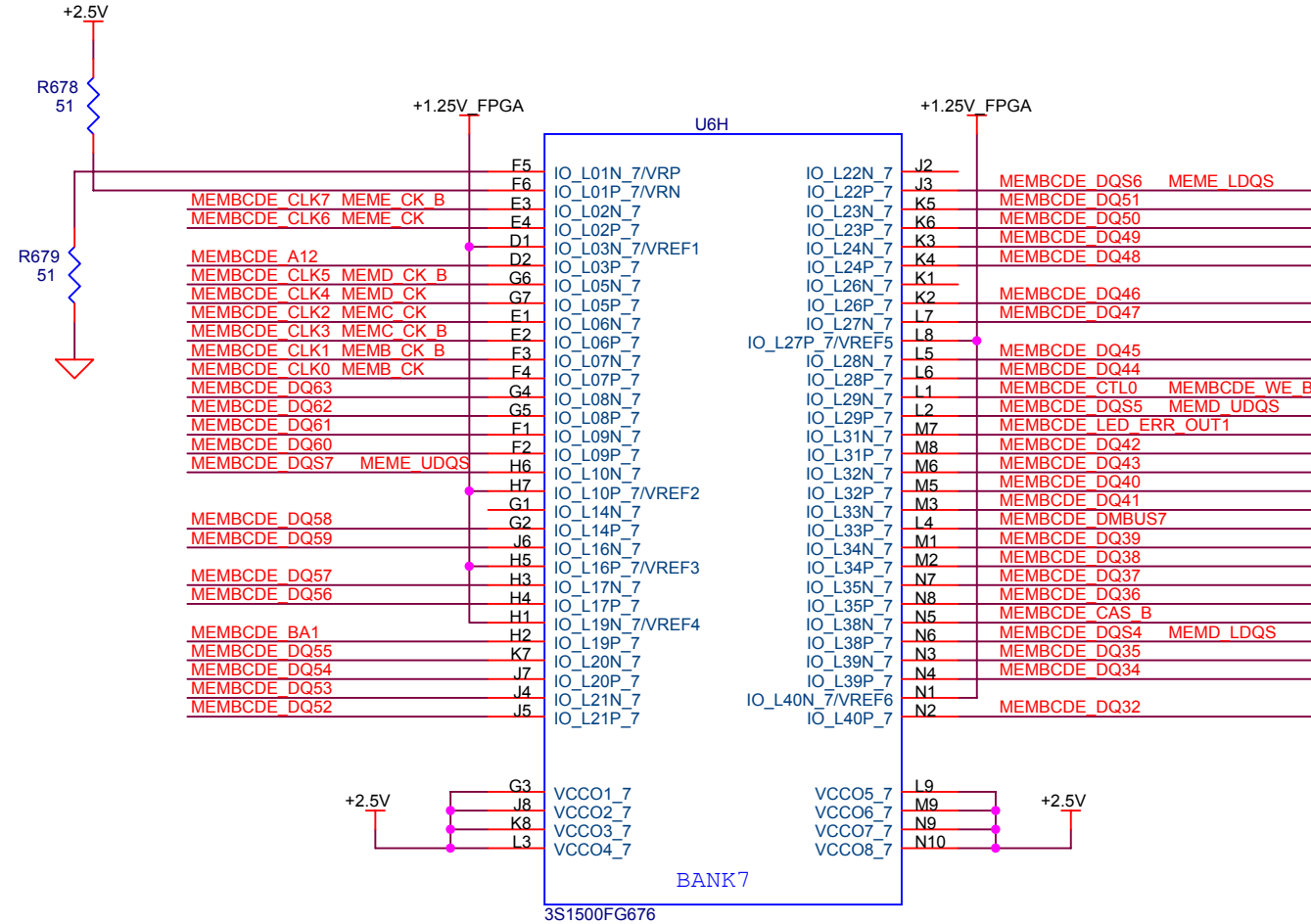
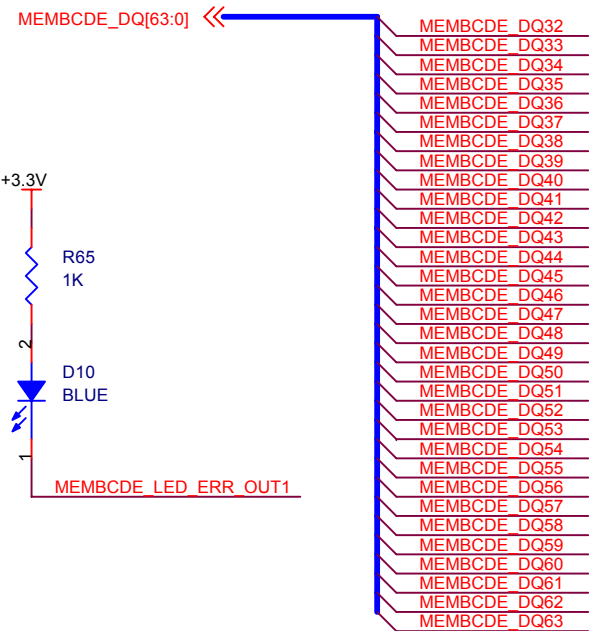
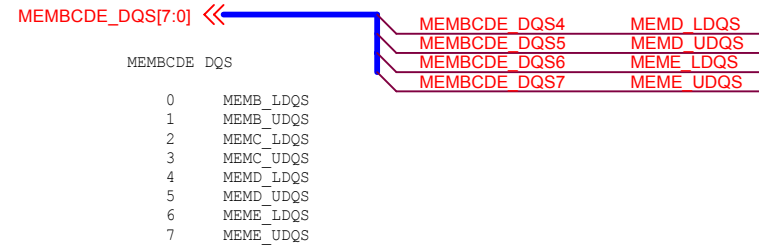
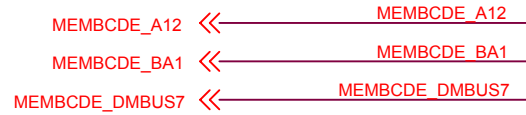
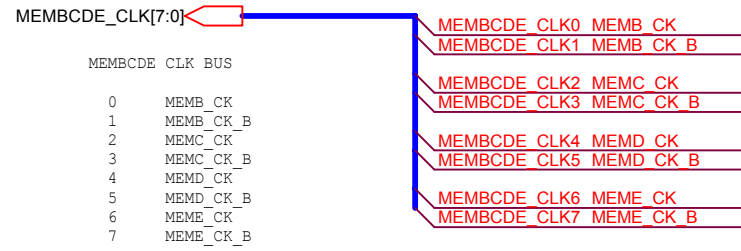
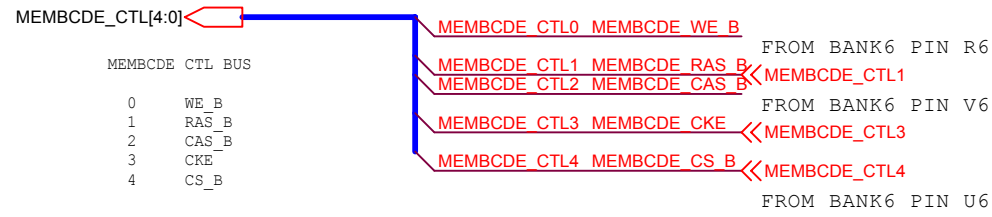
### DDR1 x4 (MEMB - MEME) "Left" Side Interface

4 x 16-bit DDR-1 Mem  
 on the Left are designated:  
 MEMB = MEM DQS (0:1)  
 MEMC = MEM DQS (2:3)  
 MEMD = MEM DQS (4:5)  
 MEME = MEM DQS (6:7)



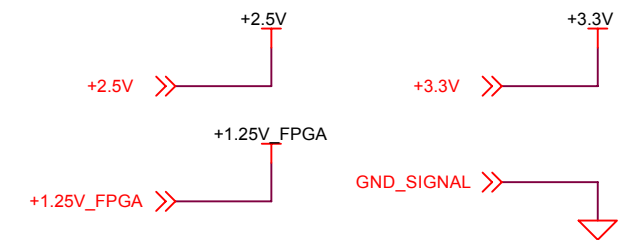
3S1500FG676 Bank6

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## DDR1 x4 (MEMB - MEME) "Left" Side Interface

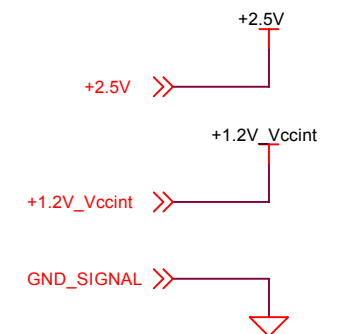
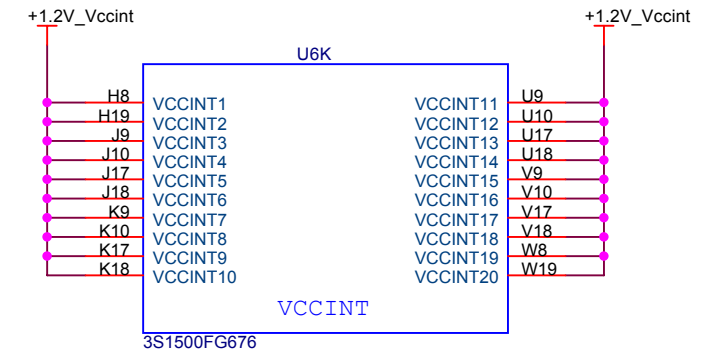
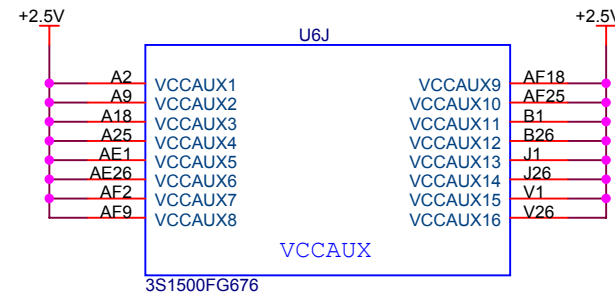
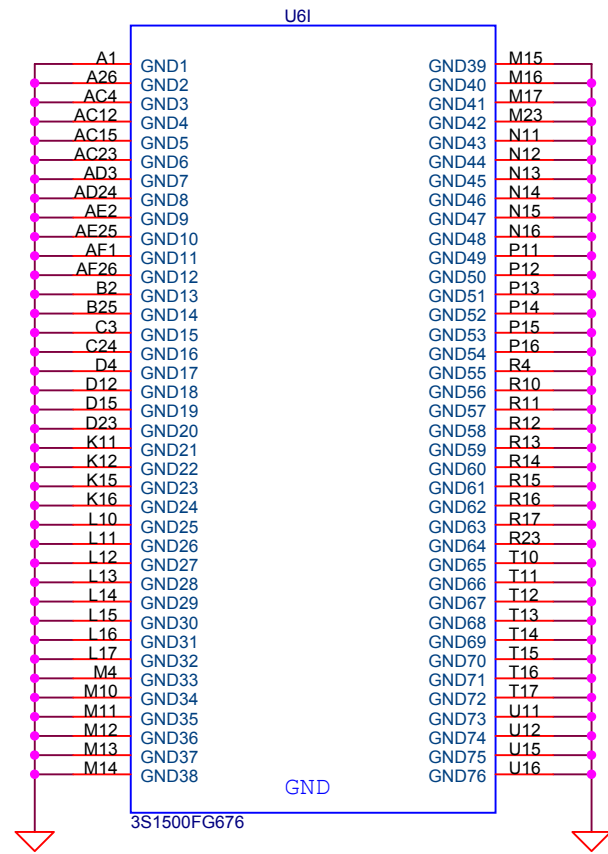
4 x 16-bit DDR-1 Mem  
on the Left are designated:  
MEMB = MEM DQS (0:1)  
MEMC = MEM DQS (2:3)  
MEMD = MEM DQS (4:5)  
MEME = MEM DQS (6:7)



3S1500FG676 Bank7

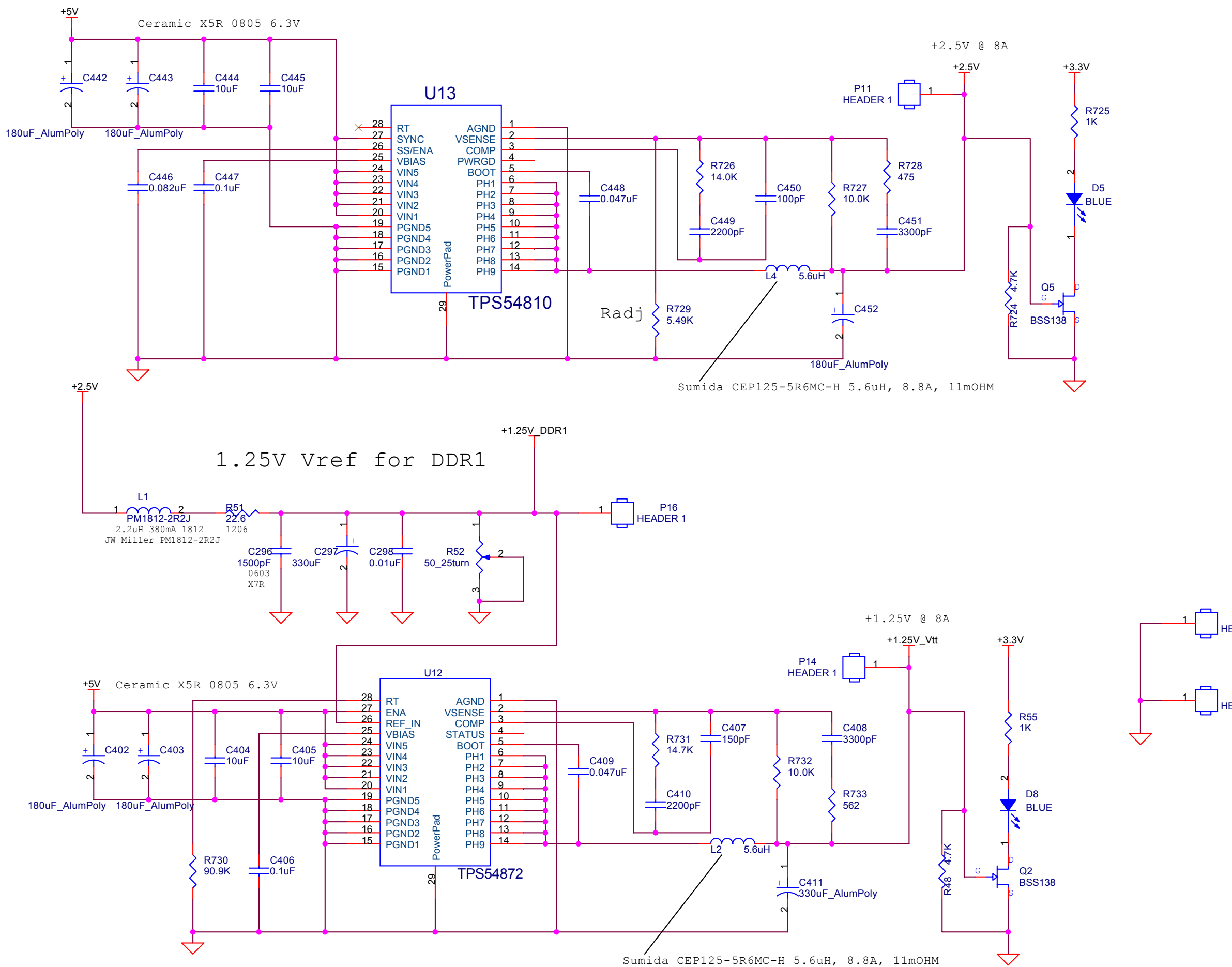
Title		
Spartan3 DDR-1 Board		
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3S1500FG676 GND, VCCAUX, VCCINT

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Spartan3 DDR-1 Board		
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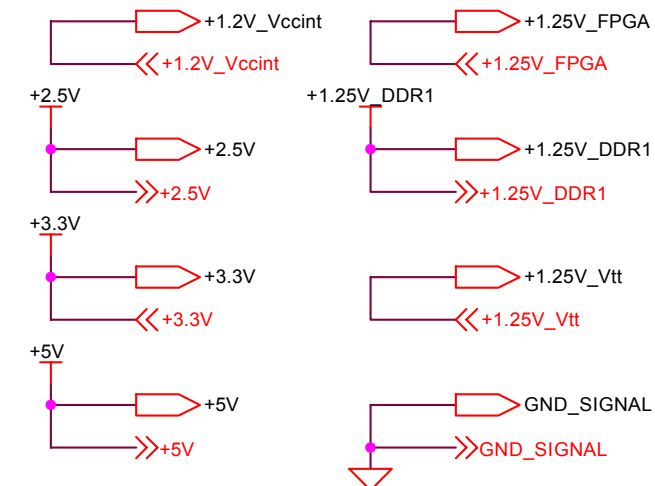


**Power Requirements:**

Item:	Purpose:	Voltage:	Current:
XC3S1500	Vccaux	2.5V	70mA (typ)
	Vcco	2.5V	1.68A (typ)
	Vccint	1.2V	1.52A (typ)
MT46V16M16	Vdd/Vddq	2.5V	2.2A (wc)
MT5VDDT1672	Vdd	2.5V	2.2A (wc)
Mem.Term.R's	Vtt	1.25V	8.1A (wc)
LEDs, Misc.	3.3V	3.3V	200mA (typ)

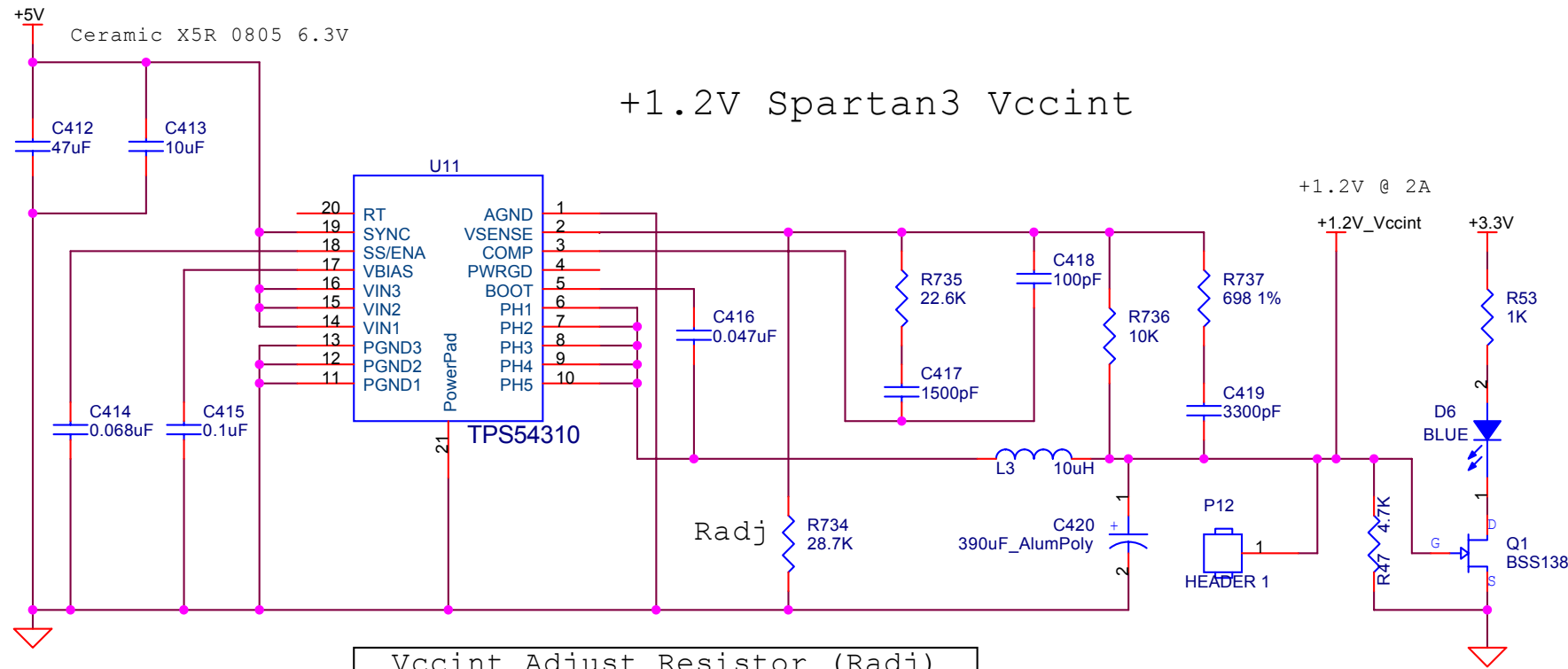
**2.5V Adjust Resistor (Radj)**

Vout		Std.1%R	Calc Vout
2.375V	-5%	6.04K	2.366V
2.500V	Nom	5.49K	2.514V
2.625V	+5%	5.11K	2.635V

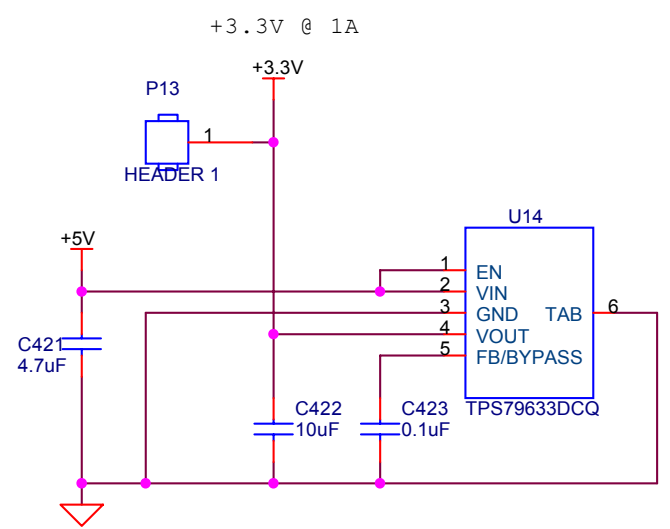


# LOCAL POWER REGULATION

Title		
Spartan3 DDR-1 Interface Board		
Size B	Document Number 0381177	Rev 2
Date:	Tuesday, March 15, 2005	Sheet 29 of 33

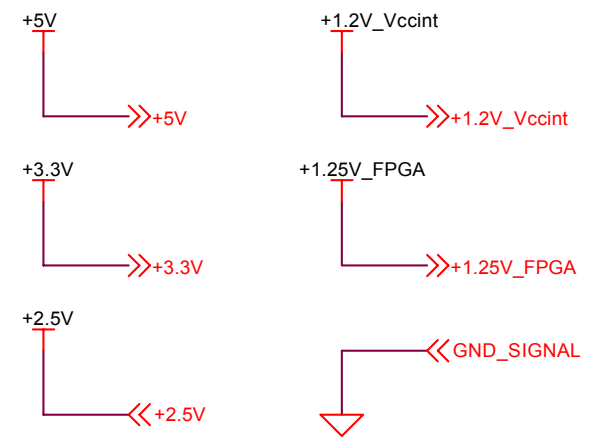
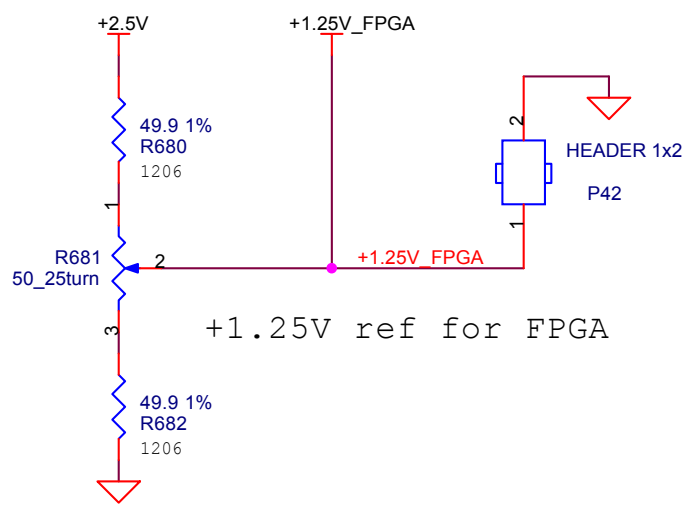
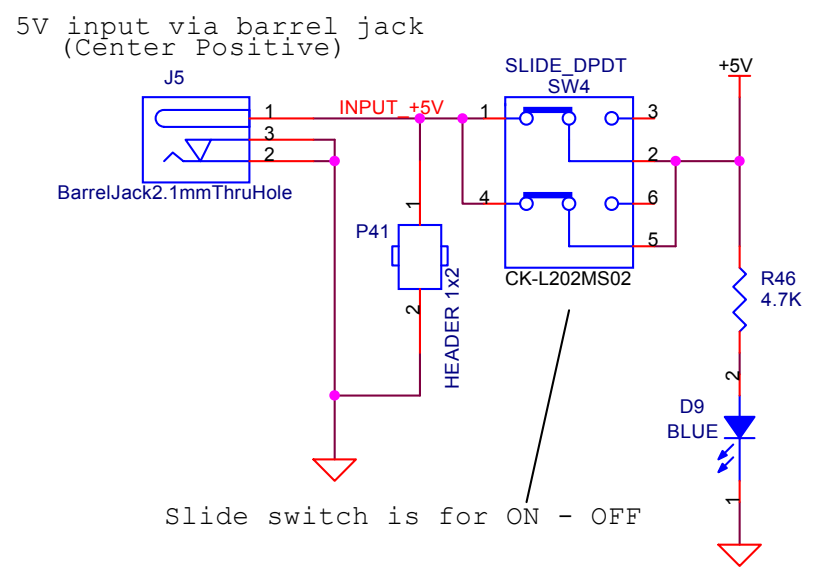


+3.3V (SysAce, LCD I/F, 7-Seg, LED's)



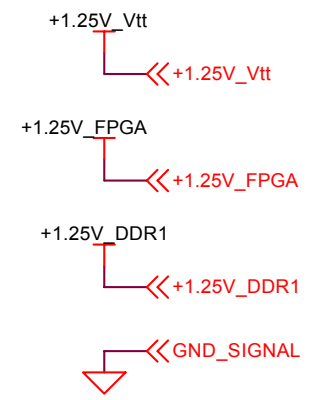
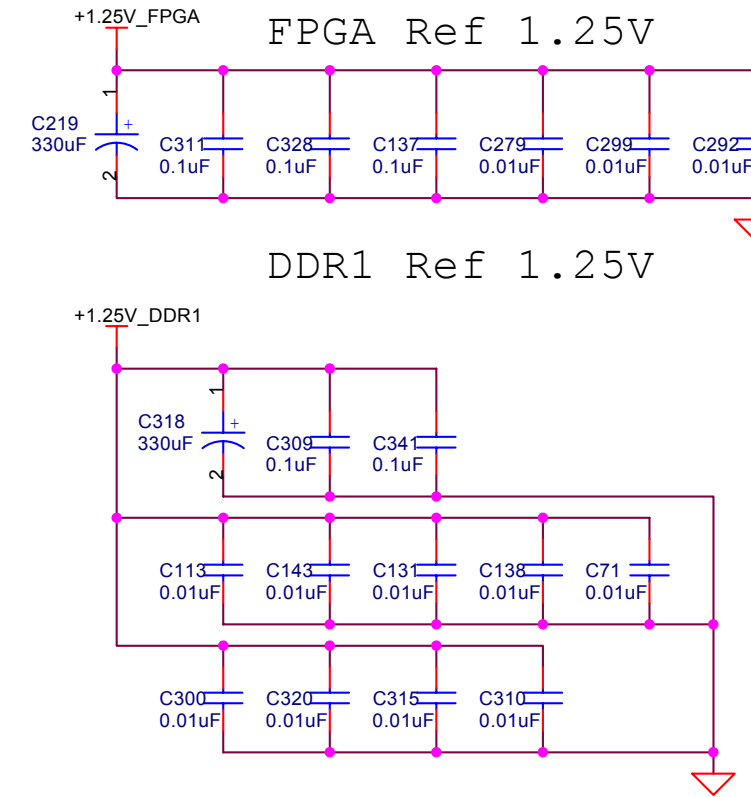
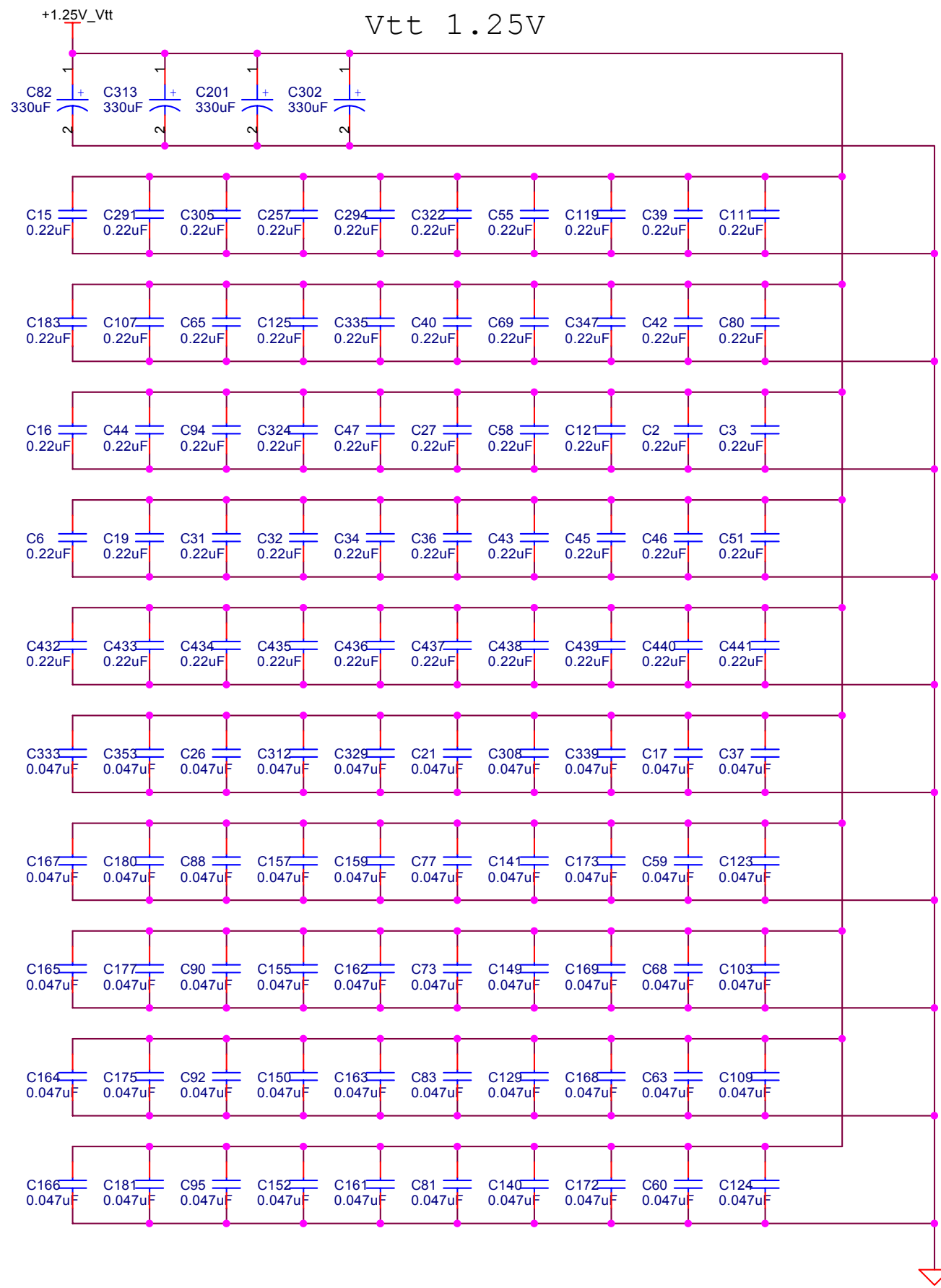
Vccint Adjust Resistor (Radj)

Vout		Std. 1%R	Calc Vout
1.140V	-5%	35.7K	1.141V
1.200V	Nom	28.7K	1.201V
1.260V	+5%	24.0K	1.262V



# LOCAL POWER REGULATION

Title Spartan3 DDR-1 Interface Board		
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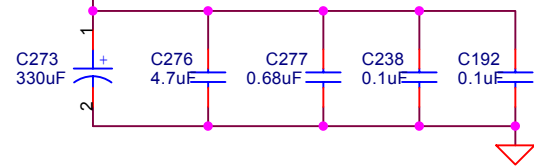


# DECOUPLING

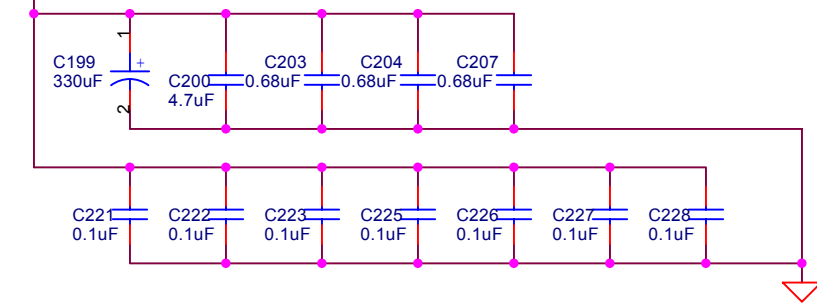
ALL non-Tantalum caps are X7R or X5R

Title Spartan3 DDR-1 Interface Board		
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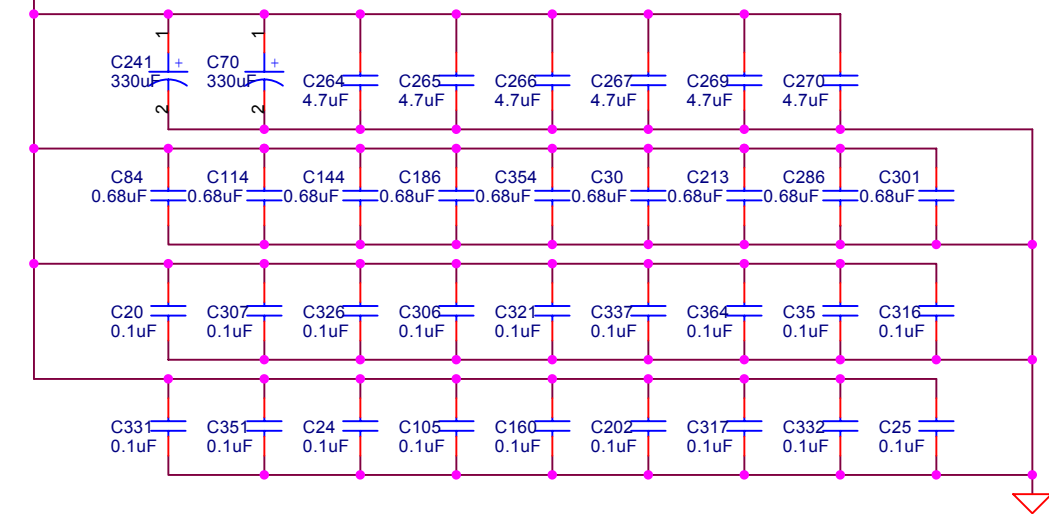
### +5V Power Input & LCD



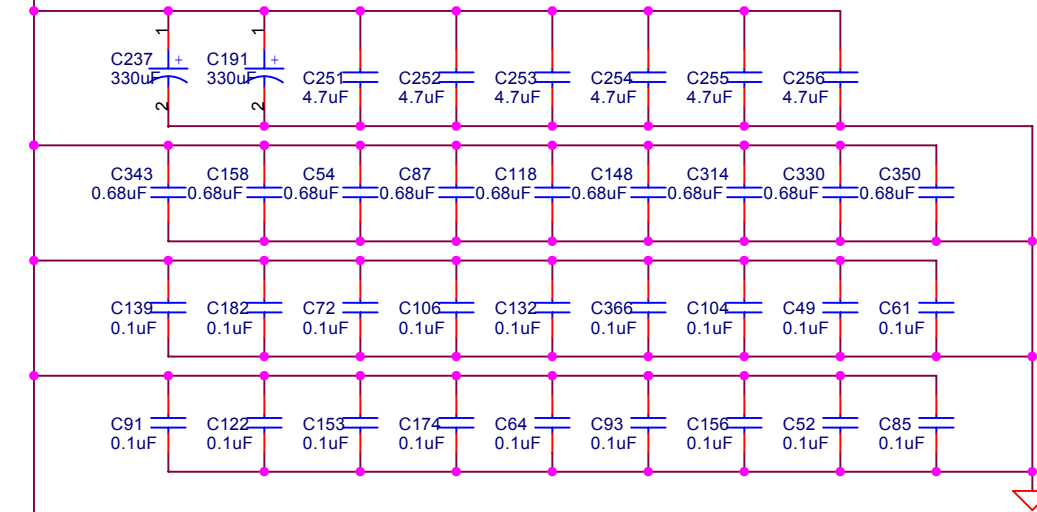
### +3.3V



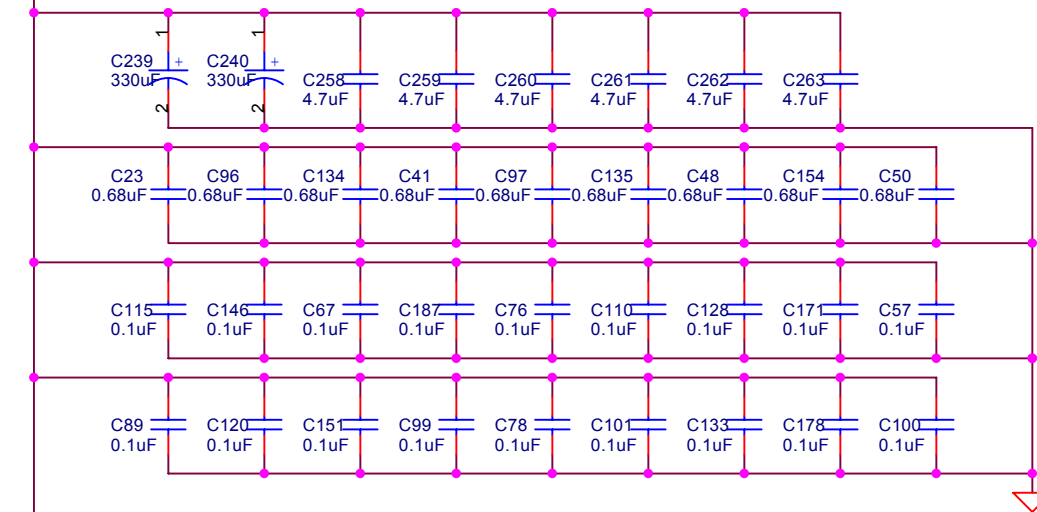
### Vccint 1.2V



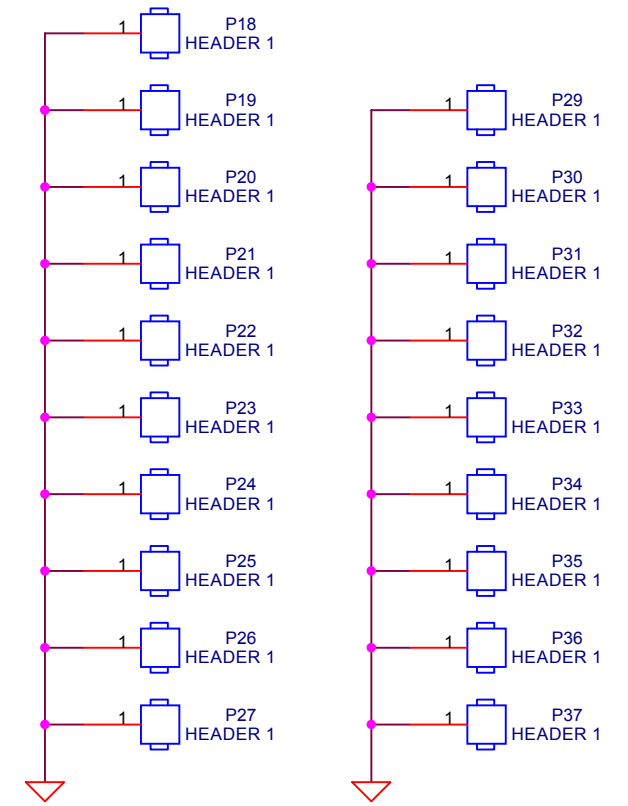
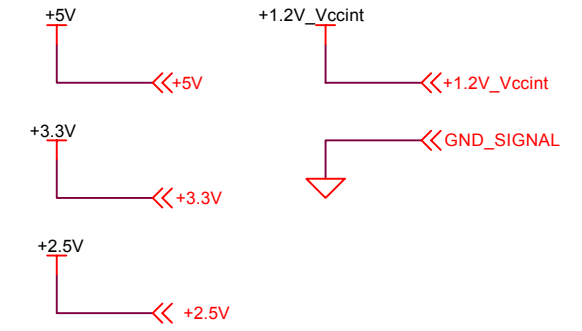
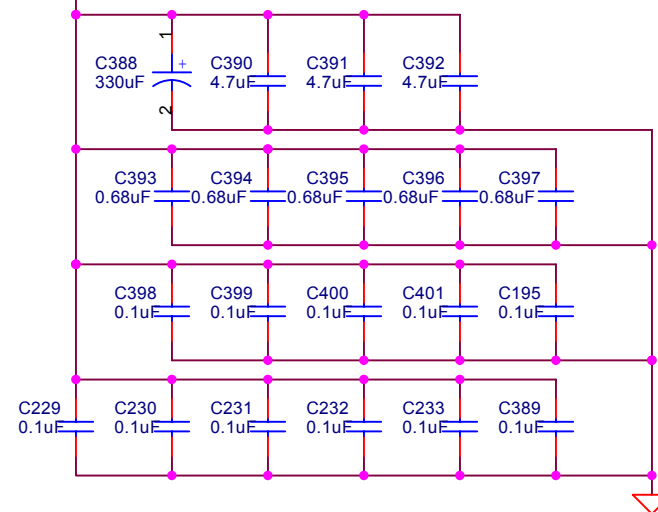
### System 2.5V



### Vcco 2.5V



### Vccaux 2.5V



# DECOUPLING

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Spartan3 DDR-1 Interface Board		
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Rev# Sheet# Description

- 0 All Initial Release
- 1 2 Changed bus widths DIMM\_DQ, DIMM\_DQS, DIMM\_DM
- 15 Changed bus widths DIMM\_DQ, DIMM\_DQS, DIMM\_DM
- 16 Changed bus widths DIMM\_DQ, DIMM\_DQS, DIMM\_DM
- 21 Changed bus widths DIMM\_DQ, DIMM\_DQS, DIMM\_DM
- 22 Changed bus widths DIMM\_DQ, DIMM\_DQS, DIMM\_DM
- 2 Misc Updates resulting from schematic review
- 3 Misc Replaced discrete 0402 50 ohm memory bus term R's with Rpaks
- 15 Added 0 ohm R738 connecting DIMM\_CKE0 to CKE1 pin
- 4 27 Correct wiring error: TCK and TMS were swapped
- 5 30 Change R values to 50 ohms: R680,R681(trimpot),R682
- 6 32 Delete GND test pin P28

Rev Notes

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Spartan3 DDR-1 Interface Board		
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