



XILINX

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AC701 Built-In Self Test Flash Application

December 2013

XTP194

Revision History

Date	Version	Description
12/18/13	6.0	Recompiled for 2013.4.
10/23/13	5.0	Recompiled for 2013.3. Converted to IPI, added RGMII interface and LwIP.
06/19/13	4.0	Recompiled for 2013.2. AR55431, AR55531 and AR55738 fixed.
04/03/13	3.0	Recompiled for 2013.1. Added AR55431, AR55531 and AR55738. AR53420 Fixed.
02/04/13	2.1	As per AR54044, added 2012.4 device pack. Added AR53420 and AR54223.
12/18/12	2.0	Recompiled for 2012.4
10/23/12	1.0	Initial Version.

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Overview

- **Xilinx AC701 Board**
- **Software Requirements**
- **AC701 Setup**
- **AC701 BIST (Built-In Self Test)**
- **Compile AC701 BIST Design**
- **Program AC701 with BIST Design**
- **Run the LwIP Ethernet Design**
- **References**
 - IP Release Notes Guide [XTP025](#)

AC701 BIST Design Description

➤ Description

- The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

➤ Block Design Source

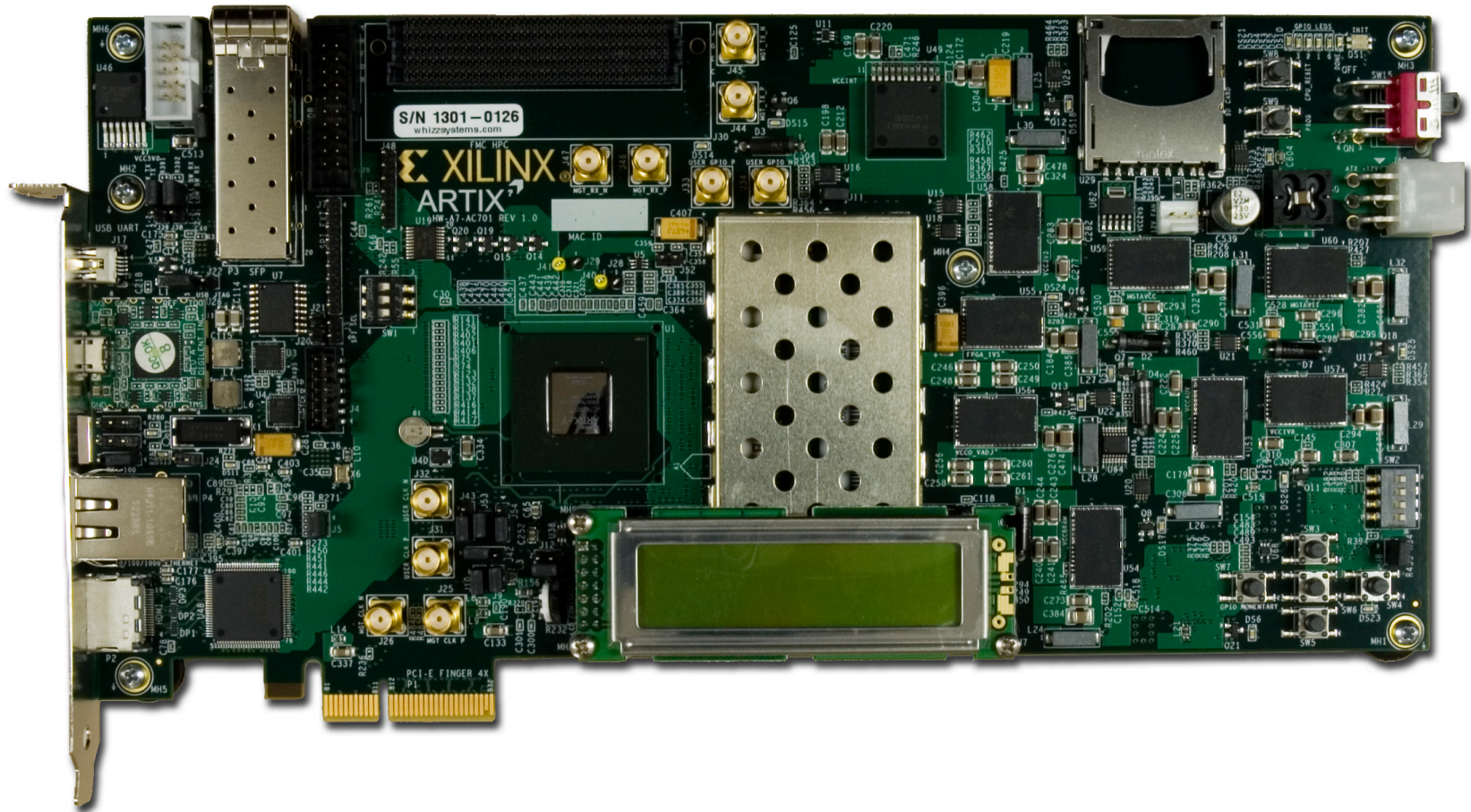
- RDF0220 - AC701 BIST Design Files (2013.4 C) zip file
- Available through <http://www.xilinx.com/ac701>

AC701 BIST Design Description

➤ Block Design IP

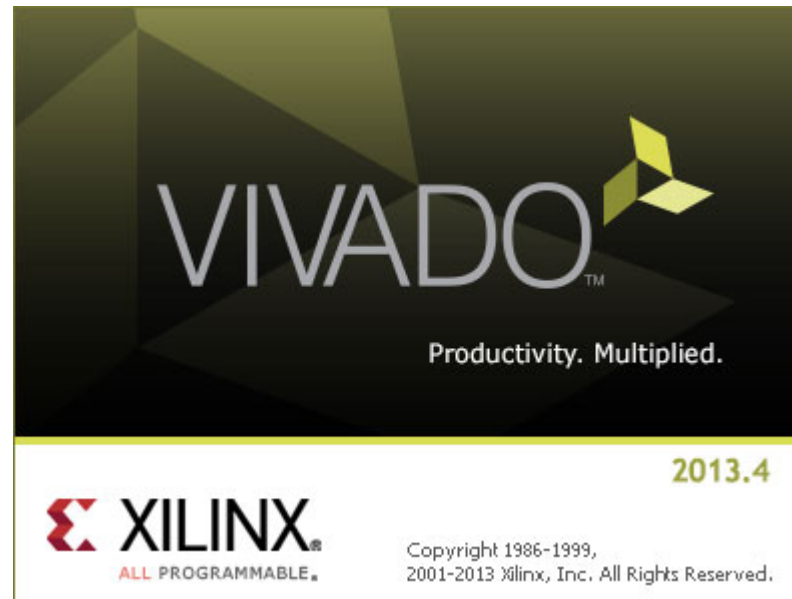
- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus, LMB BRAM Controller, Block Memory Generator, Proc Sys Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect, AXI Timer
- Memory: AXI BRAM Controller, MIG 7 Series, AXI DMA
- Peripherals: AXI Ethernet, AXI IIC, AXI GPIO, AXI UART 16550, XADC Wizard
- Other IP: Clocking Wizard, Constant, Concat, gte2_top
 - [Vivado Design Suite Tcl Command Reference Guide](#) (UG835)
 - [Designing IP Subsystems Using IP Integrator](#) (UG994)

Xilinx AC701 Board



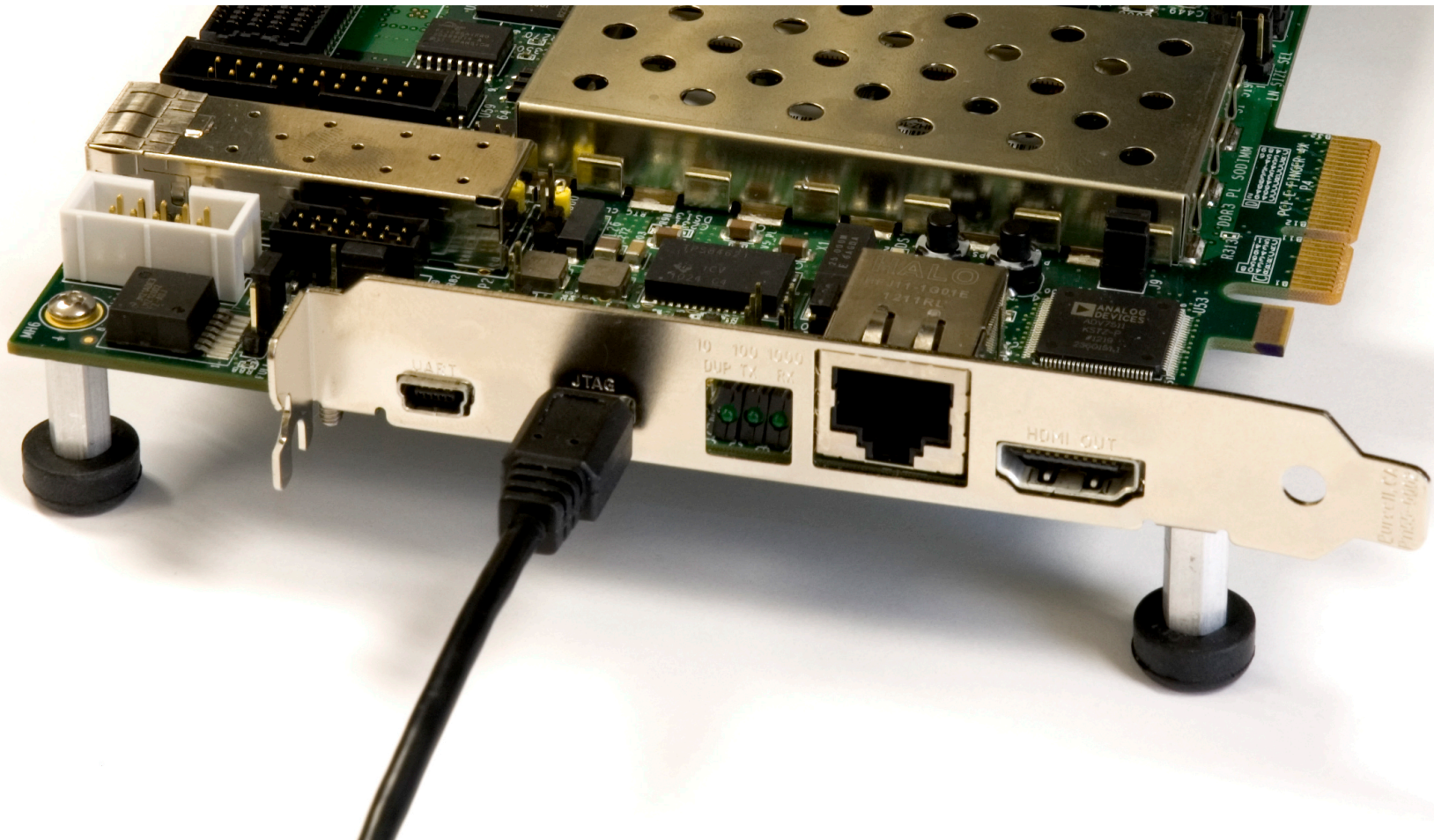
Vivado Software Requirements

- Xilinx Vivado Design Suite 2013.4, Design Edition + SDK
 - Combined installer



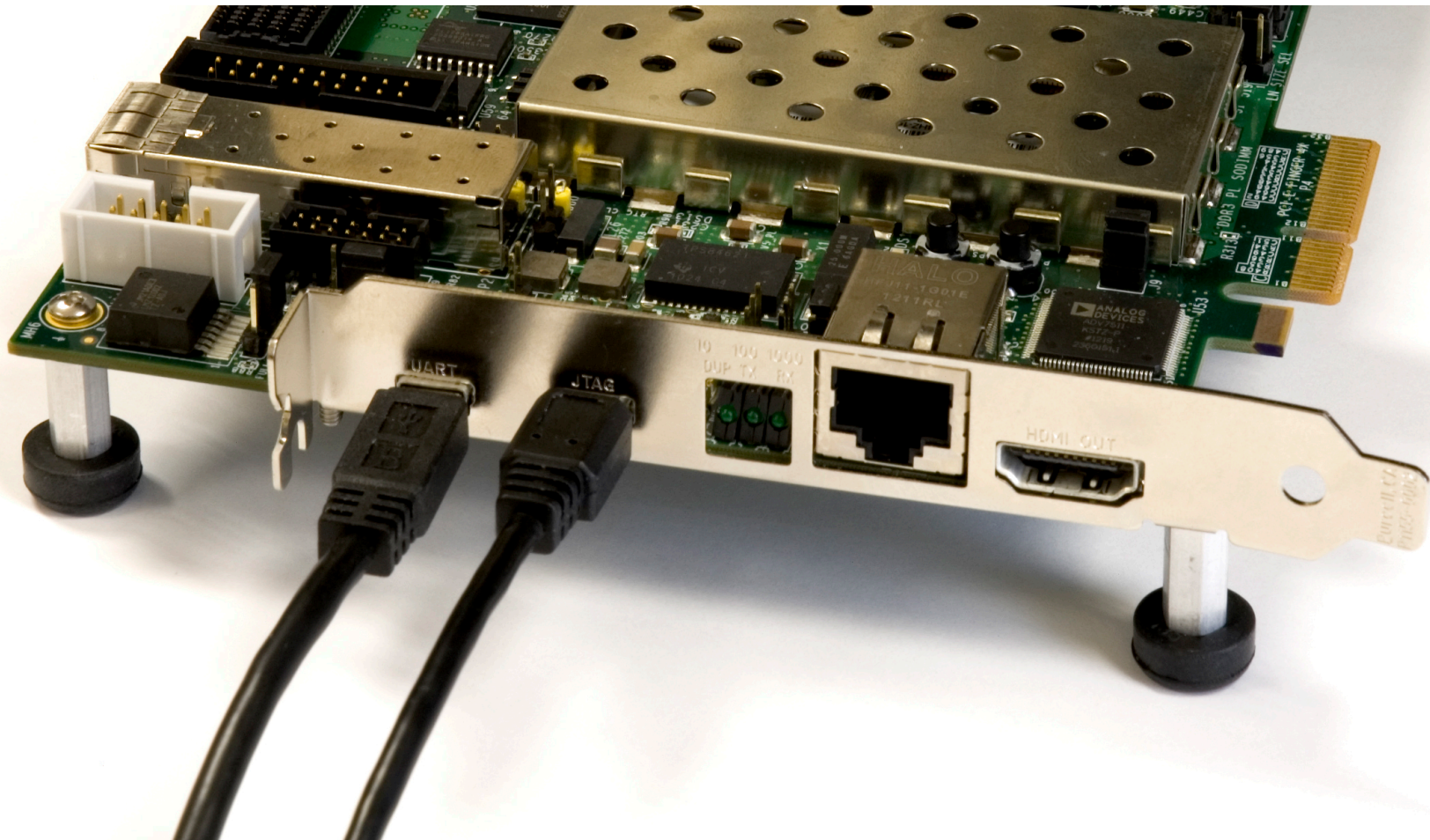
AC701 Setup

- Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board
 - Connect this cable to your PC



AC701 Setup

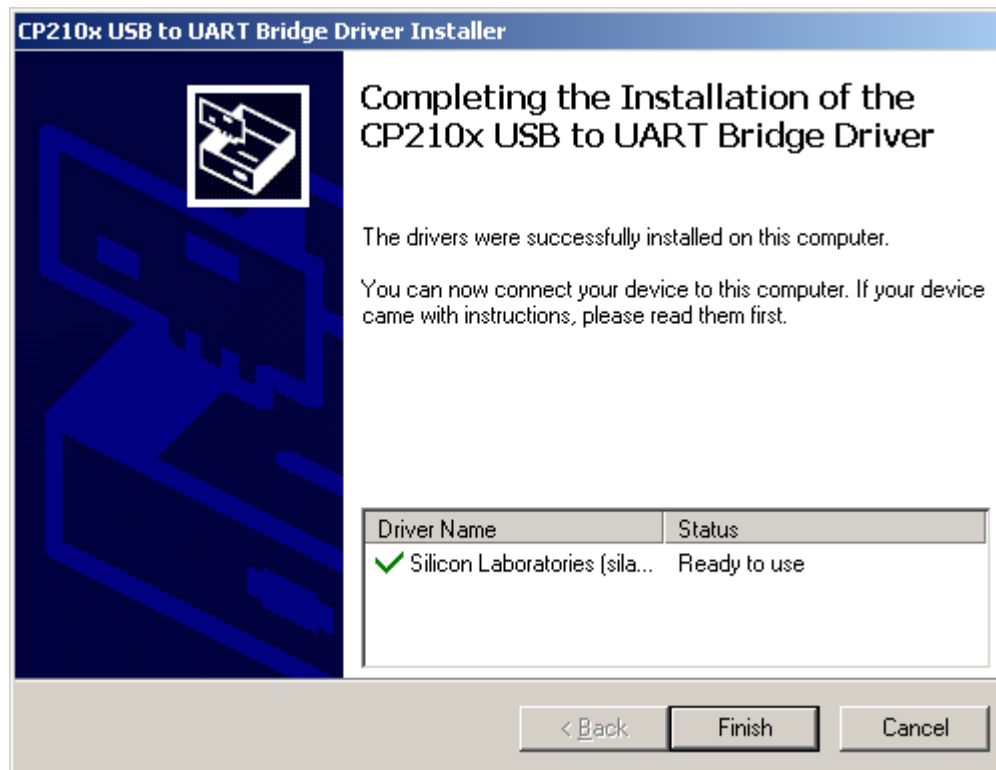
- Connect a USB Type-A to Mini-B cable to the USB UART connector on the AC701 board
 - Connect this cable to your PC
 - Power on the AC701 board for UART Drivers Installation



AC701 Setup

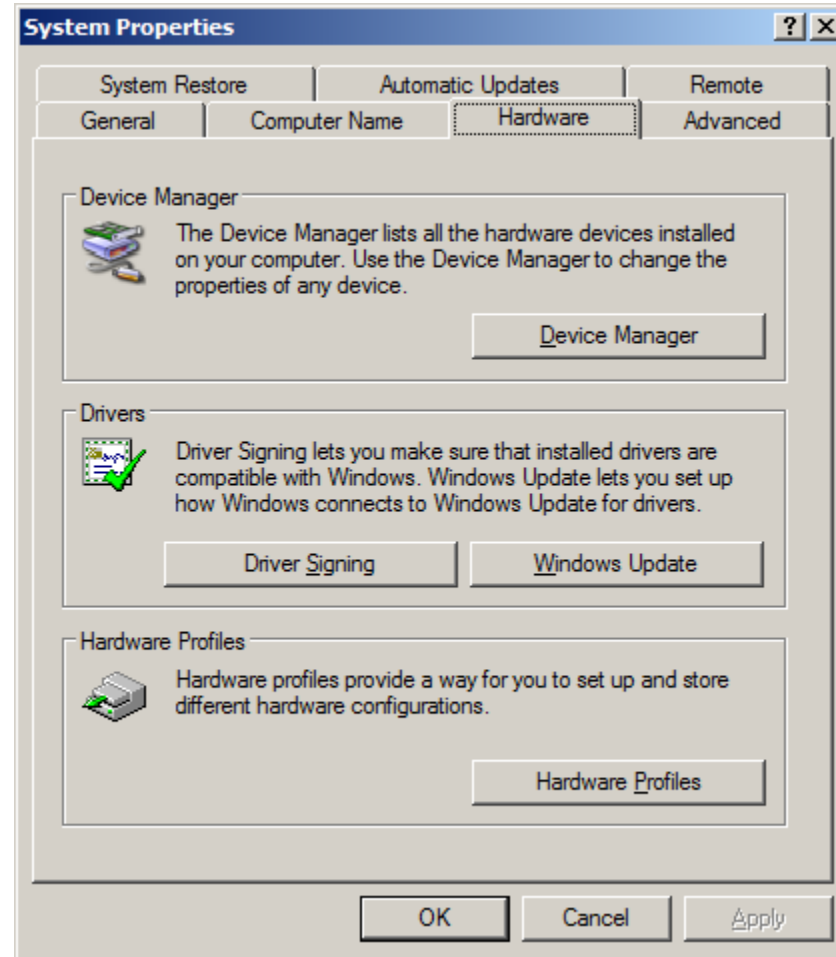
➤ Install USB UART Drivers

- Go to <http://www.silabs.com>
- Search for Virtual port drivers



AC701 Setup

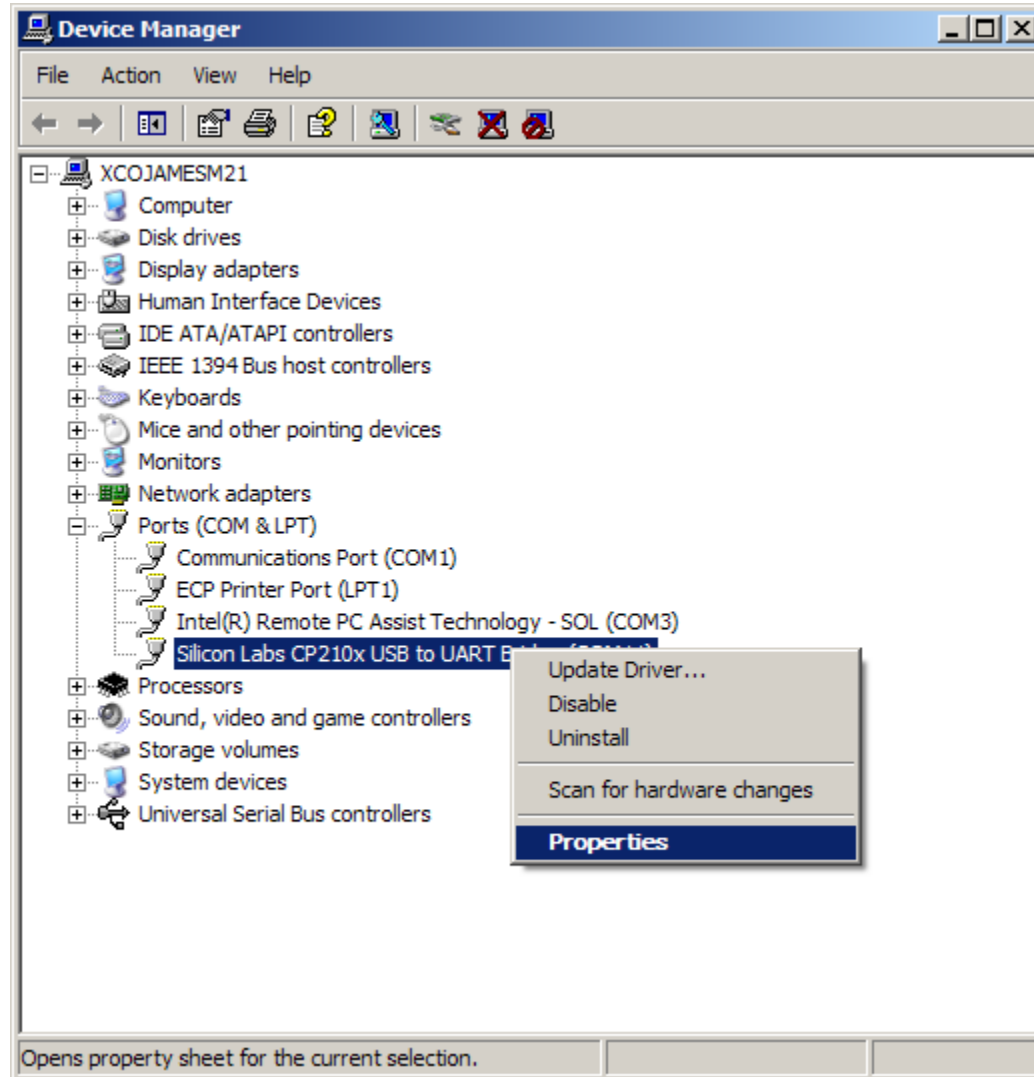
- Reboot your PC if necessary
- Right-click on My Computer and select Properties
 - Select the Hardware tab
 - Click on Device Manager



AC701 Setup

➤ Expand the Ports Hardware

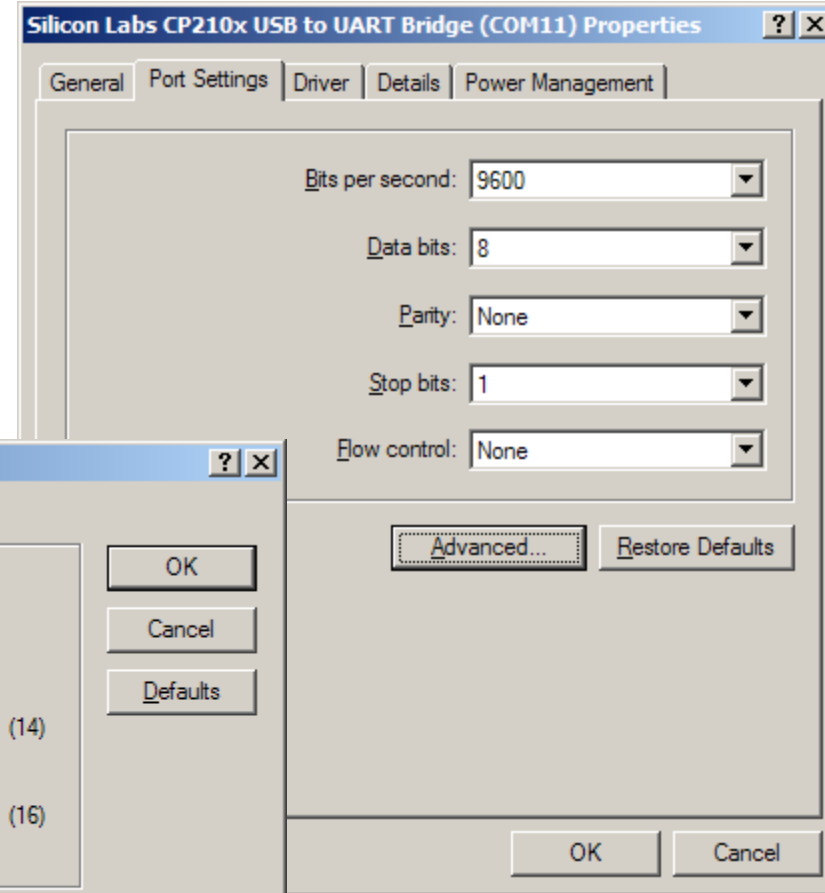
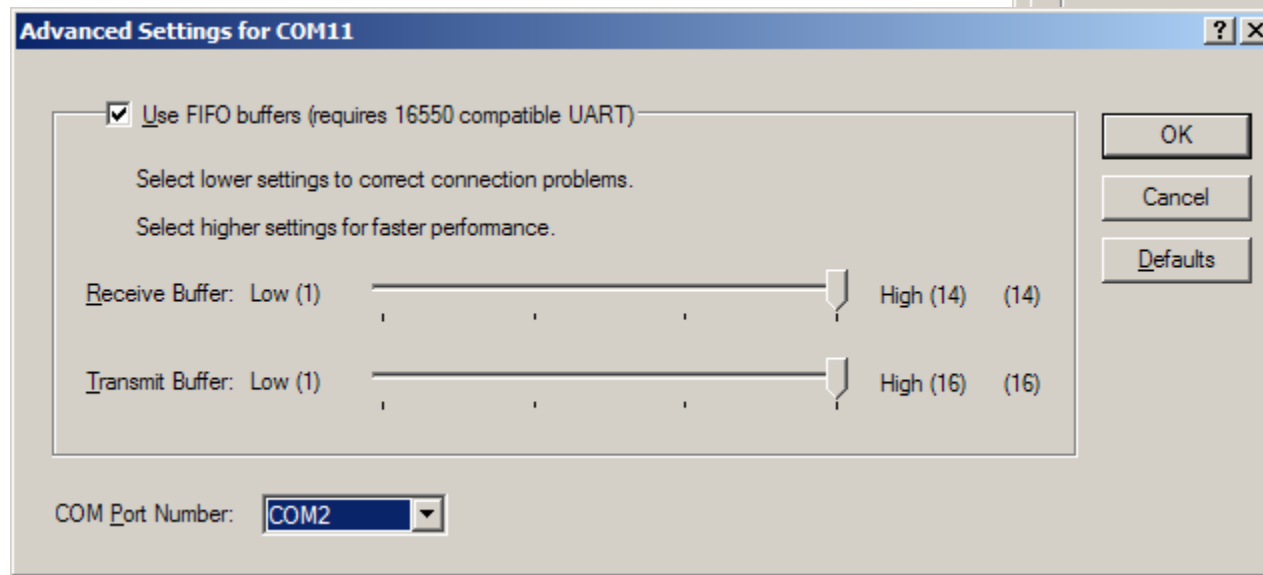
- Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties



AC701 Setup

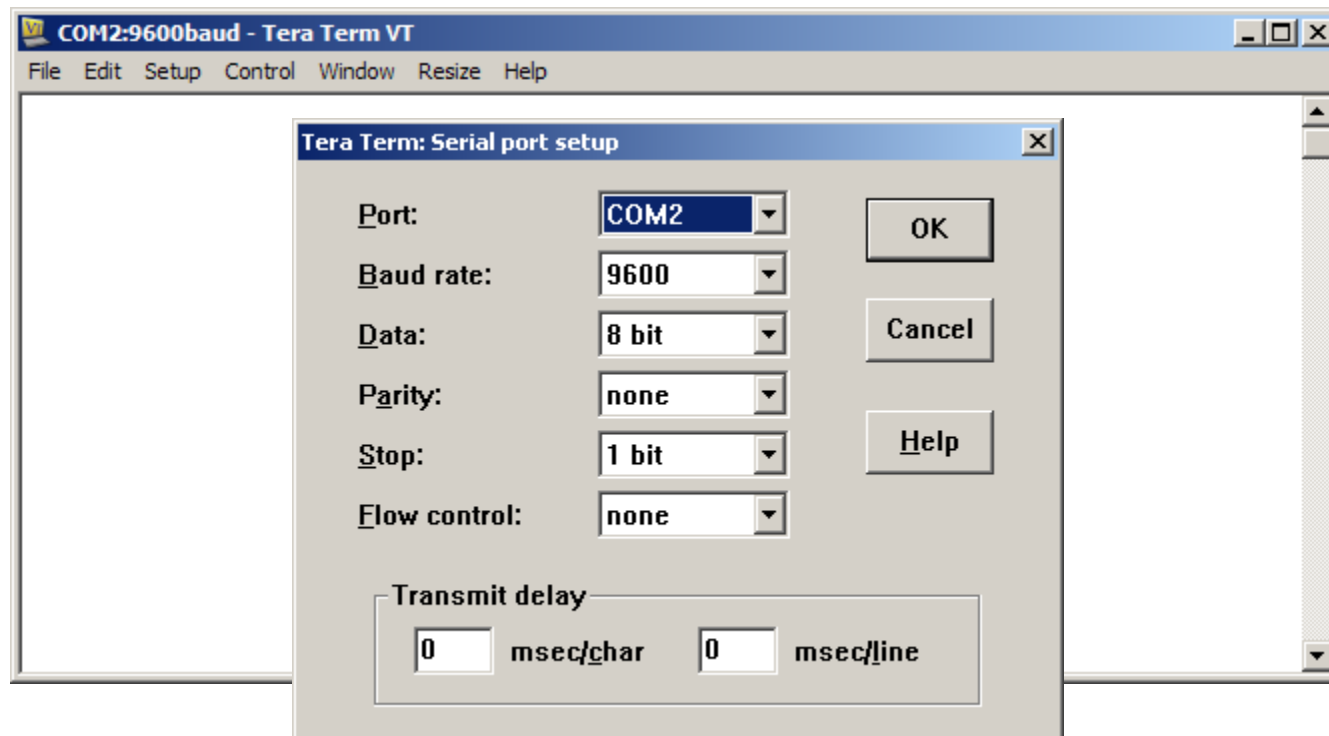
► Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



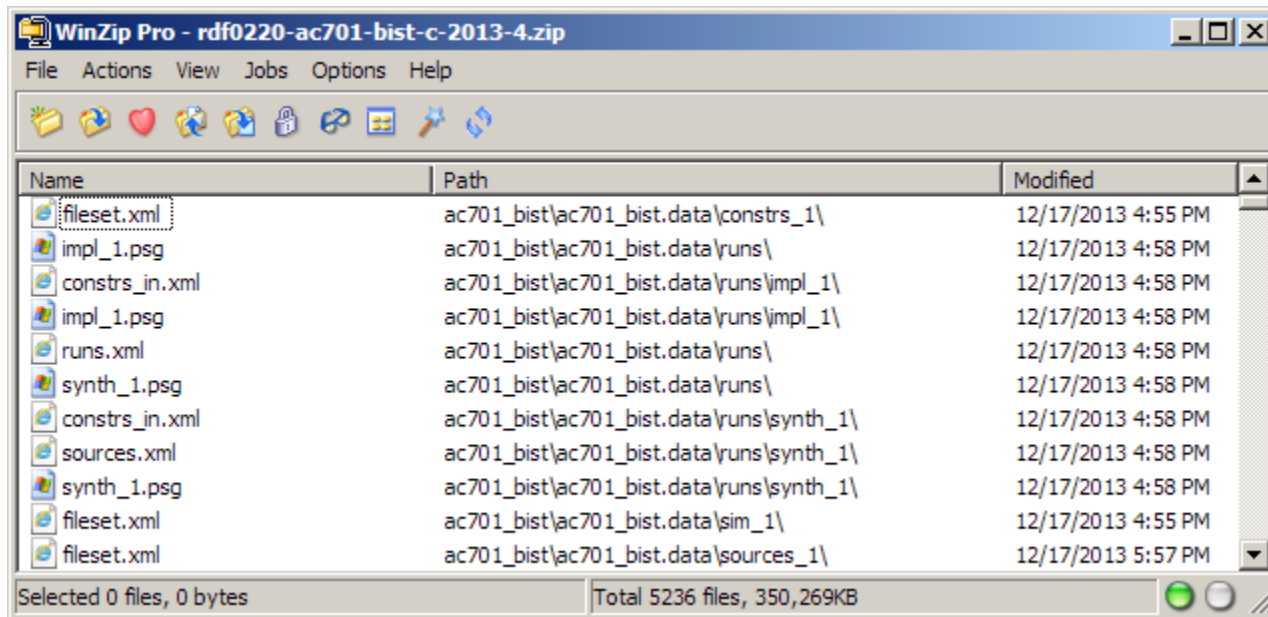
AC701 Setup

- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your USB Com Port
 - Set the baud to 9600



AC701 Setup

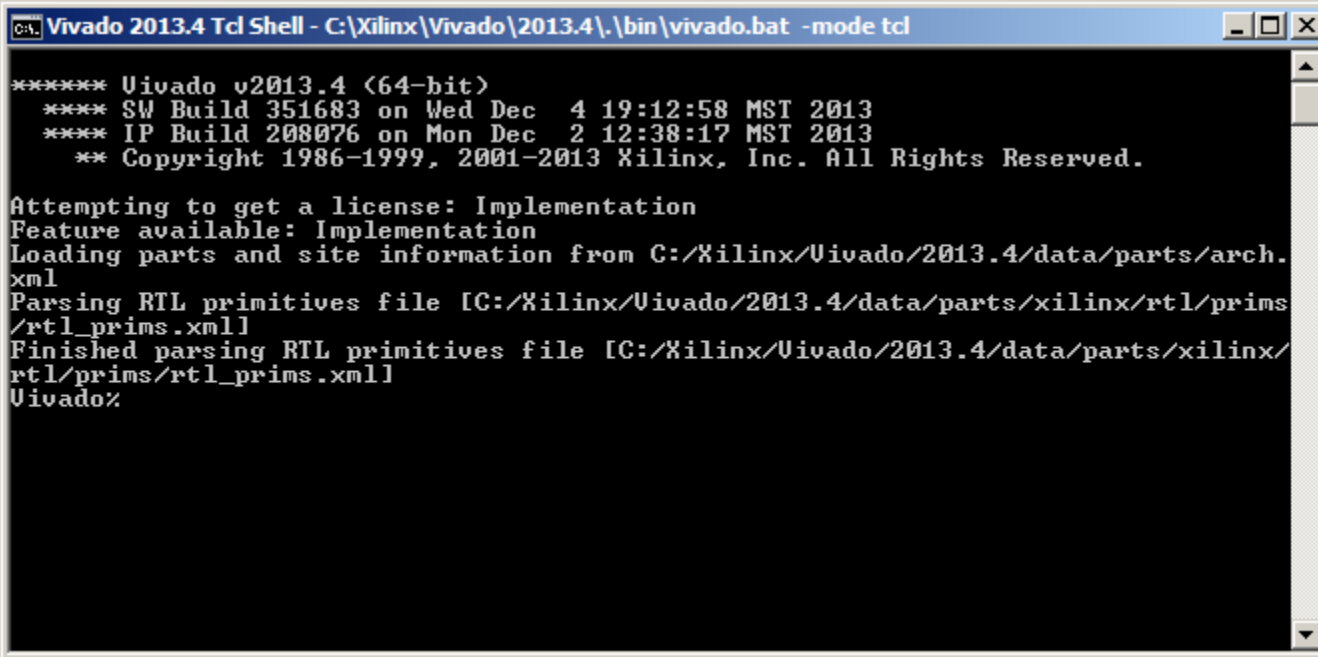
- Unzip the RDF0220 - AC701 BIST Design Files (2013.4 C) zip file
 - Available through <http://www.xilinx.com/ac701>



AC701 BIST

➤ Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2013.4 → Vivado 2013.4 Tcl Shell



```
C:\Xilinx\Vivado\2013.4\bin\vivado.bat -mode tcl

***** Vivado v2013.4 (64-bit)
***** SW Build 351683 on Wed Dec  4 19:12:58 MST 2013
***** IP Build 208076 on Mon Dec  2 12:38:17 MST 2013
***** Copyright 1986-1999, 2001-2013 Xilinx, Inc. All Rights Reserved.

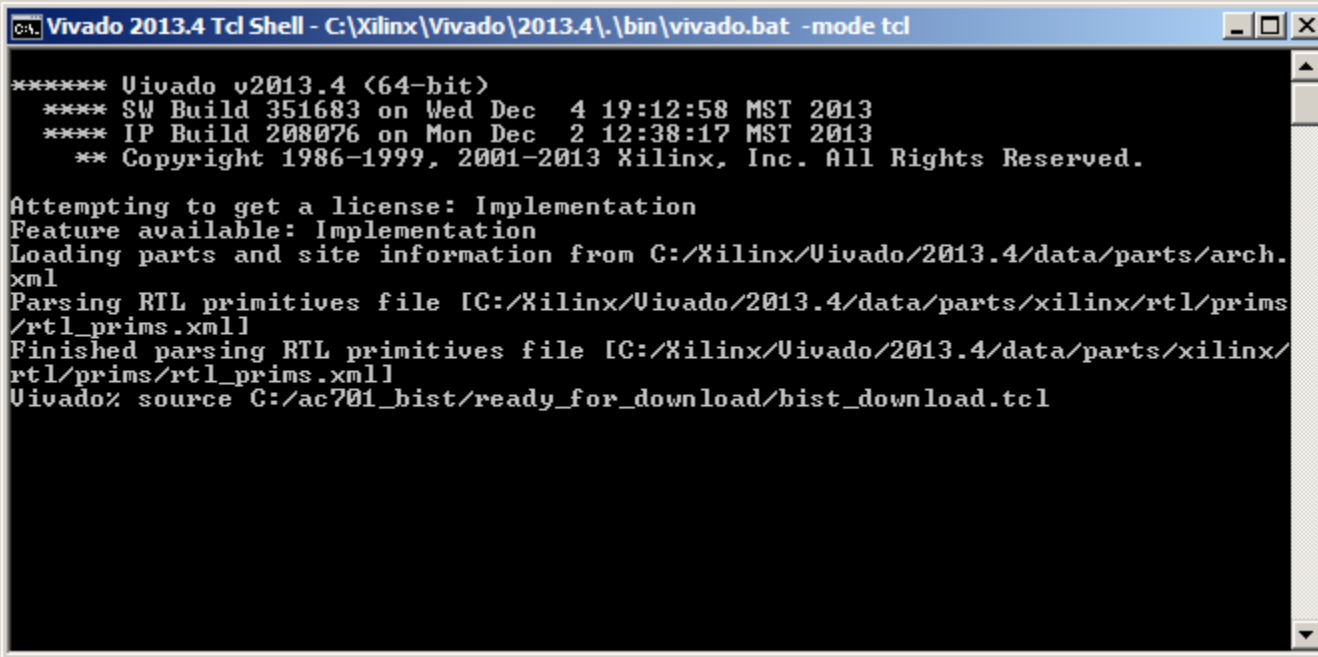
Attempting to get a license: Implementation
Feature available: Implementation
Loading parts and site information from C:/Xilinx/Vivado/2013.4/data/parts/arch.xml
Parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Finished parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Vivado%
```


AC701 BIST

➤ Download the BIST bitstream

➤ In the Vivado Tcl Shell type:

```
source C:/ac701_bist/ready_for_download/bist_download.tcl
```



```
C:\Xilinx\Vivado\2013.4\bin\vivado.bat -mode tcl

***** Vivado v2013.4 (64-bit)
***** SW Build 351683 on Wed Dec  4 19:12:58 MST 2013
***** IP Build 208076 on Mon Dec  2 12:38:17 MST 2013
***** Copyright 1986-1999, 2001-2013 Xilinx, Inc. All Rights Reserved.

Attempting to get a license: Implementation
Feature available: Implementation
Loading parts and site information from C:/Xilinx/Vivado/2013.4/data/parts/arch.xml
Parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Finished parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Vivado% source C:/ac701_bist/ready_for_download/bist_download.tcl
```

AC701 BIST

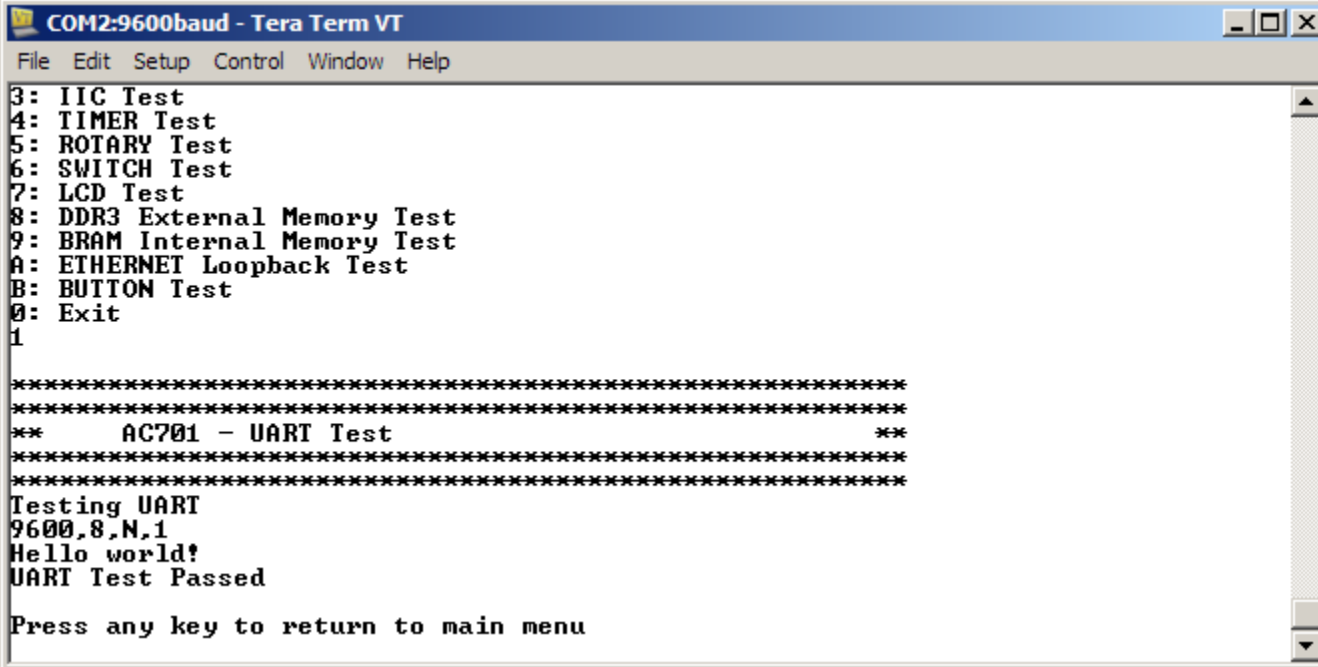
➤ View initial BIST screen

```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
*****
*****
**      Xilinx Artix-7 FPGA AC701 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
```

AC701 BIST

➤ UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
1
*****
*****
**      AC701 - UART Test      **
*****
*****
Testing UART
9600,8,N,1
Hello world!
UART Test Passed

Press any key to return to main menu
```

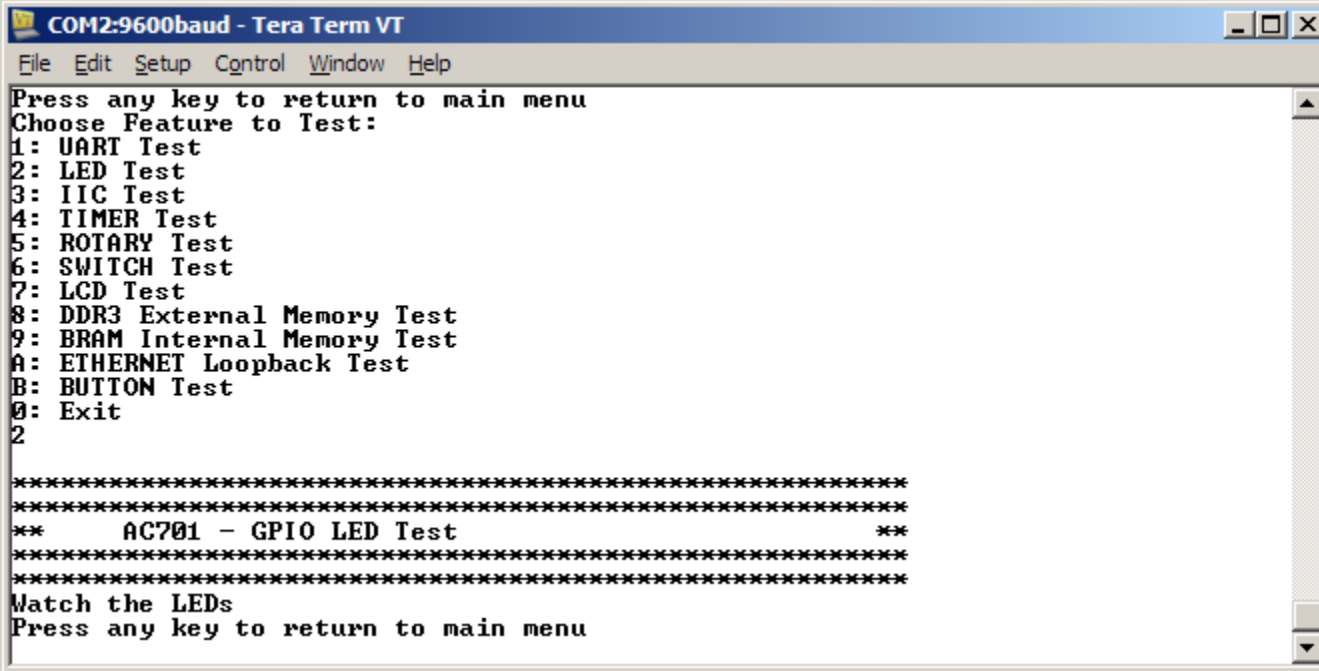
AC701 BIST

➤ LED Test

- Type **2** to begin LED Test

➤ View Walking 1's pattern on GPIO LEDs

- Sequence repeats twice



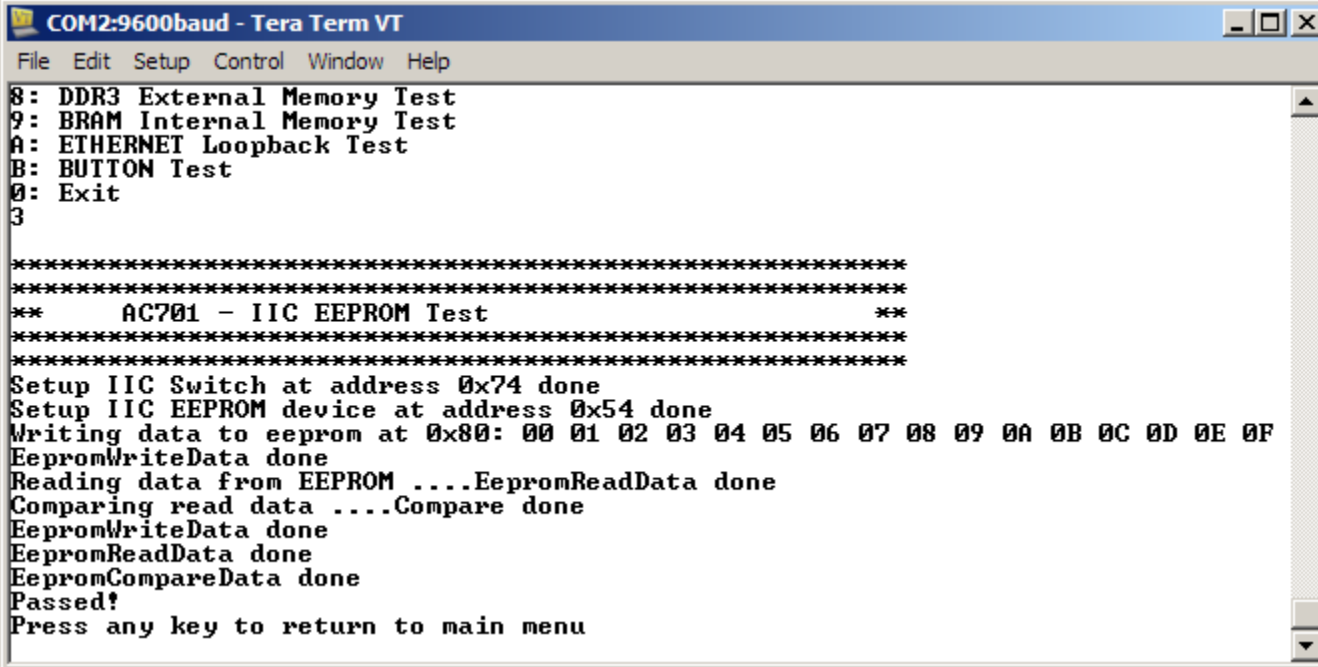
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
Press any key to return to main menu
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
2

*****
*****
**      AC701 - GPIO LED Test      **
*****
*****
Match the LEDs
Press any key to return to main menu
```

AC701 BIST

➤ IIC Test

- Type **3** to begin IIC Test

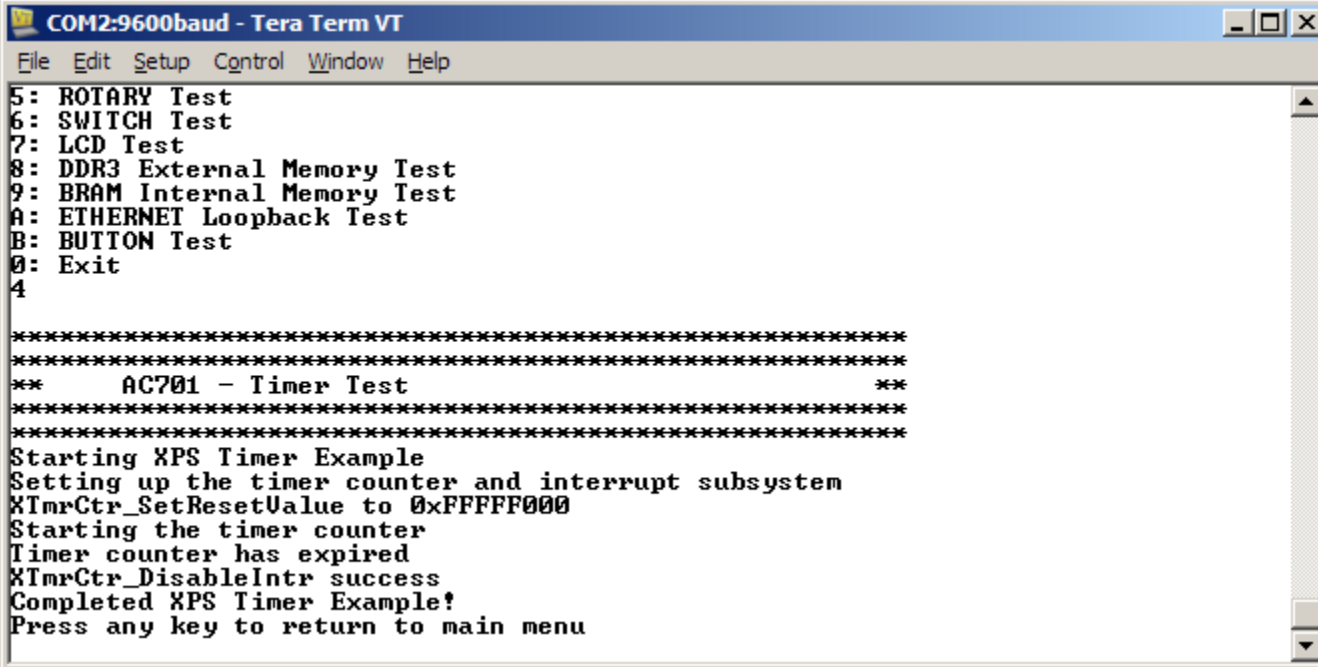


```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
3
*****
**      AC701 - IIC EEPROM Test      **
*****
Setup IIC Switch at address 0x74 done
Setup IIC EEPROM device at address 0x54 done
Writing data to eeprom at 0x80: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
EepromWriteData done
Reading data from EEPROM ....EepromReadData done
Comparing read data ....Compare done
EepromWriteData done
EepromReadData done
EepromCompareData done
Passed!
Press any key to return to main menu
```

AC701 BIST

➤ Timer Test

- Type **4** to begin Timer Test



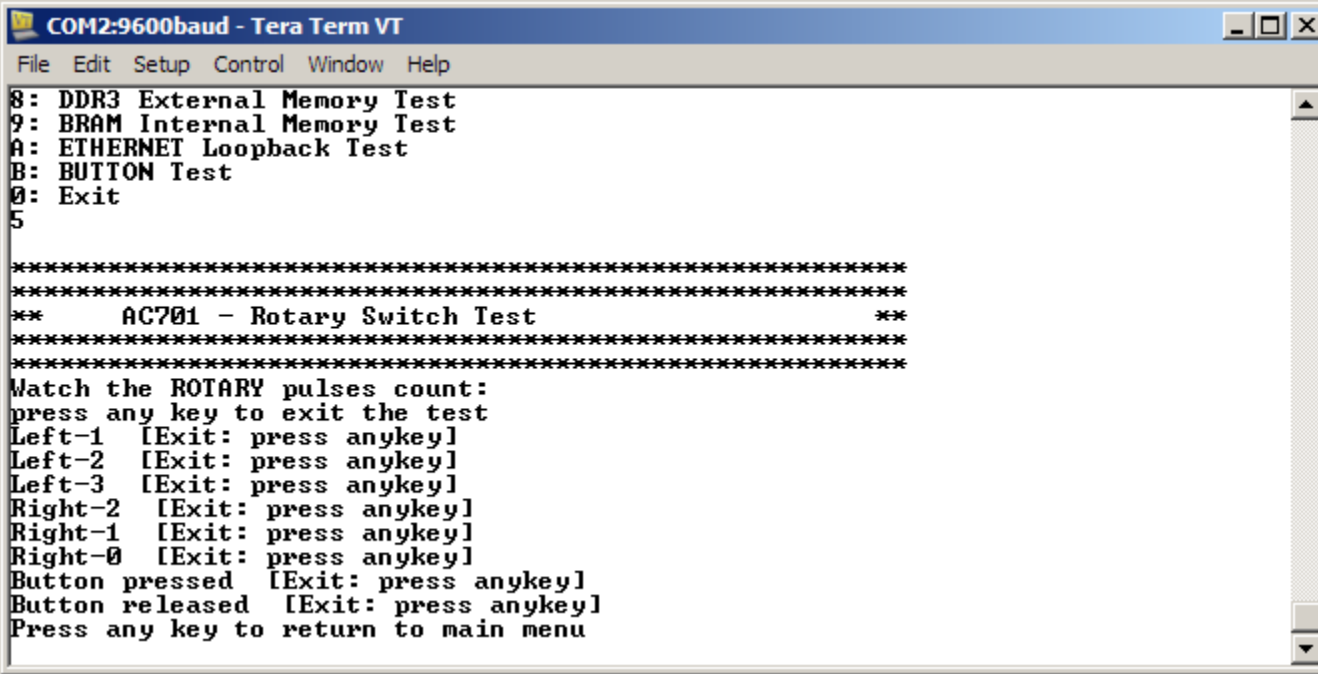
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
4

*****
**      AC701 - Timer Test      **
*****
Starting XPS Timer Example
Setting up the timer counter and interrupt subsystem
XImrCtr_SetResetUvalue to 0xFFFFF000
Starting the timer counter
Timer counter has expired
XImrCtr_DisableIntr success
Completed XPS Timer Example!
Press any key to return to main menu
```

AC701 BIST

➤ Rotary Test

- Type **5** to begin Rotary Test
- Turn the rotary switch (under the LCD) back and forth

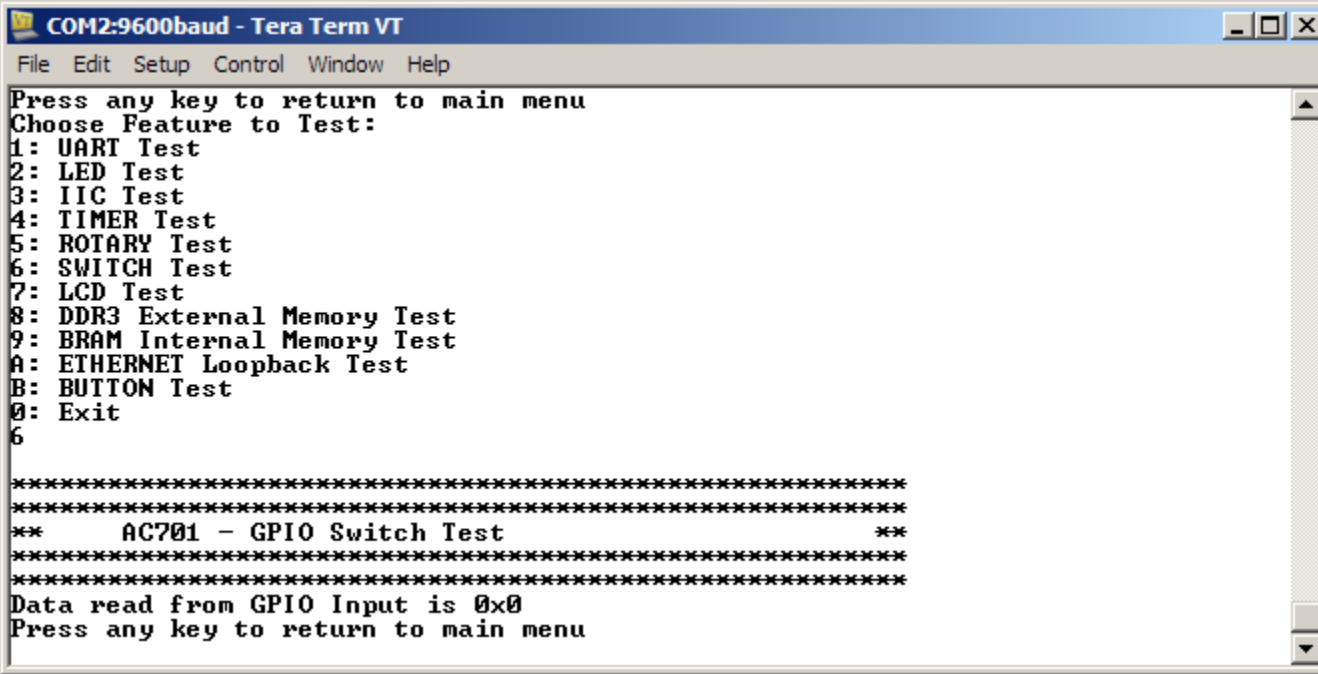


```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
5
*****
*****
**      AC701 - Rotary Switch Test      **
*****
*****
Match the ROTARY pulses count:
press any key to exit the test
Left-1 [Exit: press anykey]
Left-2 [Exit: press anykey]
Left-3 [Exit: press anykey]
Right-2 [Exit: press anykey]
Right-1 [Exit: press anykey]
Right-0 [Exit: press anykey]
Button pressed [Exit: press anykey]
Button released [Exit: press anykey]
Press any key to return to main menu
```

AC701 BIST

➤ GPIO Switch Test

- Set 4-position GPIO DIP Switch (SW2)
- Type **6** to begin GPIO Switch Test
 - Reads switch settings

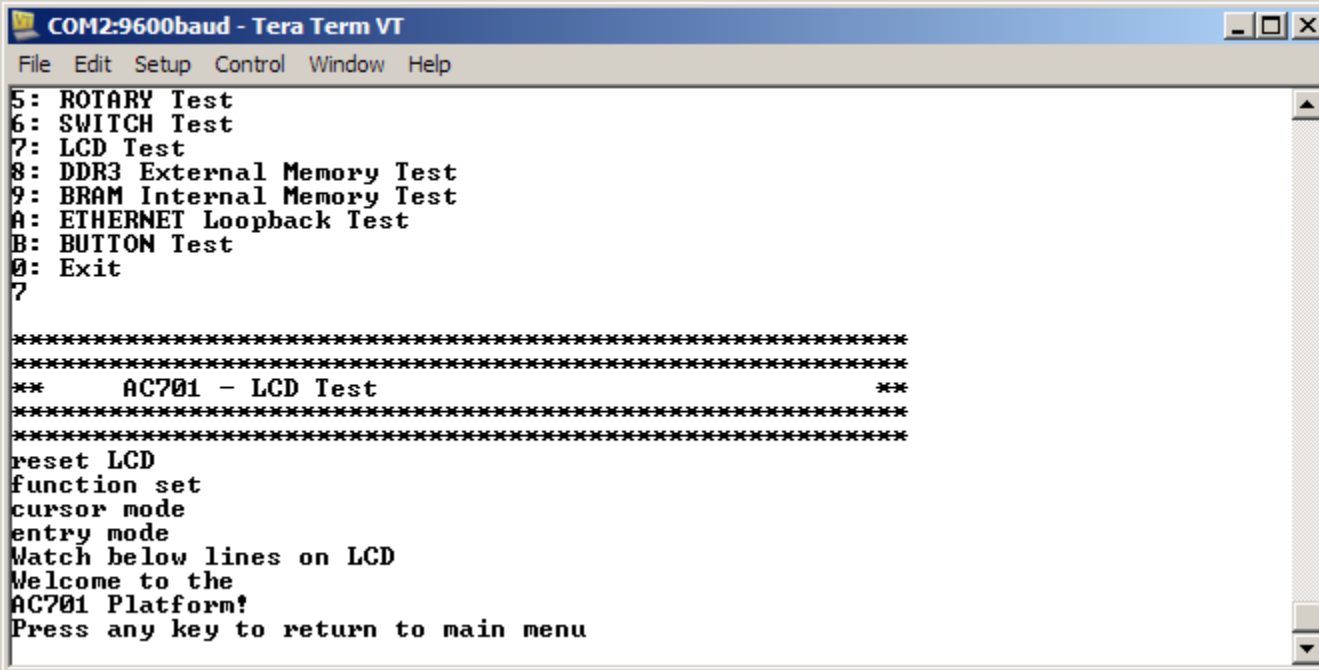


```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
Press any key to return to main menu
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
6
*****
**      AC701 - GPIO Switch Test      **
*****
Data read from GPIO Input is 0x0
Press any key to return to main menu
```


AC701 BIST

➤ LCD Test

- Type 7 to begin LCD Test



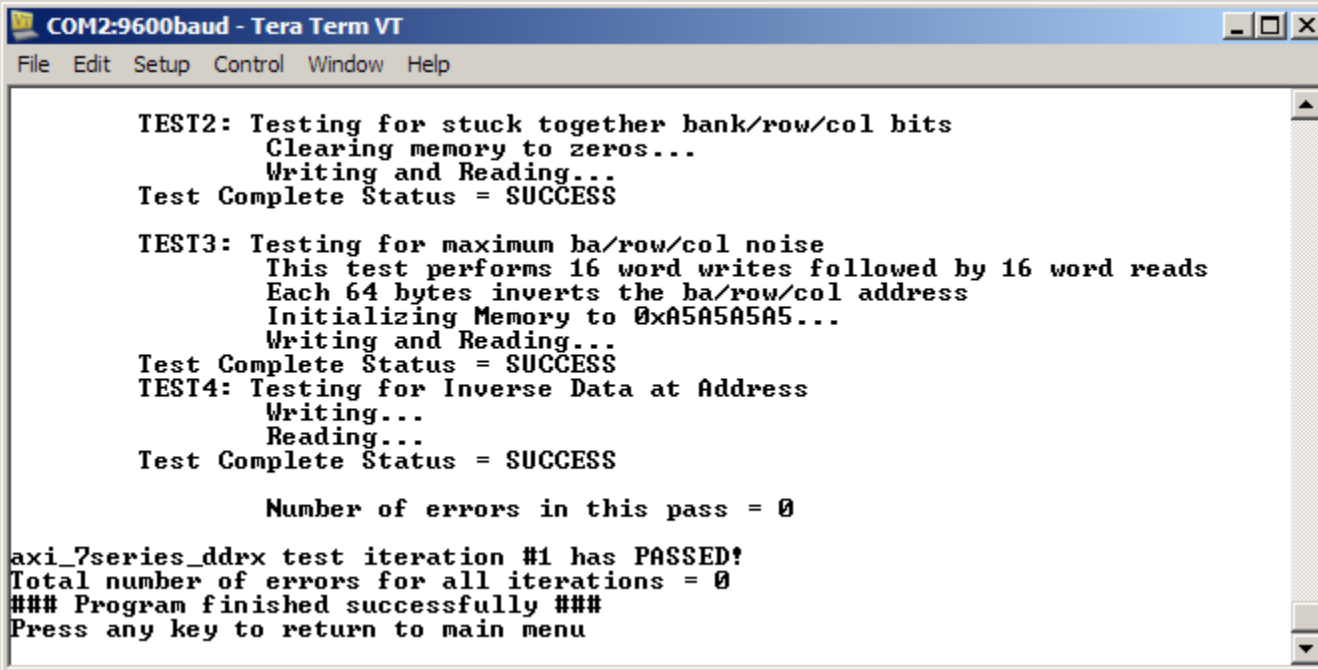
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
7

*****
**      AC701 - LCD Test      **
*****
reset LCD
function set
cursor mode
entry mode
Match below lines on LCD
Welcome to the
AC701 Platform!
Press any key to return to main menu
```

AC701 BIST

➤ External Memory Test

- Type **8** to begin External Memory Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help

TEST2: Testing for stuck together bank/row/col bits
      Clearing memory to zeros...
      Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
      This test performs 16 word writes followed by 16 word reads
      Each 64 bytes inverts the ba/row/col address
      Initializing Memory to 0xA5A5A5A5...
      Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
      Writing...
      Reading...
Test Complete Status = SUCCESS

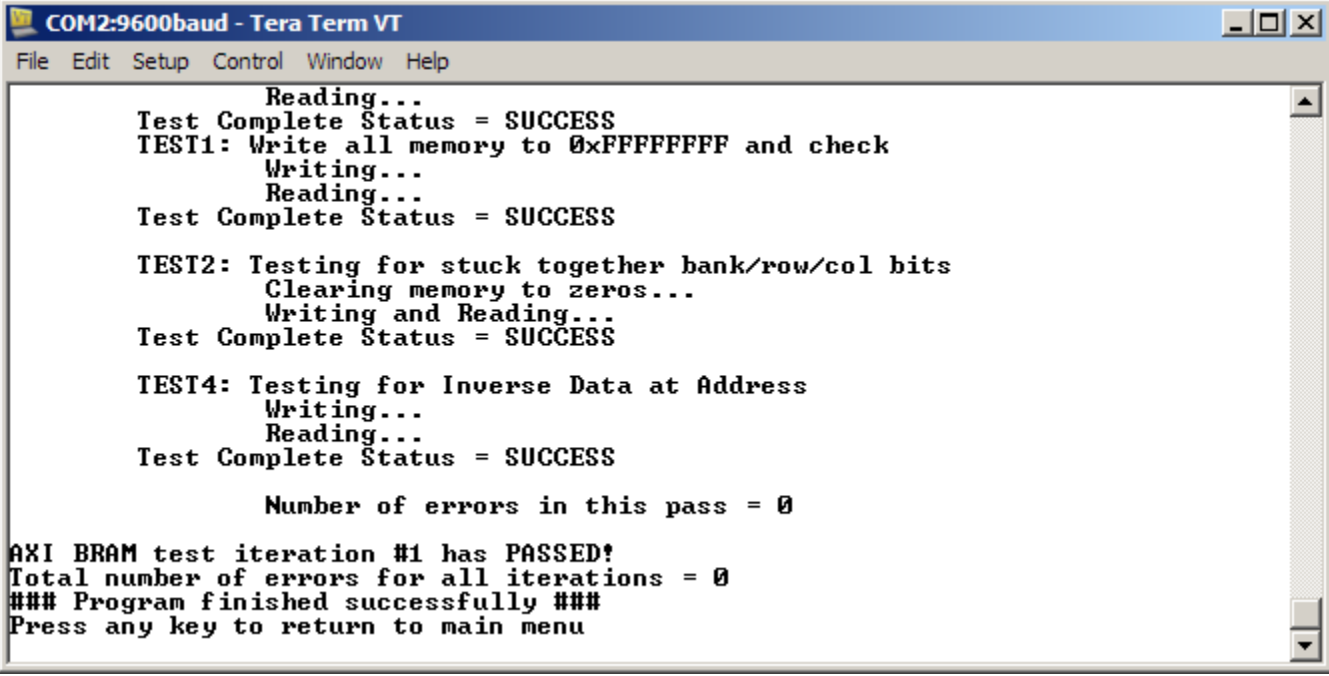
      Number of errors in this pass = 0

axi_7series_ddrx test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
Press any key to return to main menu
```

AC701 BIST

➤ Internal Memory Test

- Type **9** to begin BRAM Memory Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help

    Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
    Writing...
    Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
    Clearing memory to zeros...
    Writing and Reading...
Test Complete Status = SUCCESS

TEST4: Testing for Inverse Data at Address
    Writing...
    Reading...
Test Complete Status = SUCCESS

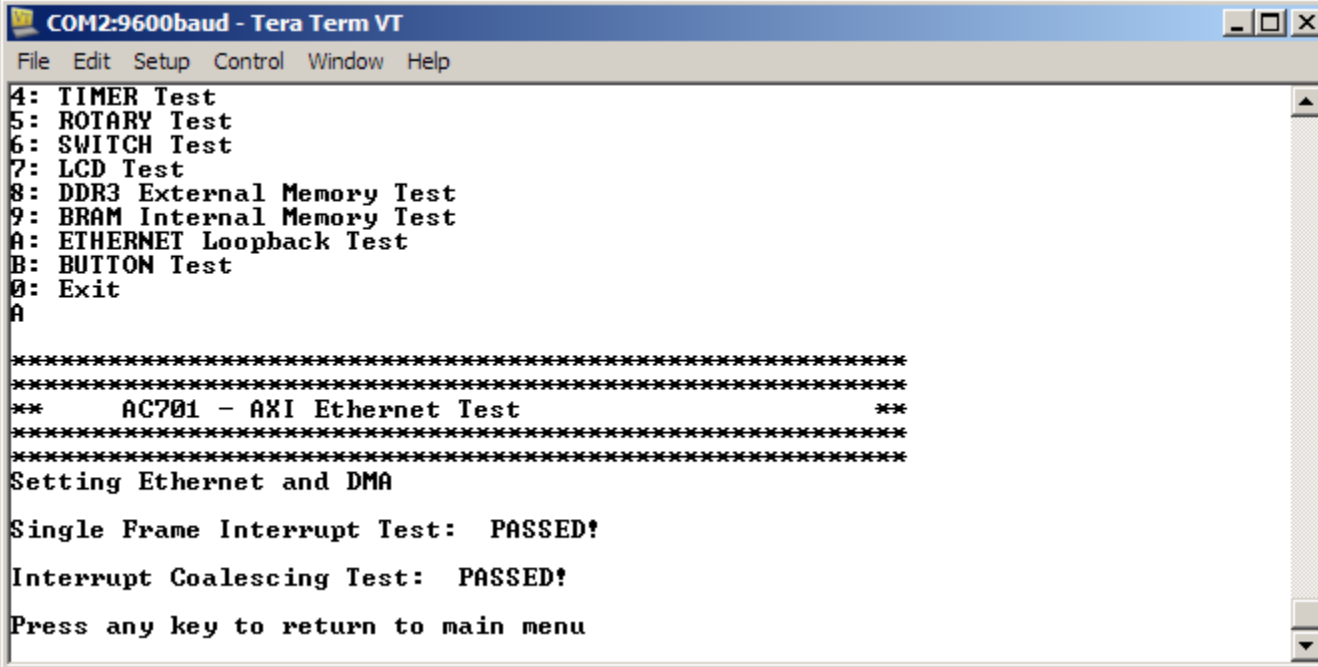
    Number of errors in this pass = 0

AXI BRAM test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
Press any key to return to main menu
```

AC701 BIST

➤ Ethernet Test

- Type **A** to begin AXI Ethernet Test

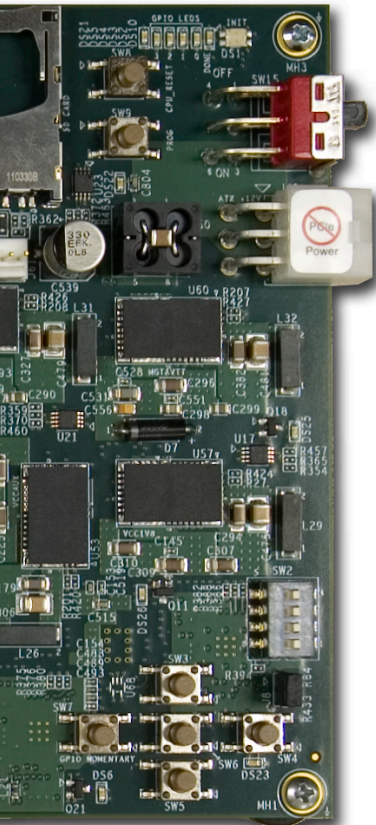


```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
A
*****
**      AC701 - AXI Ethernet Test      **
*****
Setting Ethernet and DMA
Single Frame Interrupt Test:  PASSED!
Interrupt Coalescing Test:  PASSED!
Press any key to return to main menu
```

AC701 BIST

➤ Button Test

- Type **B** to begin Button Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
A: ETHERNET Loopback Test
B: BUTTON Test
Ø: Exit
B

*****
*****
**      AC701 - Button Test      **
*****
*****
Press west button

Press south button

Press east button

Press north button

Press center button

Press any button

Press any key to return to main menu
```

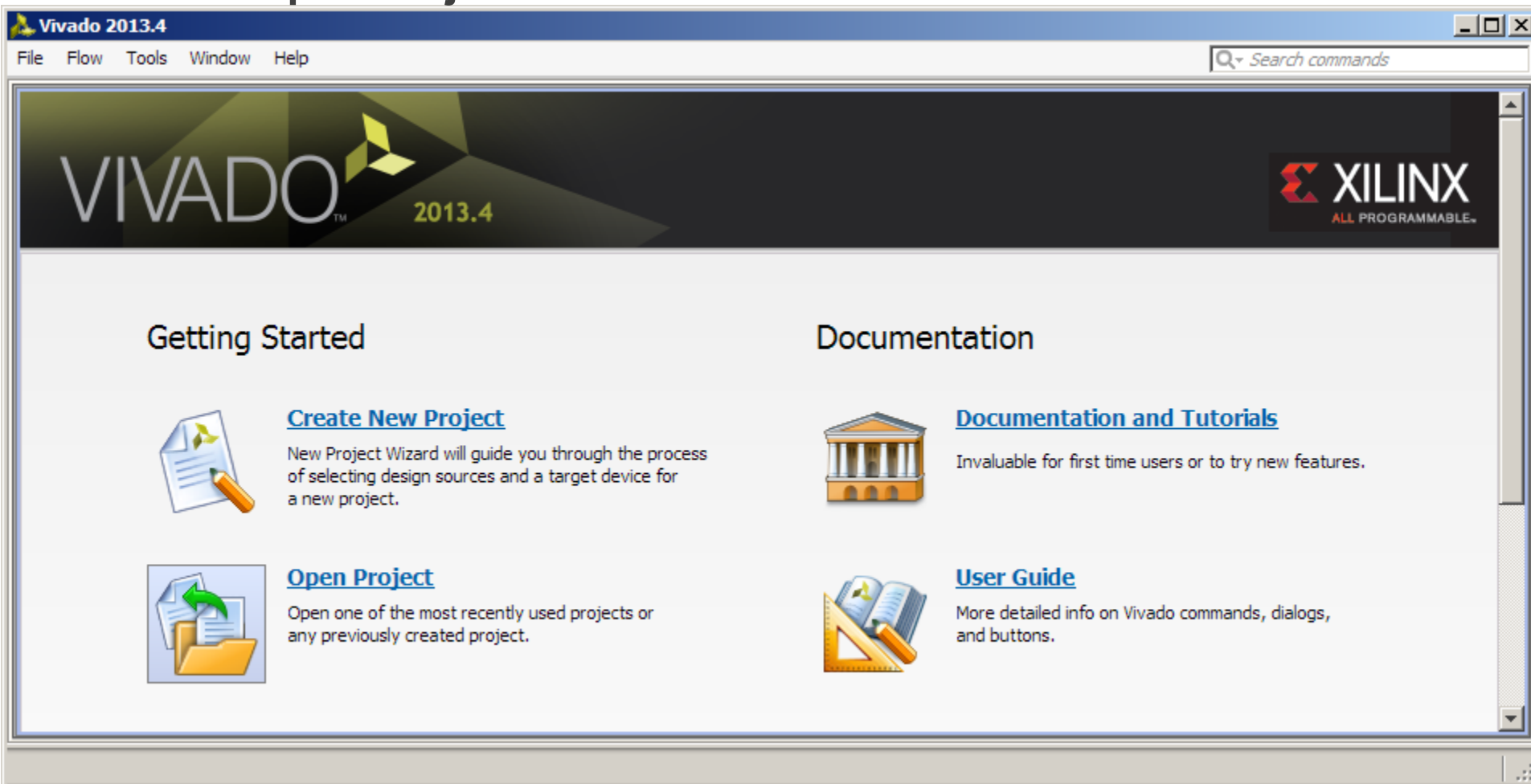
Compile AC701 BIST Design

Compile AC701 BIST Design

➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2013.4 → Vivado

➤ Select Open Project



Compile AC701 BIST Design

- Open the AC701 Design:
 - <Design Name>\ac701_bist.xpr

The screenshot displays the Vivado 2013.4 IDE interface for a project named 'ac701_bist'. The 'Project Manager' window shows the design sources, including 'system_wrapper (system_wrapper.v) (1)'. The 'Project Summary' window provides details about the project settings, including the project name, product family (Artix-7), project part (Artix-7 AC701 Evaluation Platform), and board name (xilinx.com:artix7:ac701:1.0). The 'Design Runs' window shows the synthesis and implementation steps completed, with the status 'write_bitstream Complete' displayed in the top right corner.

Name	Part	Constraints	Strategy	
synth_1	xc7a200tfg676-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2013)	synth_1
impl_1	xc7a200tfg676-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2013)	write_1

Note: Presentation applies to the AC701

Compile AC701 BIST Design

- The design is fully implemented; you can recompile, or export to SDK
 - To recompile, right-click **synth_1**, select **Reset Runs** then **Generate Bitstream**

The screenshot displays the Vivado 2013.4 IDE interface for a project named 'ac701_bist'. The 'Flow Navigator' on the left shows the project progress through 'RTL Analysis', 'Synthesis', and 'Implementation'. The 'Implementation' section is expanded, and the 'Generate Bitstream' option is highlighted with a red box. The 'Project Manager' window shows the 'Sources' tab with 'system_wrapper' and 'Configuration Files'. The 'Design Runs' window shows 'synth_1' selected, and a context menu is open over it with 'Reset Runs' highlighted. The 'Project Summary' window shows project settings for 'ac701_bist' on an 'Artix-7' device. The status bar at the bottom indicates 'write_bitstream Complete'.

ac701_bist - [C:/ac701_bist/ac701_bist.xpr] - Vivado 2013.4

File Edit Flow Tools Window Layout View Help

Search commands

write_bitstream Complete

Flow Navigator

Project Manager - ac701_bist

Sources

Design Sources (2)

- system_wrapper (system_wrapper.v) (1)
- Configuration Files (1)
- Constraints (1)

Hierarchy IP Sources Libraries Compile Order

Sources Templates

Synthesis Run Properties

synth_1

Design Runs

Name

- synth_1
- impl_1

Synthesis Run Properties... Ctrl+E

Delete Delete

Make Active

Change Run Settings...

Save As Strategy...

Launch Runs...

Reset Runs

Launch Next Step

Reset to Previous Step: synth_design

Open Elaborated Design

Project Summary

Project Settings

Project name: ac701_bist

Product family: Artix-7

Project part: Artix-7 AC701 Evaluation Platform (xc7a100tcefg3243-1)

Top module name: system_wrapper

Board

Display name: Artix-7 AC701 Evaluation Platform

Board name: xilinx.com:artix7:ac701:1.0

Strategy

Results (Vivado Synthesis 2013) synth_1

Defaults (Vivado Implementation 2013) write_bitstream

Generate a programming file after implementation

Note: Presentation applies to the AC701

Compile AC701 BIST Design

- Once done, both the Synthesis and Implementation will have green check marks

The screenshot displays the Vivado 2013.4 IDE interface for a project named 'ac701_bist'. The 'Design Runs' table at the bottom shows the following data:

Name	Part	Constraints	Strategy	
synth_1	xc7a200tfg676-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2013)	synth_1
impl_1	xc7a200tfg676-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2013)	write_bitstream Complete

The 'Project Summary' window shows the following details:

- Project Settings:**
 - Project name: ac701_bist
 - Product family: Artix-7
 - Project part: Artix-7 AC701 Evaluation Platform (xc7a200tfg676-2)
 - Top module name: system_wrapper
- Board:**
 - Display name: Artix-7 AC701 Evaluation Platform
 - Board name: xilinx.com:artix7:ac701:1.0

Compile AC701 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design

The screenshot displays the Vivado 2013.4 IDE interface for a project named 'ac701_bist'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A search bar for commands is visible on the right. The main workspace is divided into several panes:

- Flow Navigator:** Shows the project hierarchy with 'Project Manager' selected.
- Project Manager - ac701_bist:** Displays the 'Sources' pane with a tree view showing 'Design Sources (2)', including 'system_wrapper (system_wrapper.v) (1)', 'Configuration Files (1)', and 'Constraints (1)'. The 'Hierarchy' tab is active, and the 'Sources' sub-tab is selected. A tooltip for 'system.bd' is visible over the 'Open Block Design' icon.
- Project Summary:** A floating window showing project details:
 - Project Settings:** Project name: ac701_bist; Product family: Artix-7; Project part: Artix-7 AC701 Evaluation Platform (xc7a200t); Top module name: system_wrapper.
 - Board:** Display name: Artix-7 AC701 Evaluation Platform; Board name: xilinx.com:artix7:ac701:1.0.
- Design Runs:** A table showing the compilation progress:

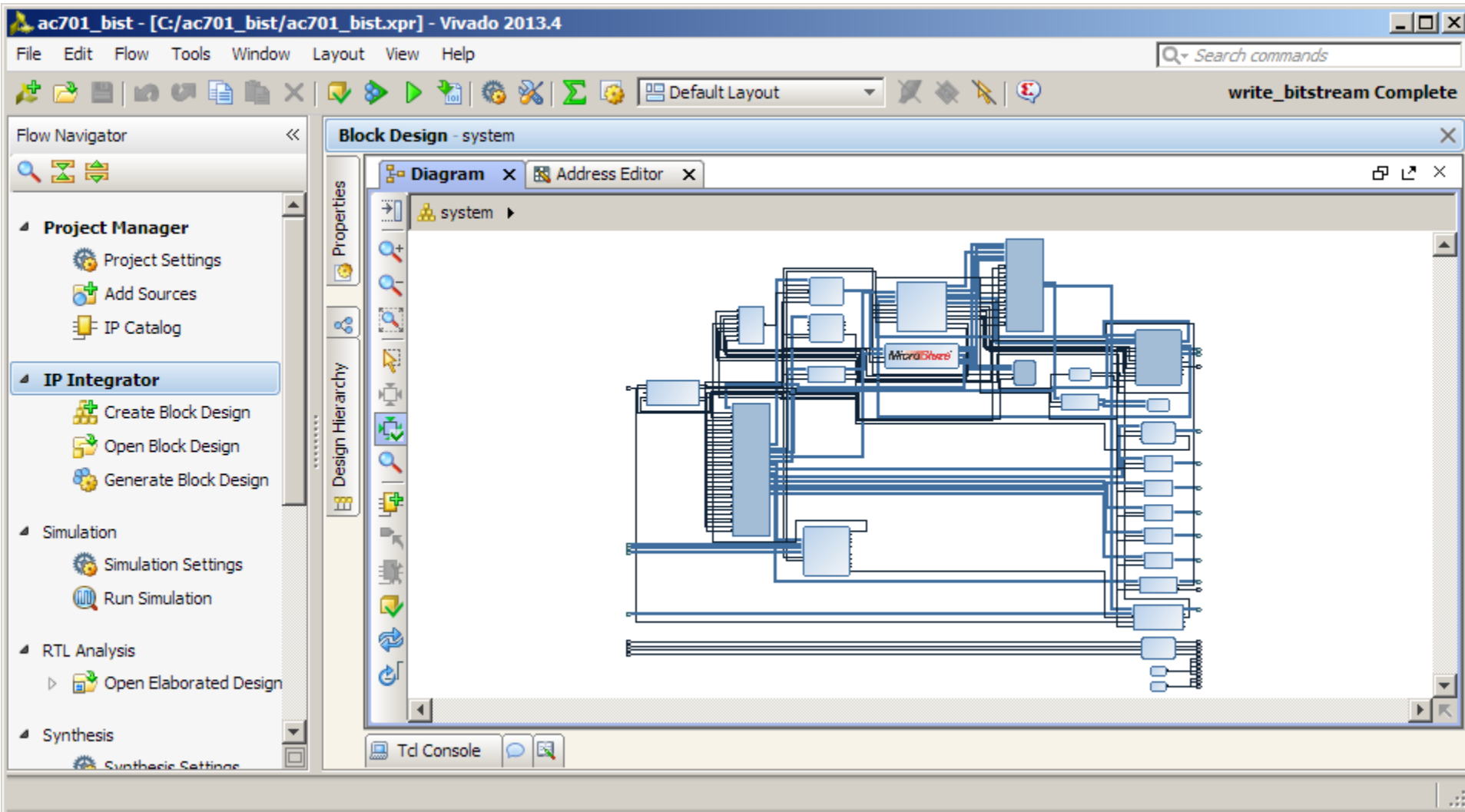
Name	Part	Constraints	Strategy	
synth_1	xc7a200tfg676-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2013)	synth_1
impl_1	xc7a200tfg676-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2013)	write_bitstream Complete

The bottom status bar shows 'system.bd' and navigation icons for Td Console, Messages, Log, Reports, and Design Runs.

Note: Presentation applies to the AC701

Compile AC701 BIST Design

➤ All the IP Blocks used in the design can be seen in this view



Note: Presentation applies to the AC701

Compile AC701 BIST Design

- To export to SDK, the Block and Implemented designs must be open
- Click Open Implemented Design

The screenshot displays the Vivado 2013.4 IDE interface for a project named 'ac701_bist'. The main window shows a 'Block Design - system' diagram with various components and interconnections. On the left, the 'Flow Navigator' pane is open, showing the project's workflow. Under the 'Implementation' section, the 'Open Implemented Design' option is highlighted. The status bar at the bottom indicates 'Analyze and constrain an Implemented Design'.

Flow Navigator:

- RTL Analysis
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager
 - Launch iMPACT

Block Design - system

Diagram x Address Editor x

system

write_bitstream Complete

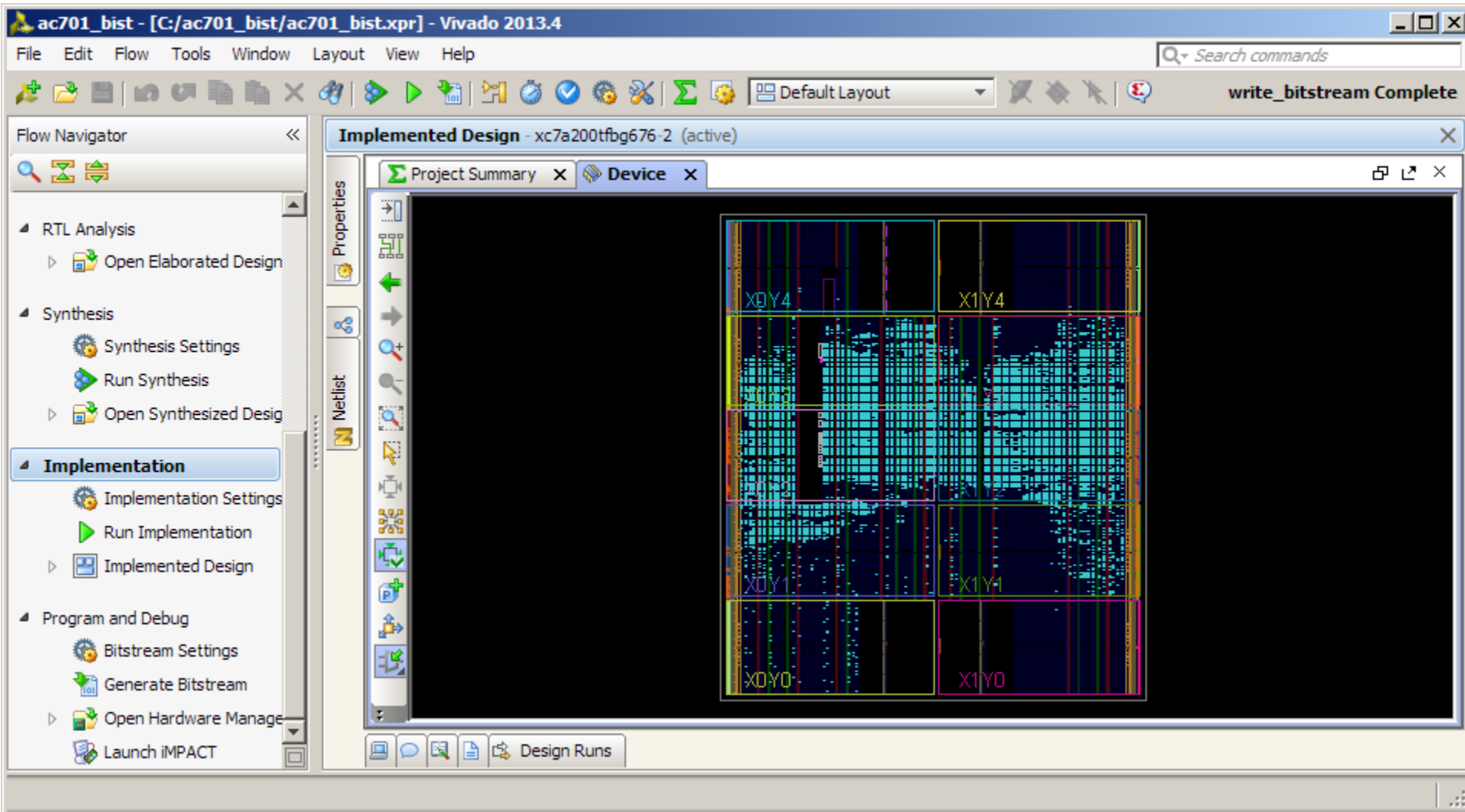
Tcl Console

Analyze and constrain an Implemented Design

Note: Presentation applies to the AC701

Compile AC701 BIST Design

➤ View Implemented Design



Note: Presentation applies to the AC701

Compile AC701 BIST Design

➤ Select File → Export → Export hardware for SDK...

➤ Select Launch SDK and click OK

The screenshot displays the Vivado 2013.4 software interface. On the left, the 'File' menu is open, with 'Export' selected. A sub-menu is visible, showing 'Export Hardware for SDK...' as the first option. In the center, the 'Export Hardware for SDK' dialog box is open. It contains the following options:

- Source: system.bd
- Export to: <Local to Project>
- Workspace: <Local to Project>
- Export Hardware
- Include bitstream (Note: an implemented design must be loaded)
- Launch SDK

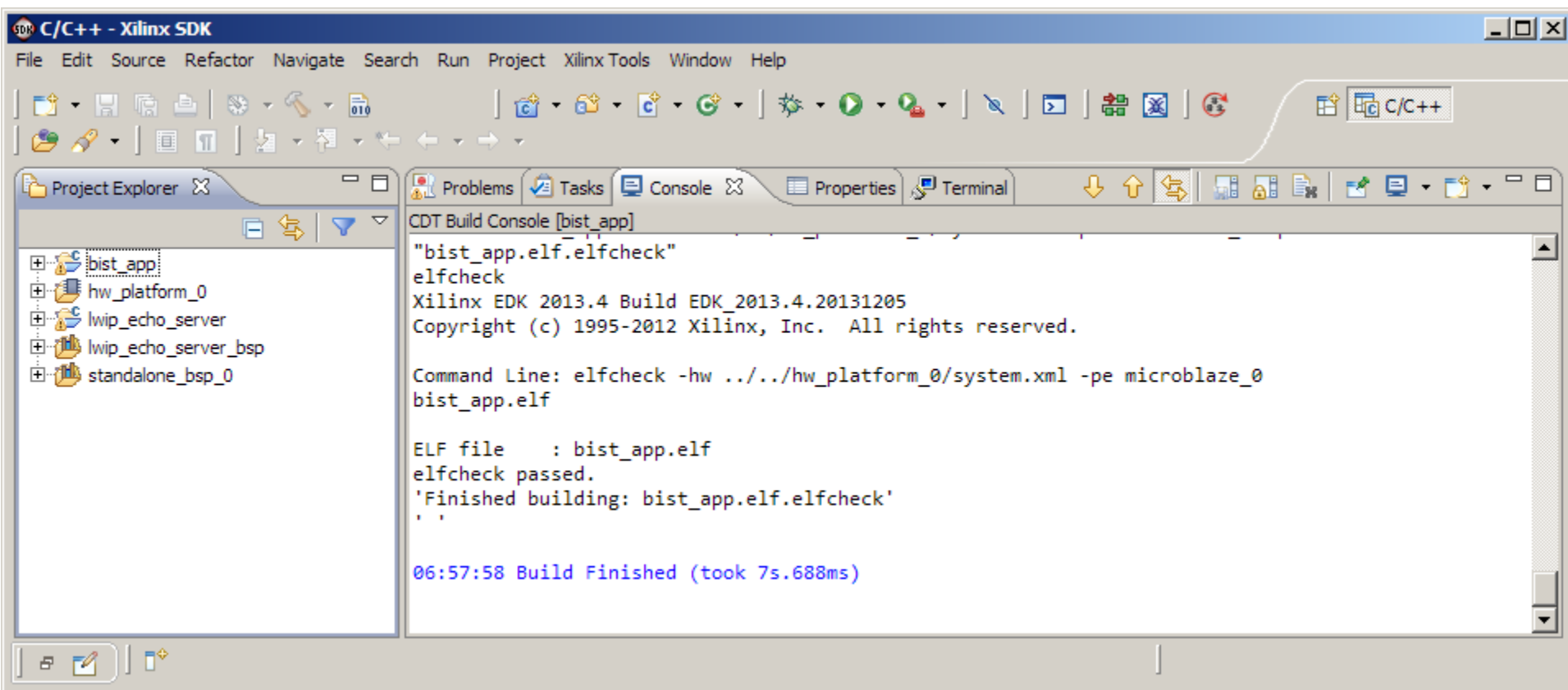
The background shows the 'Implemented Design' window for device xc7a200tfg676-2, with a 'write_bitstream Complete' status bar at the top right.

Note: Presentation applies to the AC701

Compile AC701 Software in SDK

➤ SDK Software Compile - Build ELF files in SDK

- Project builds automatically
- When done, close SDK and return to Vivado

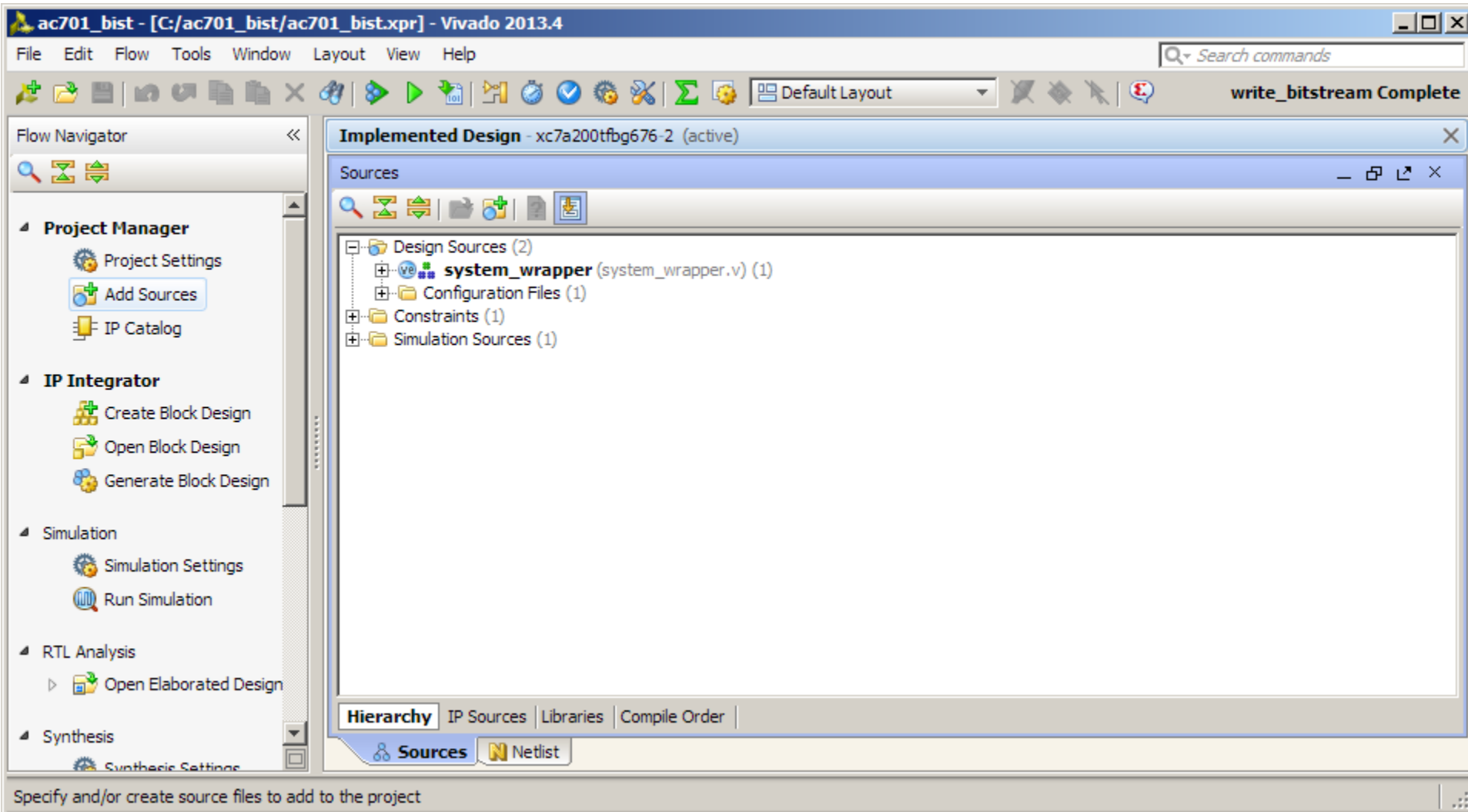




Program AC701 with BIST Design

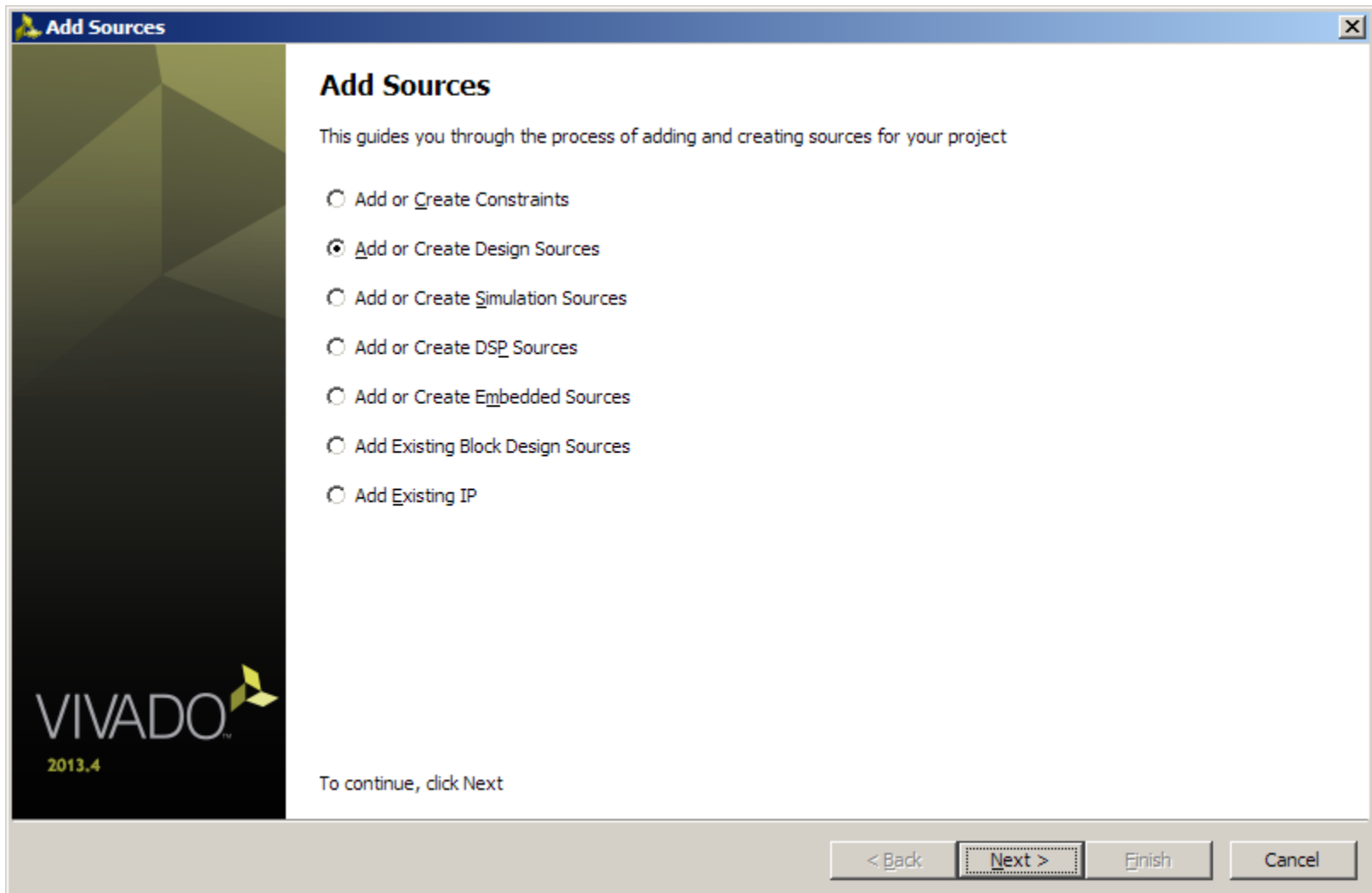
Program AC701 with BIST Design

➤ Select Add Sources



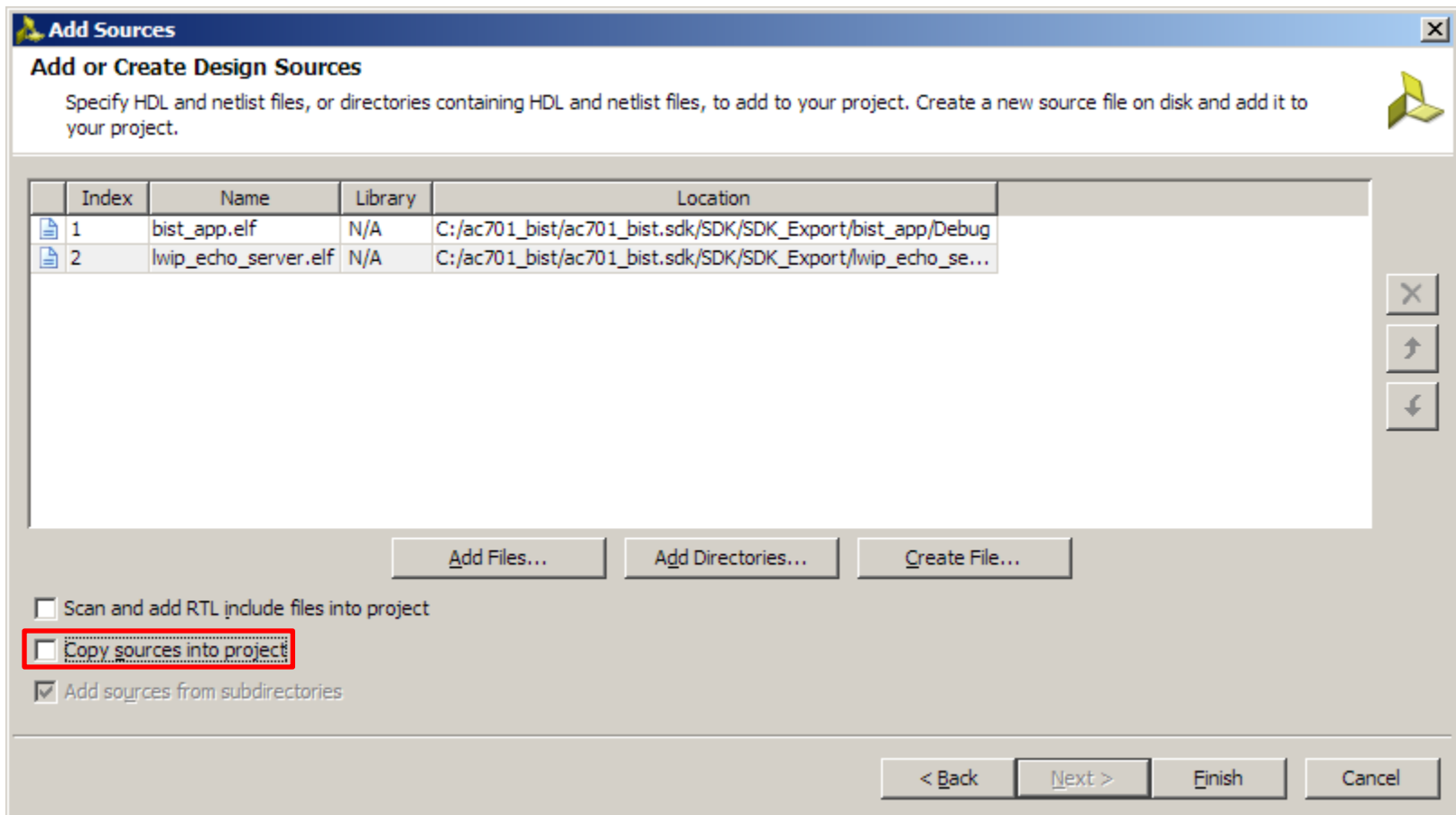
Program AC701 with BIST Design

➤ Select Add or Create Design Sources



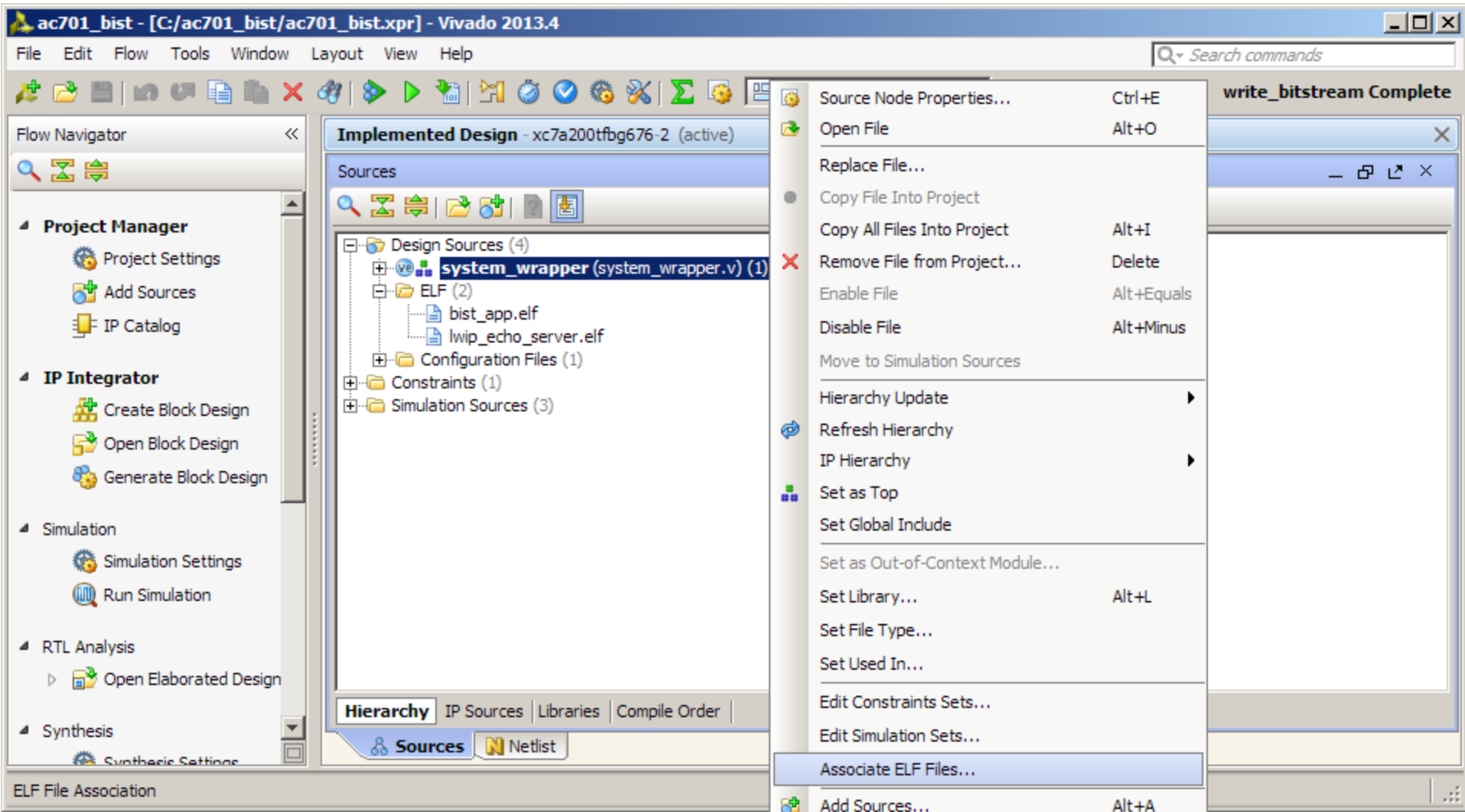
Program AC701 with BIST Design

- Add bist_app.elf and lwip_echo_server.elf from the SDK tree
- Make sure Copy sources into project is deselected
- Click Finish



Program AC701 with BIST Design

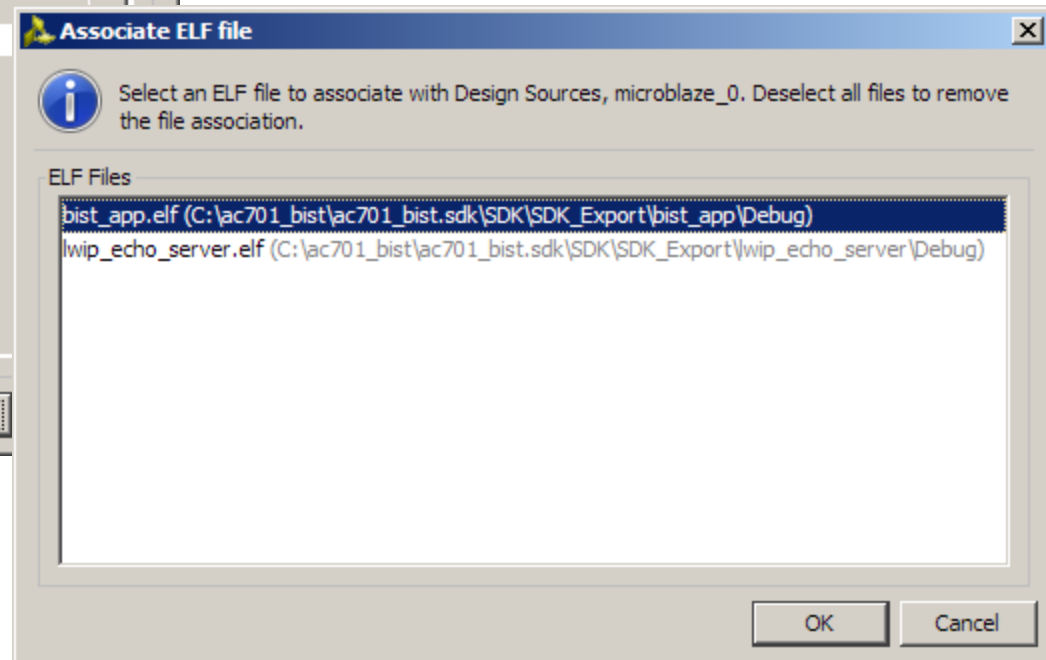
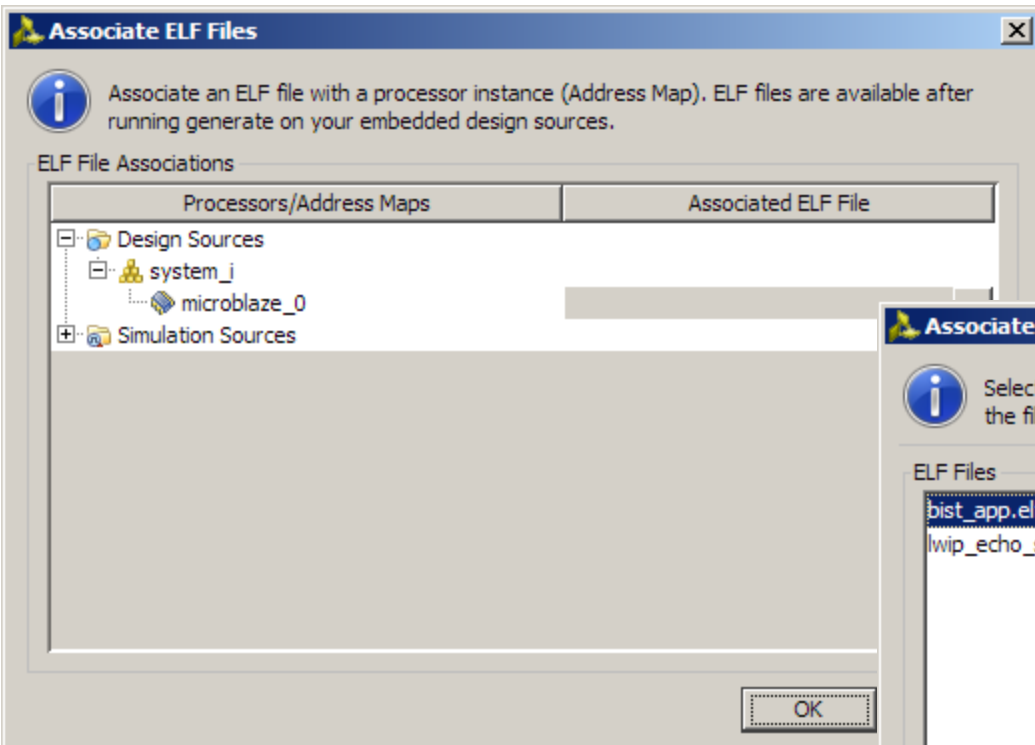
➤ Right-click on the Design and select Associate ELF Files...



Note: Presentation applies to the AC701

Program AC701 with BIST Design

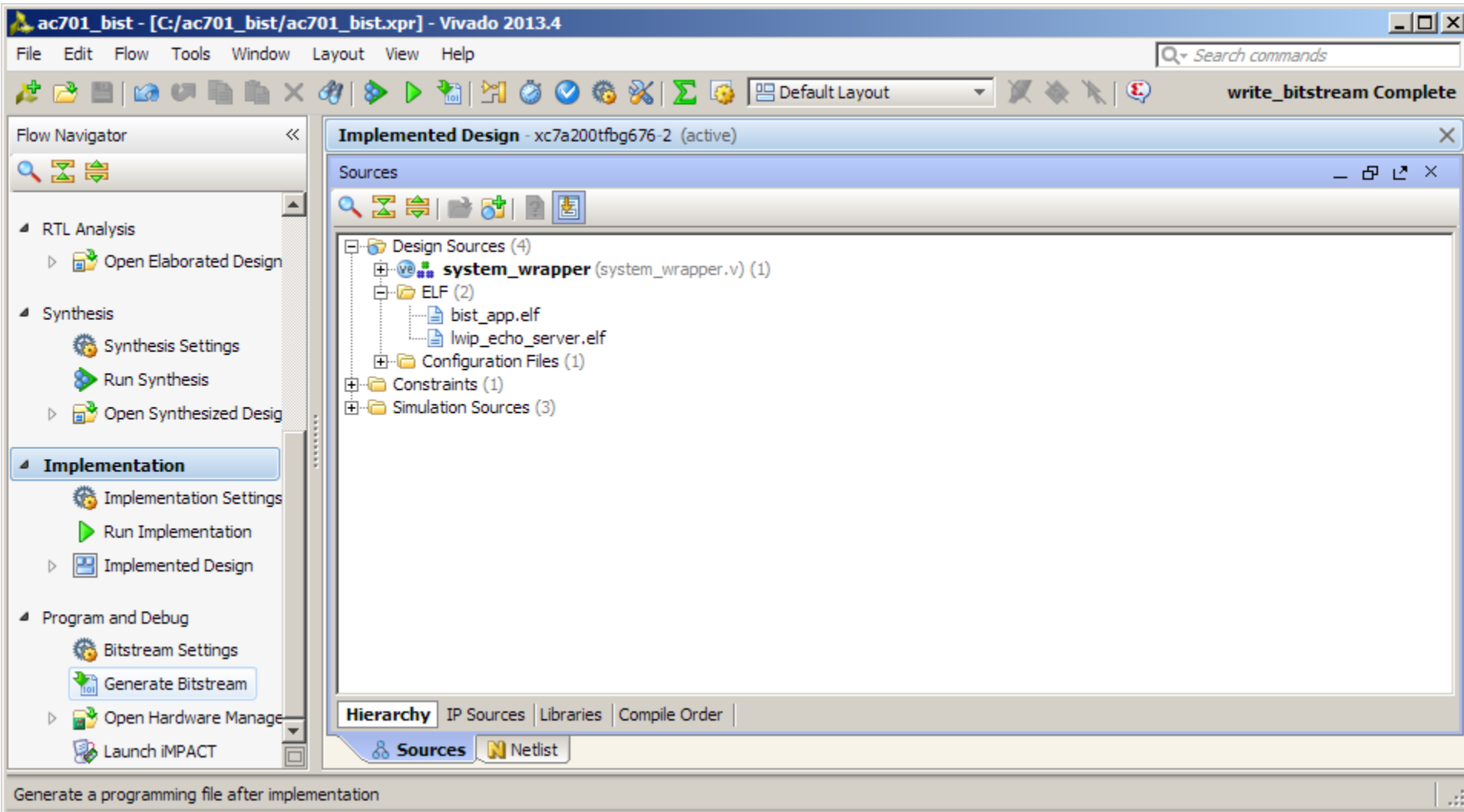
- Click the button to the right; select the bist_app.elf then click OK twice



Program AC701 with BIST Design

➤ Select Generate Bitstream

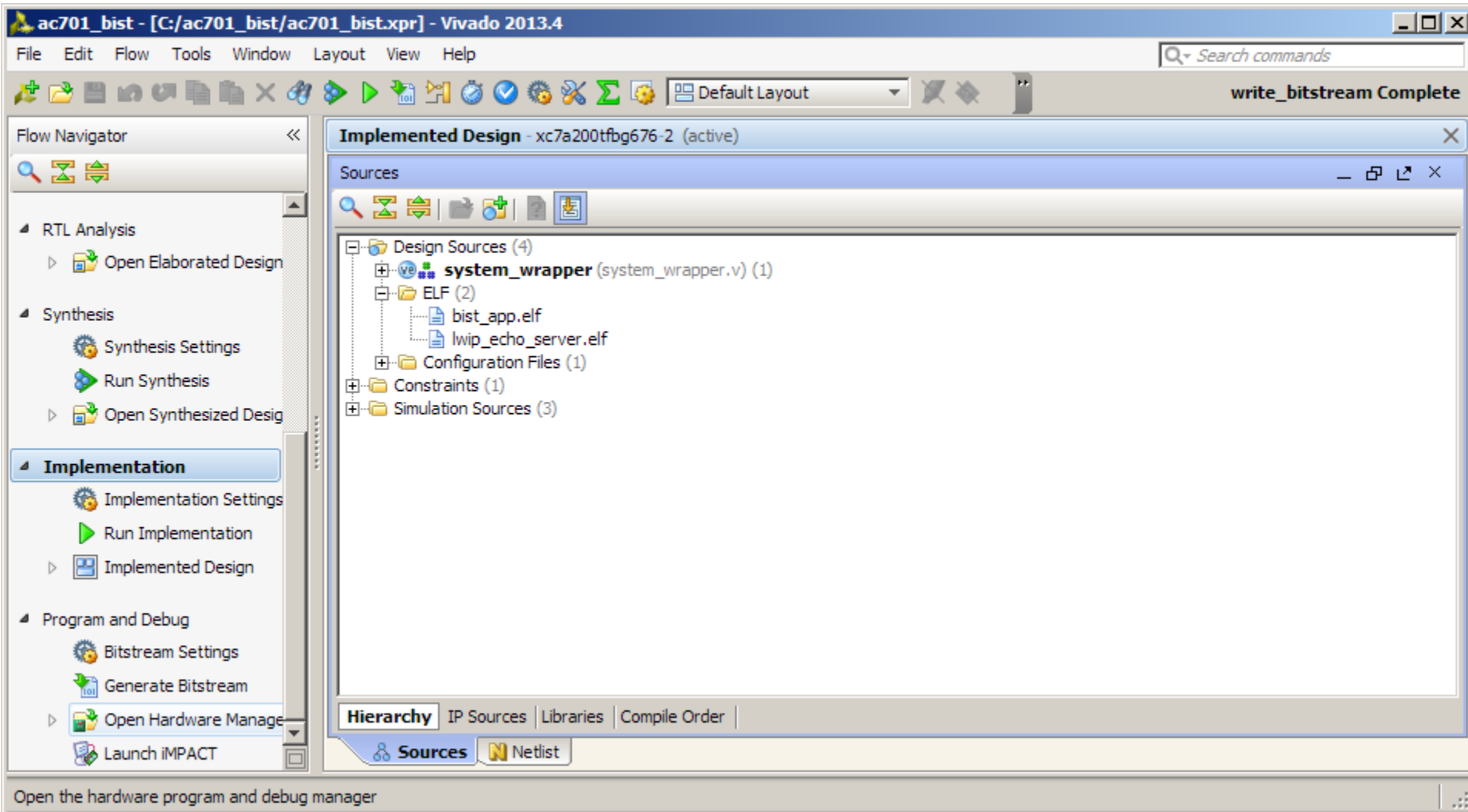
- This creates a bitstream with the BIST ELF file



Note: Presentation applies to the AC701

Program AC701 with BIST Design

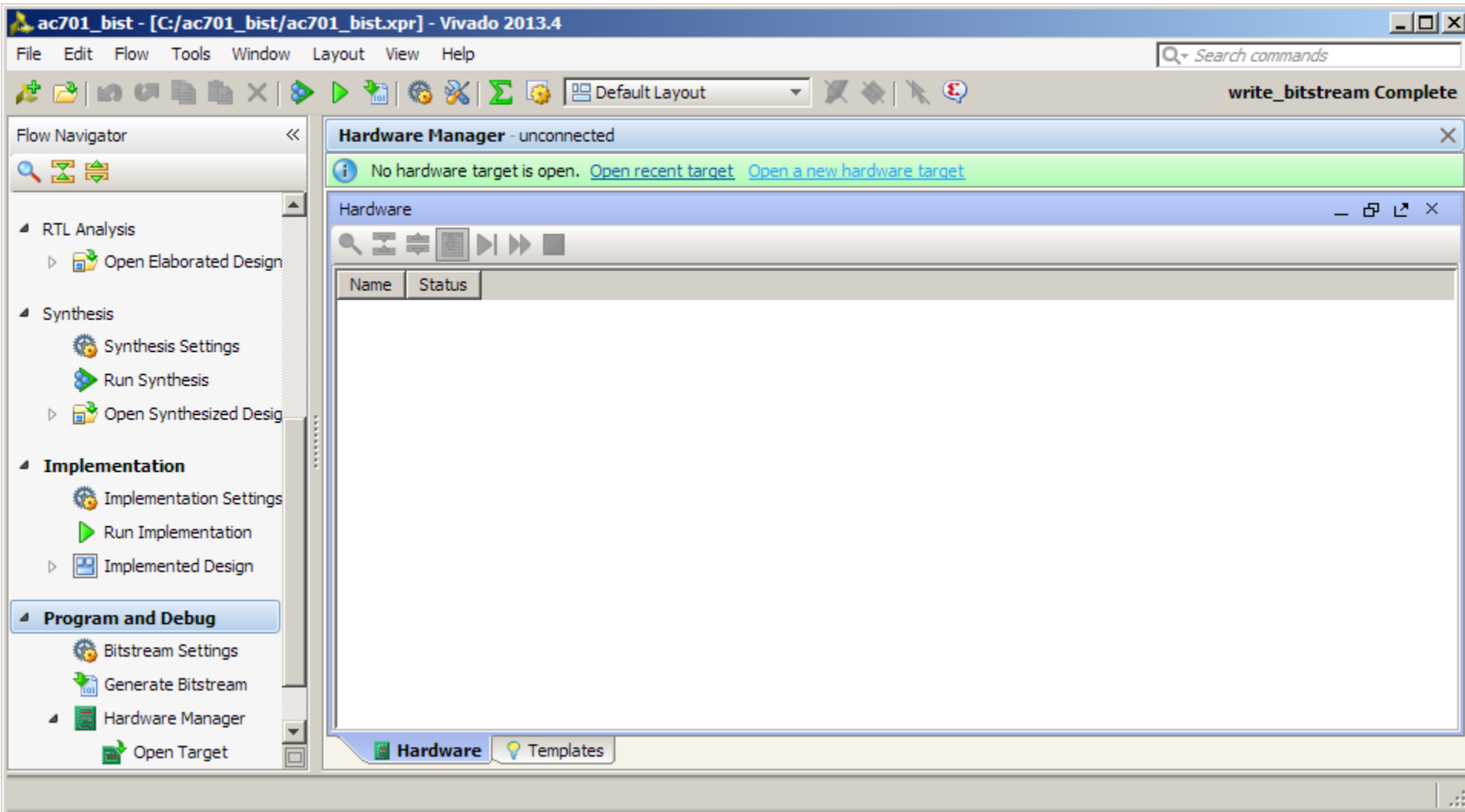
➤ Click Open Hardware Manager



Note: Presentation applies to the AC701

Program AC701 with BIST Design

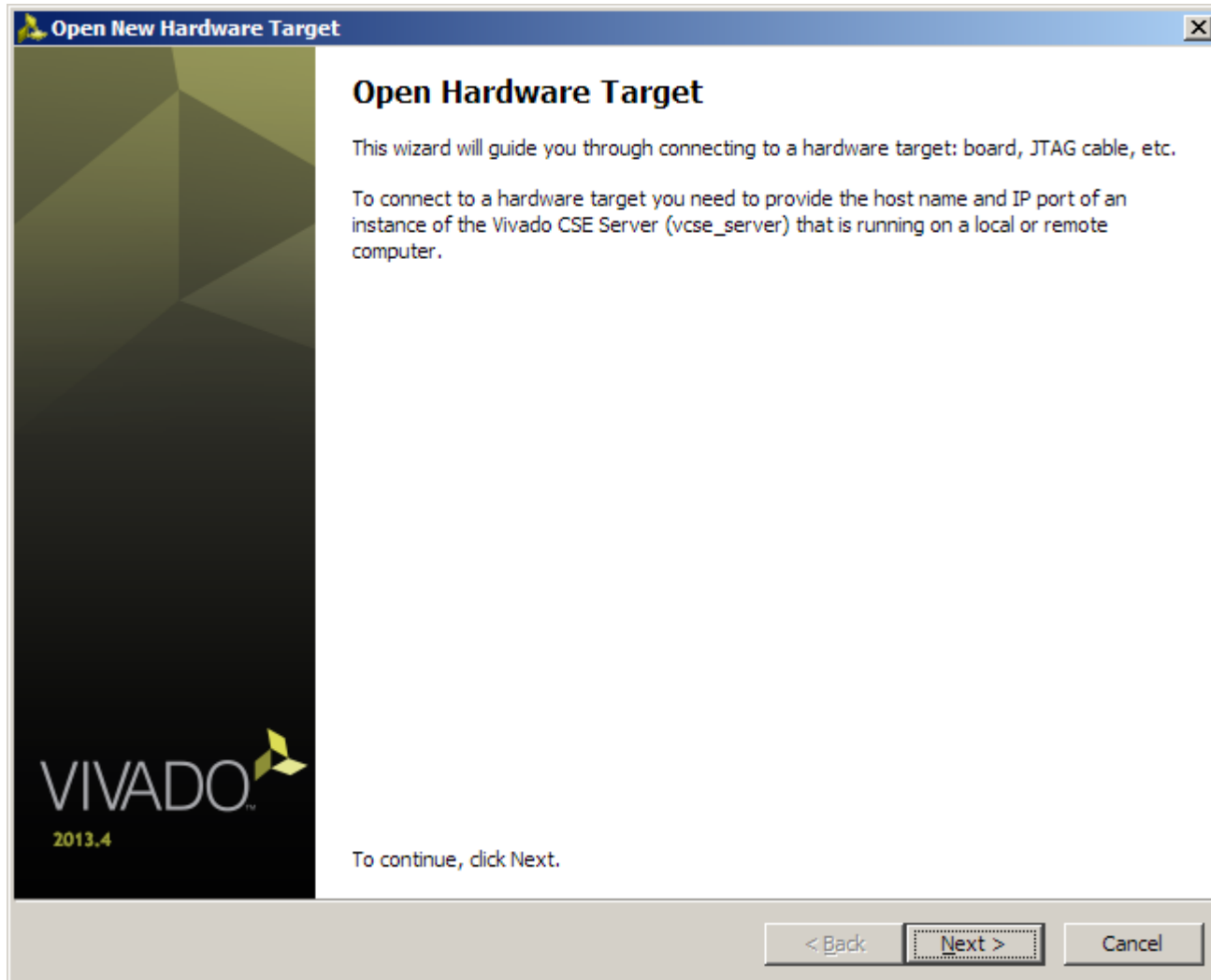
➤ Click Open a new hardware target



Note: Presentation applies to the AC701

Program AC701 with BIST Design

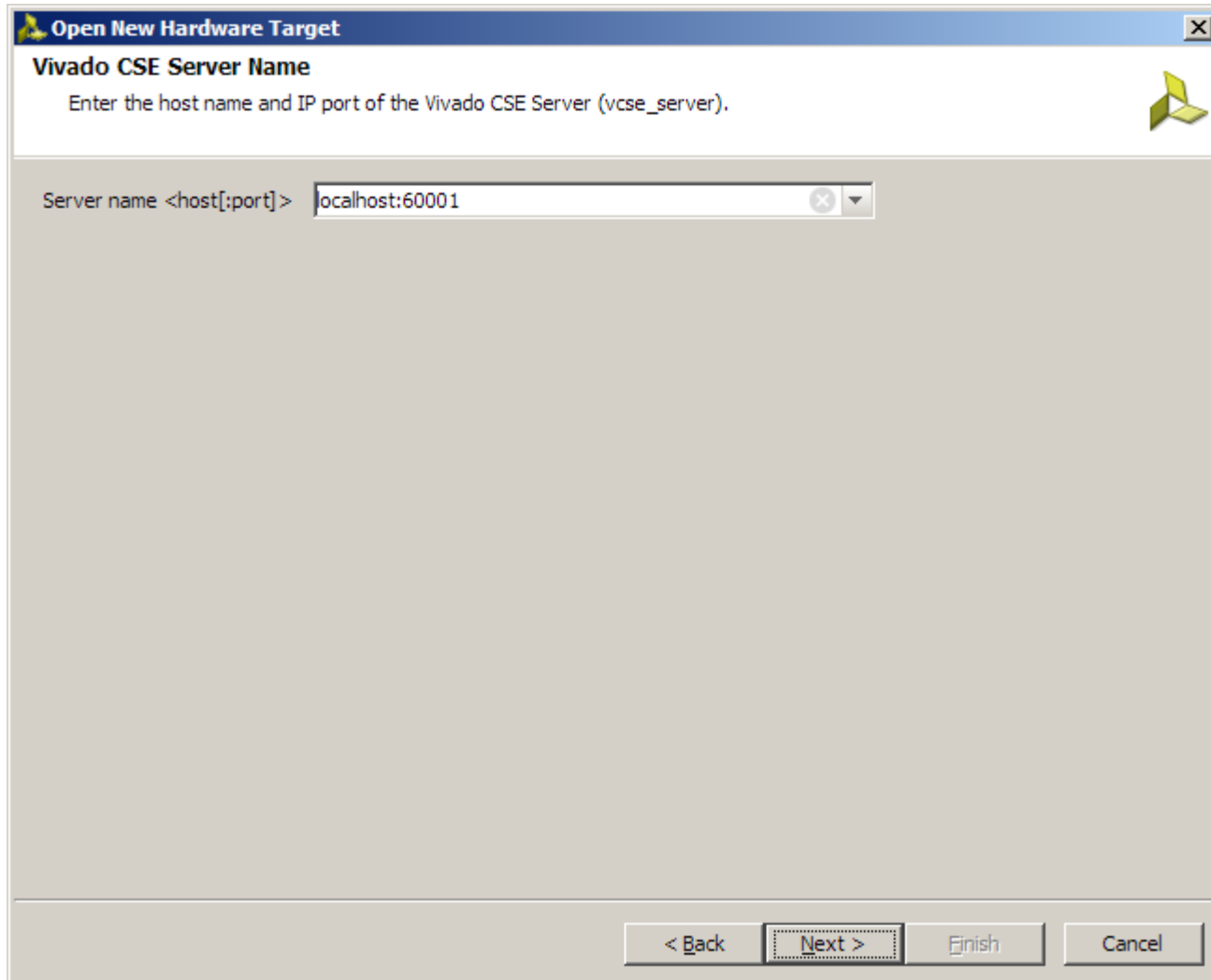
➤ Click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

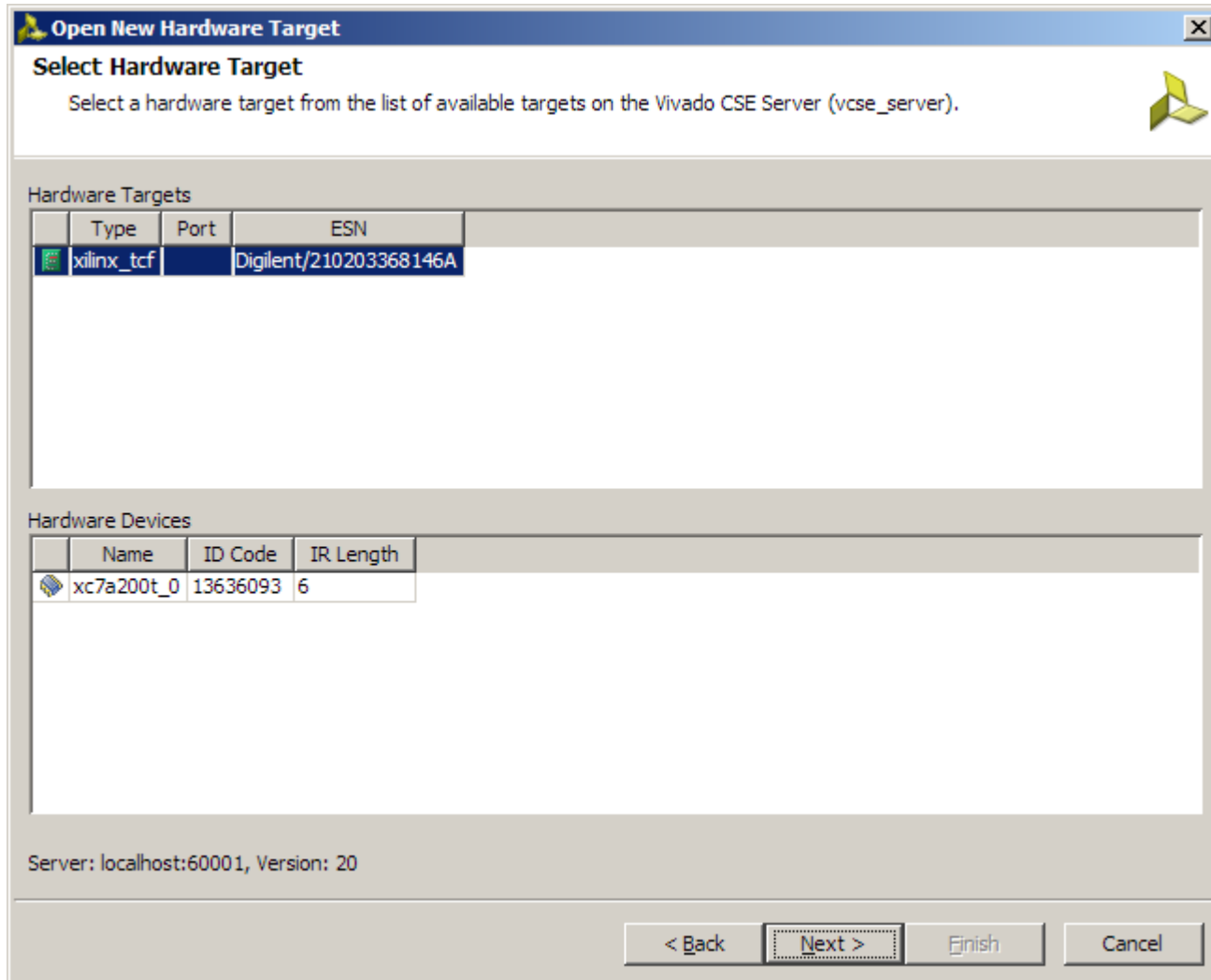
➤ Click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

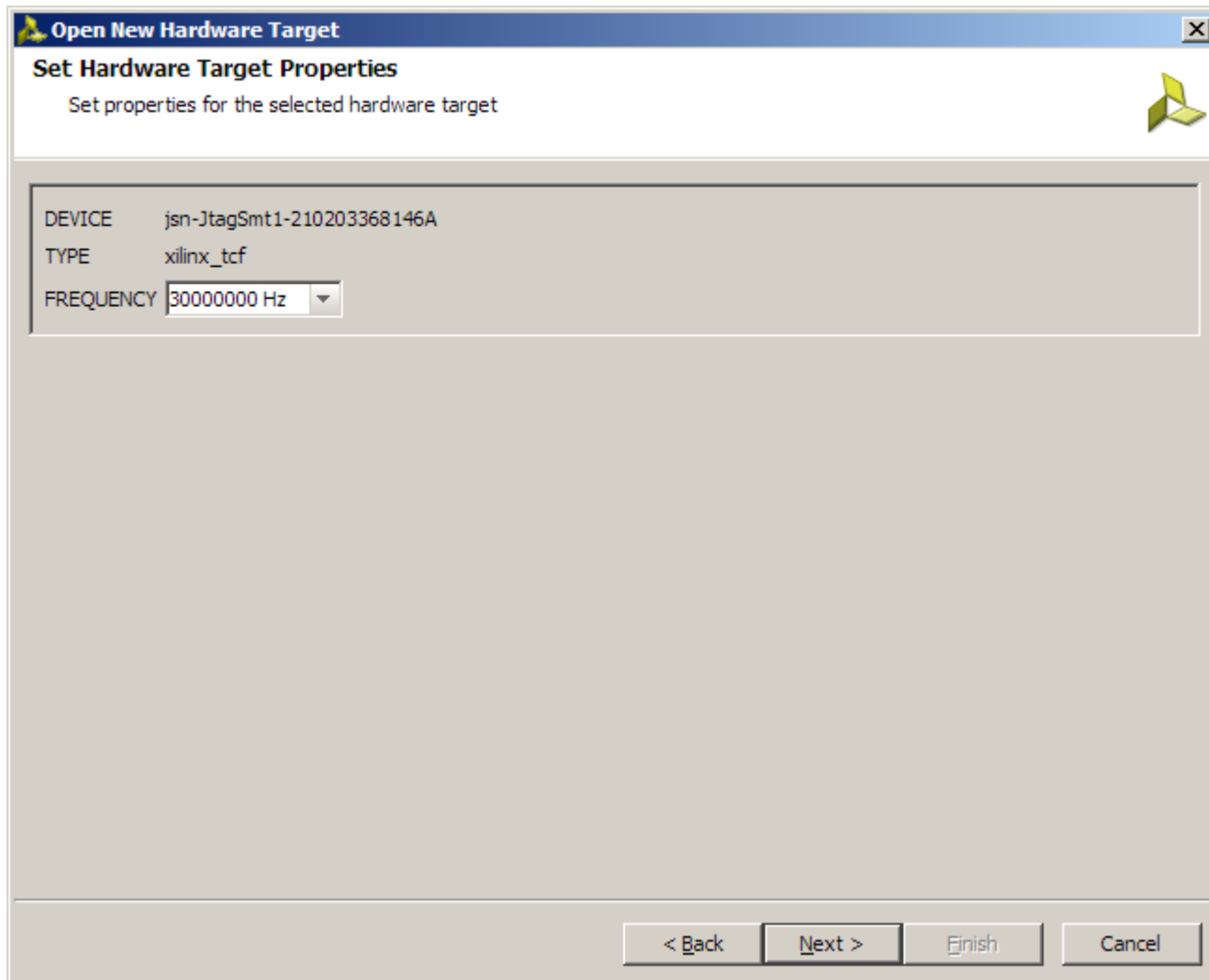
➤ Click Next



Note: Presentation applies to the AC701

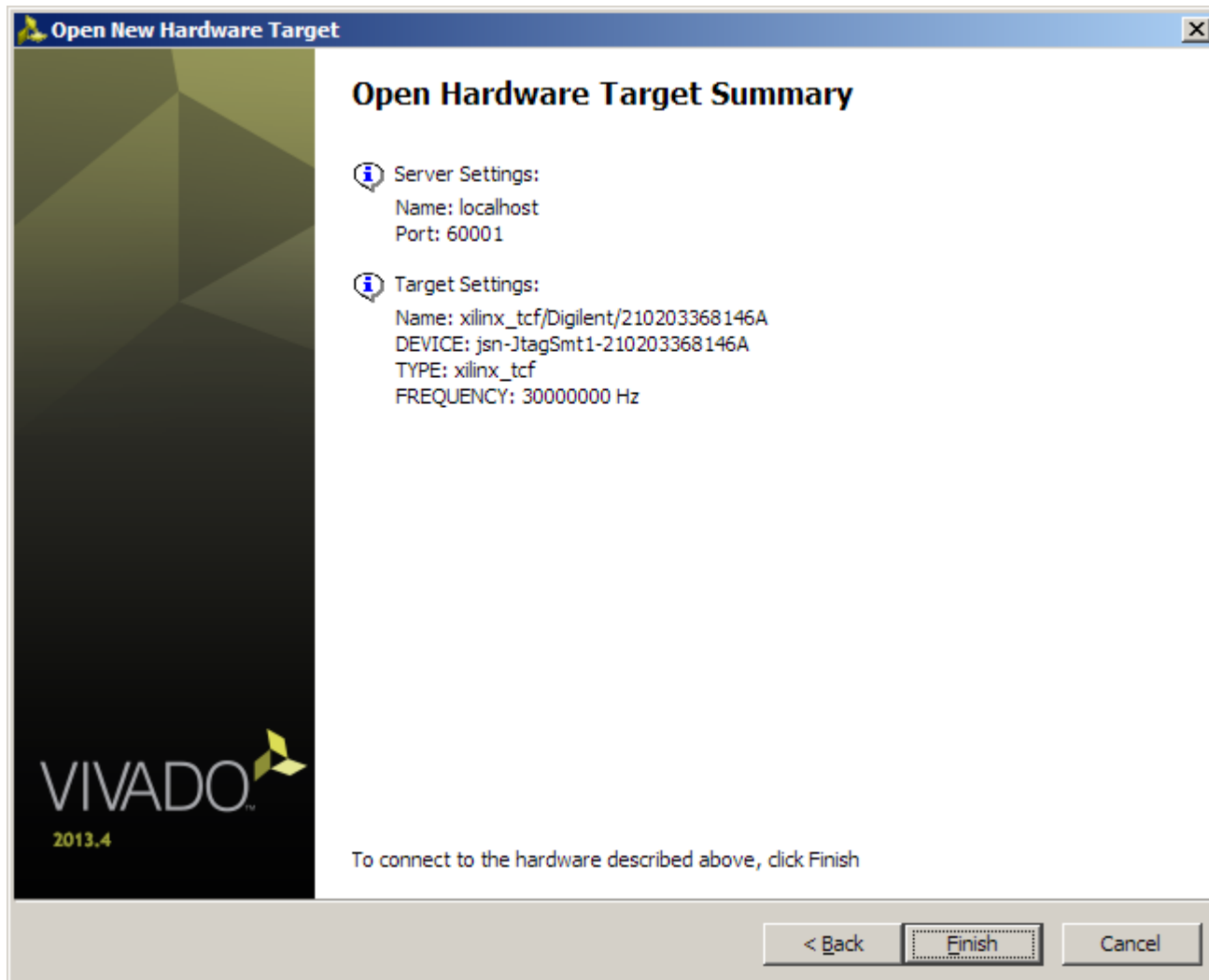
Program AC701 with BIST Design

- Set the FREQUENCY to 30000000 Hz (30 MHz) and click Next



Program AC701 with BIST Design

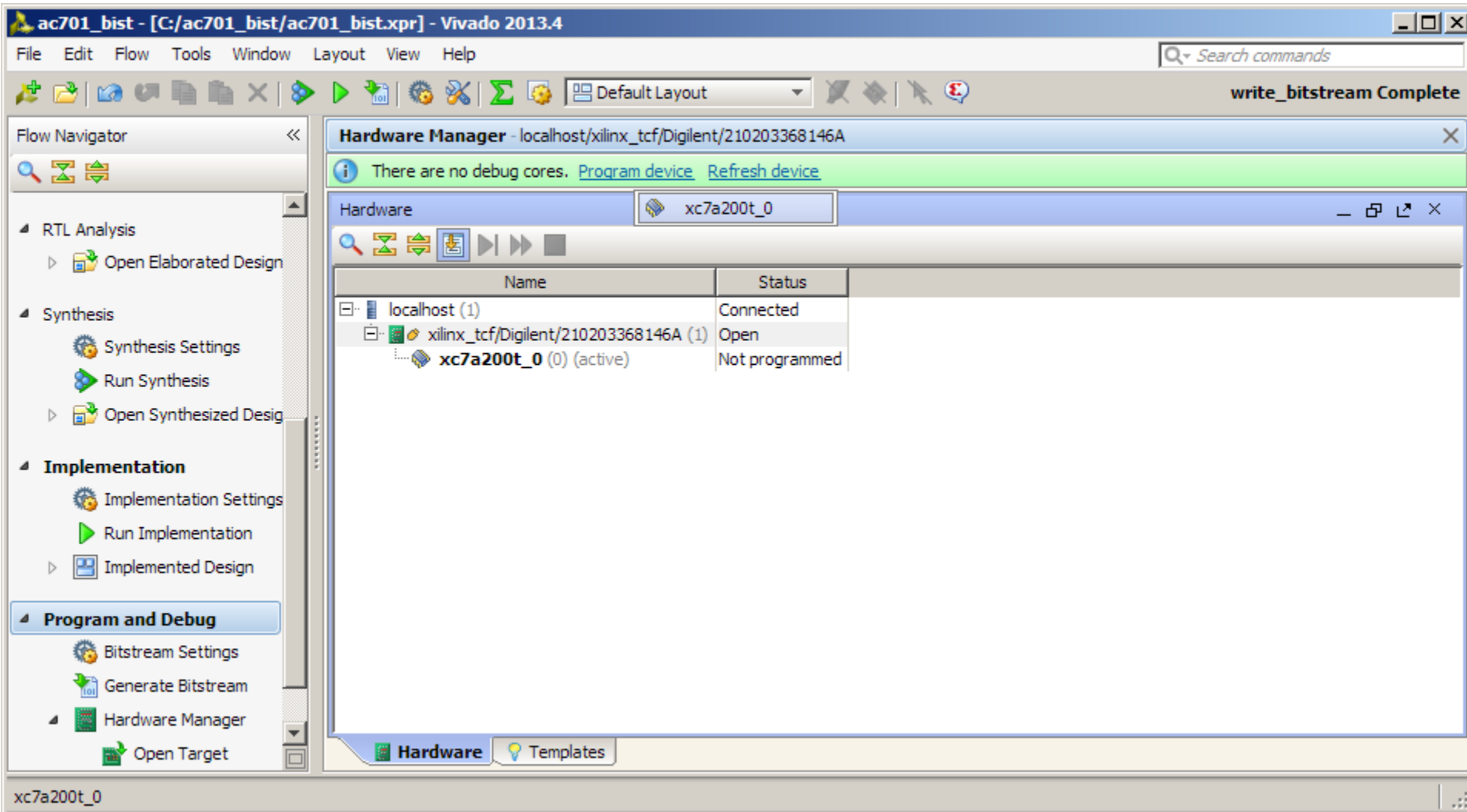
➤ Click Finish



Note: Presentation applies to the AC701

Program AC701 with BIST Design

➤ Select Program device → xc7a200t_0



The screenshot shows the Vivado 2013.4 interface. The title bar reads "ac701_bist - [C:/ac701_bist/ac701_bist.xpr] - Vivado 2013.4". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A search bar for commands is visible. The Flow Navigator on the left shows the "Program and Debug" section selected, with "Hardware Manager" highlighted. The Hardware Manager window displays the following information:

Hardware Manager - localhost/xilinx_tcf/Digilent/210203368146A

There are no debug cores. [Program device](#) [Refresh device](#)

Hardware: xc7a200t_0

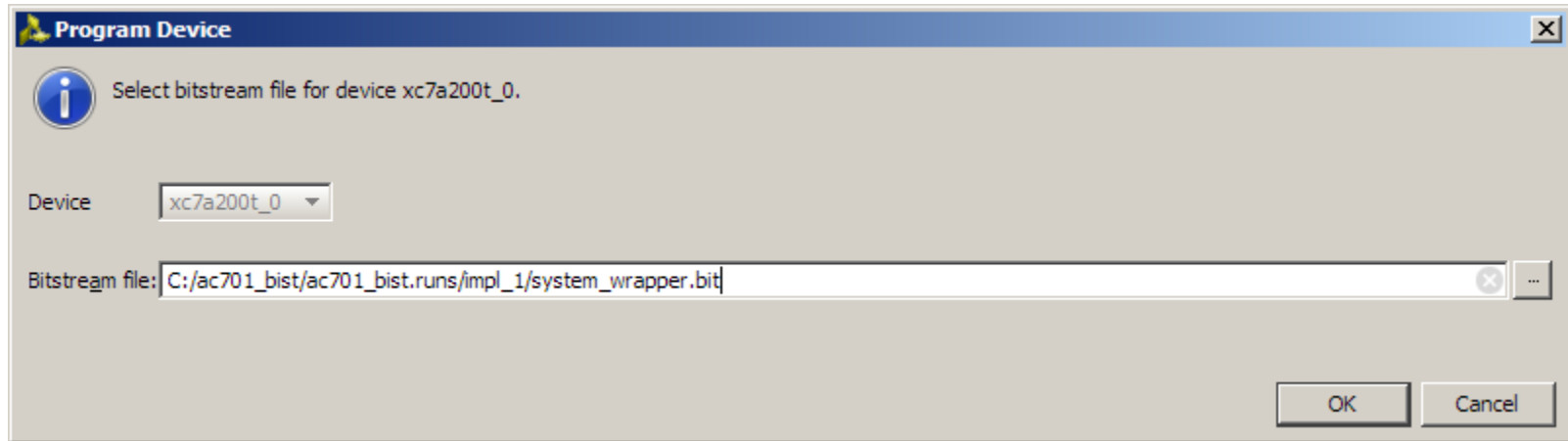
Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210203368146A (1)	Open
xc7a200t_0 (0) (active)	Not programmed

The status bar at the bottom shows "xc7a200t_0".

Note: Presentation applies to the AC701

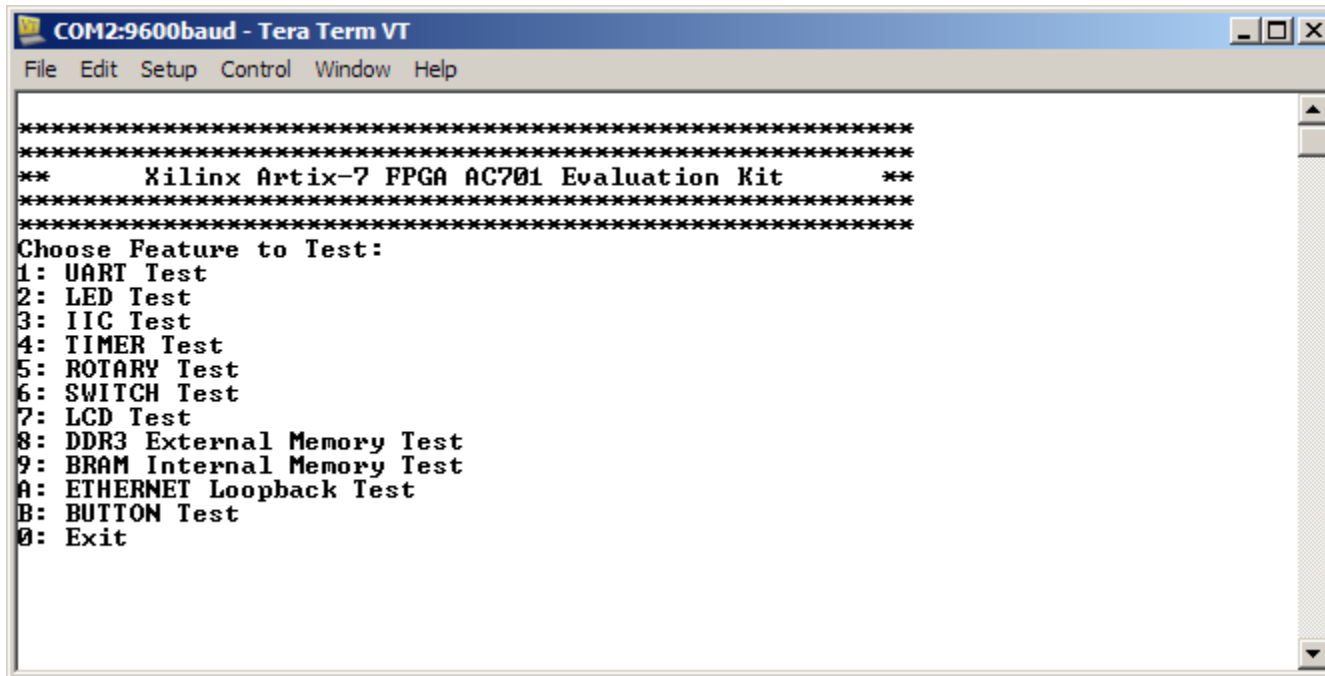
Program AC701 with BIST Design

- Program Device defaults to impl_1 bitstream
- Click Program



Program AC701 with BIST Design

➤ BIST Application runs in the terminal window



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
*****
*****
**      Xilinx Artix-7 FPGA AC701 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
```

Program AC701 with BIST Design

➤ Close the Server

- Closing the localhost server allows access by a different Vivado instance

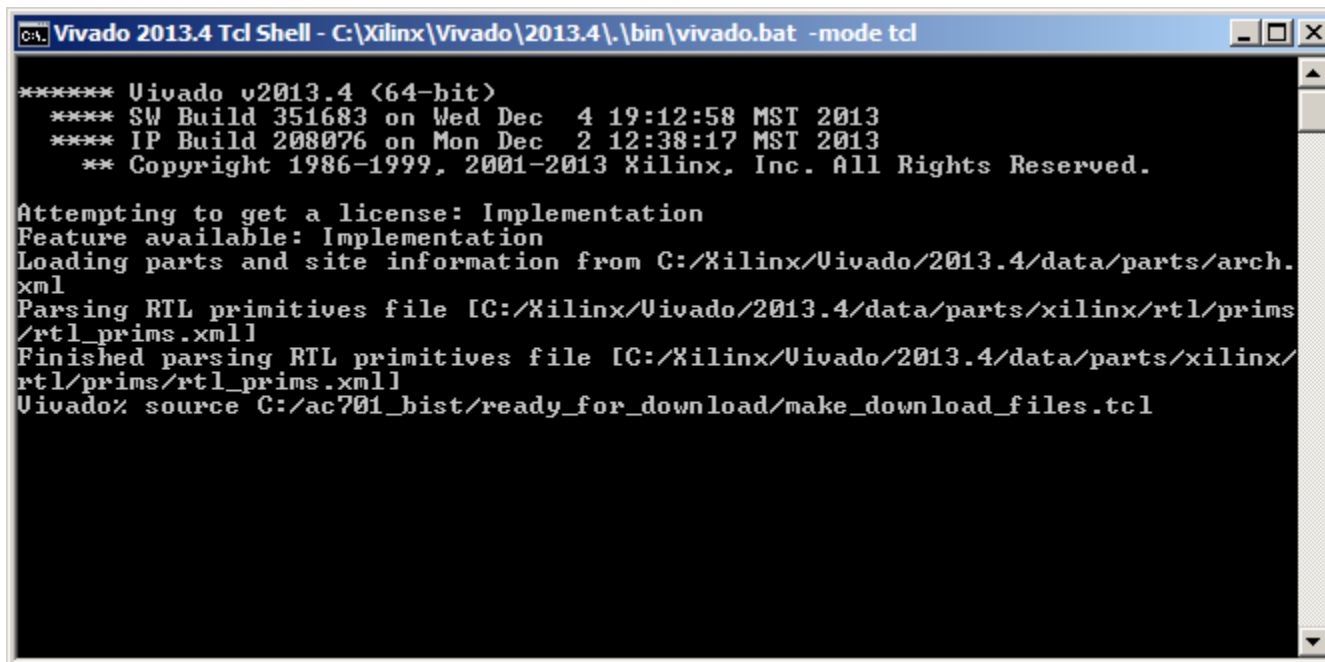
The screenshot shows the Vivado 2013.4 interface. The title bar reads "ac701_bist - [C:/ac701_bist/ac701_bist.xpr] - Vivado 2013.4". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A search bar for commands is visible. The Flow Navigator on the left shows the "Program and Debug" section expanded, with "Hardware Manager" selected. The Hardware Manager window displays a table of hardware components:

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210203368146A (1)	Open
xc7a200t_0 (0) (active)	Programmed

A context menu is open over the "localhost (1)" entry, showing options: "Hardware Server Properties..." (Ctrl+E), "Refresh Server", "Close Server" (highlighted), and "Export to Spreadsheet...". A status bar at the bottom of the Hardware Manager window shows "Close hardware server".

Program AC701 with BIST Design

- Repeat this process using Tcl scripts
- Open a Vivado Tcl shell and type:
 - source C:/ac701_bist/ready_for_download/make_download_files.tcl
- This script uses Tcl commands to add the ELF files to the BIST project , then generate both the BIST and LwIP bitstreams



```
C:\Xilinx\Vivado\2013.4\bin\vivado.bat -mode tcl

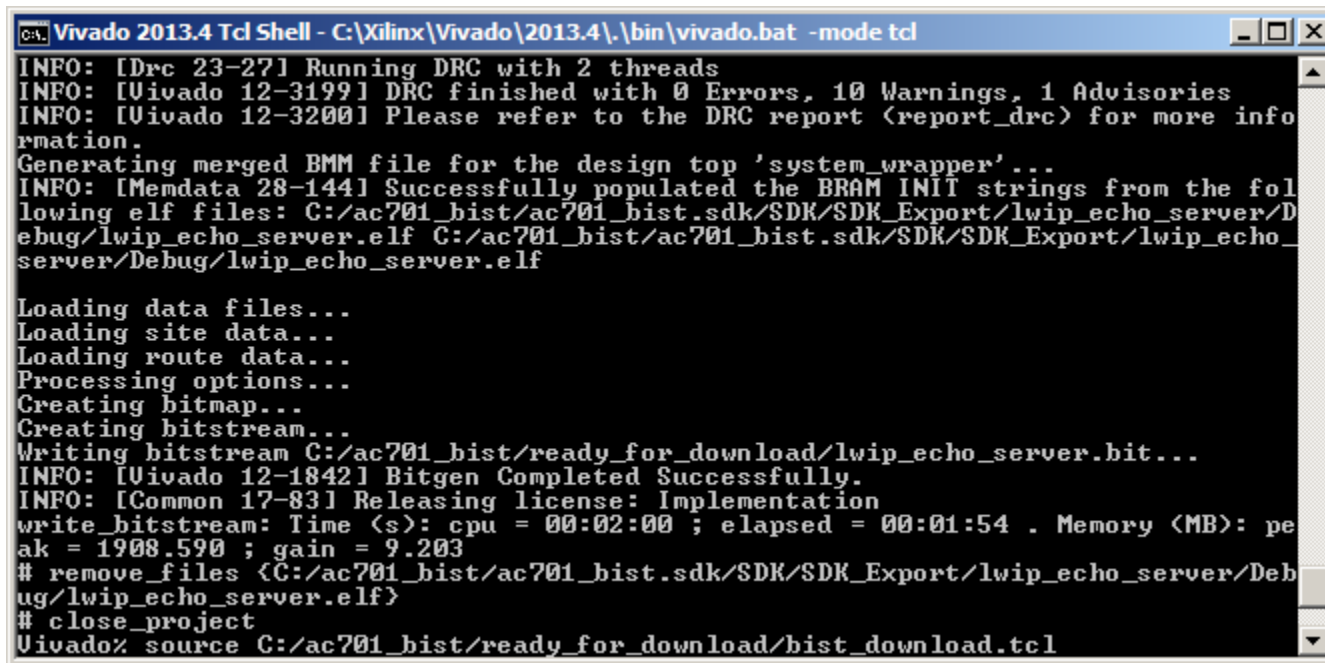
***** Uivado v2013.4 (64-bit)
**** SW Build 351683 on Wed Dec  4 19:12:58 MST 2013
**** IP Build 208076 on Mon Dec  2 12:38:17 MST 2013
** Copyright 1986-1999, 2001-2013 Xilinx, Inc. All Rights Reserved.

Attempting to get a license: Implementation
Feature available: Implementation
Loading parts and site information from C:/Xilinx/Vivado/2013.4/data/parts/arch.xml
Parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Finished parsing RTL primitives file [C:/Xilinx/Vivado/2013.4/data/parts/xilinx/rtl/prims/rtl_prims.xml]
Vivado% source C:/ac701_bist/ready_for_download/make_download_files.tcl
```

Program AC701 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:

source C:/ac701_bist/ready_for_download/bist_download.tcl

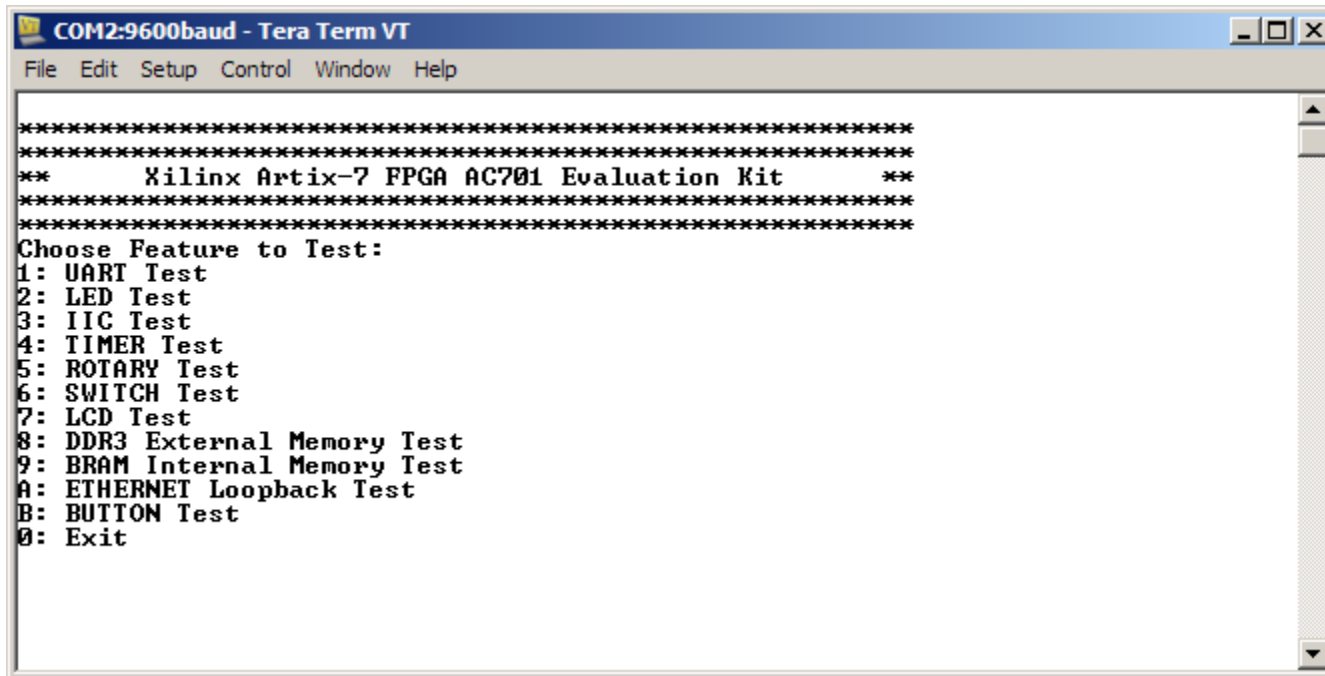


```
C:\Xilinx\Vivado\2013.4\bin\vivado.bat -mode tcl
INFO: [Drc 23-27] Running DRC with 2 threads
INFO: [Uvivo 12-3199] DRC finished with 0 Errors, 10 Warnings, 1 Advisories
INFO: [Uvivo 12-3200] Please refer to the DRC report (report_drc) for more information.
Generating merged BMM file for the design top 'system_wrapper'...
INFO: [Memdata 28-144] Successfully populated the BRAM INIT strings from the following elf files: C:/ac701_bist/ac701_bist.sdk/SDK/SDK_Export/lwip_echo_server/Debug/lwip_echo_server.elf C:/ac701_bist/ac701_bist.sdk/SDK/SDK_Export/lwip_echo_server/Debug/lwip_echo_server.elf

Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream C:/ac701_bist/ready_for_download/lwip_echo_server.bit...
INFO: [Uvivo 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
write_bitstream: Time (s): cpu = 00:02:00 ; elapsed = 00:01:54 . Memory (MB): peak = 1908.590 ; gain = 9.203
# remove_files {C:/ac701_bist/ac701_bist.sdk/SDK/SDK_Export/lwip_echo_server/Debug/lwip_echo_server.elf}
# close_project
Vivado% source C:/ac701_bist/ready_for_download/bist_download.tcl
```

Program AC701 with BIST Design

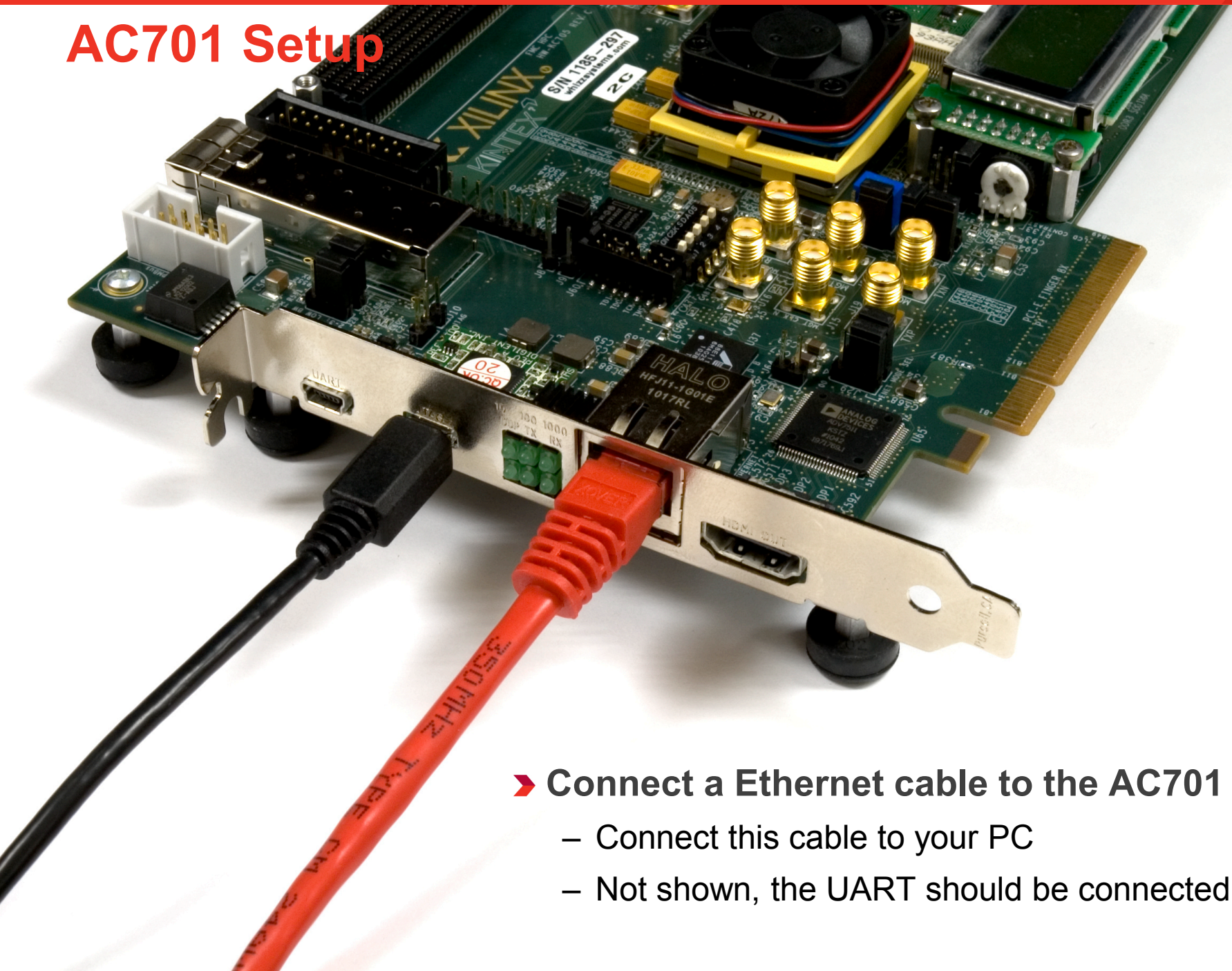
➤ BIST Application runs in the terminal window



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
*****
*****
**      Xilinx Artix-7 FPGA AC701 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: TIMER Test
5: ROTARY Test
6: SWITCH Test
7: LCD Test
8: DDR3 External Memory Test
9: BRAM Internal Memory Test
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
```

Run the LwIP Ethernet Design

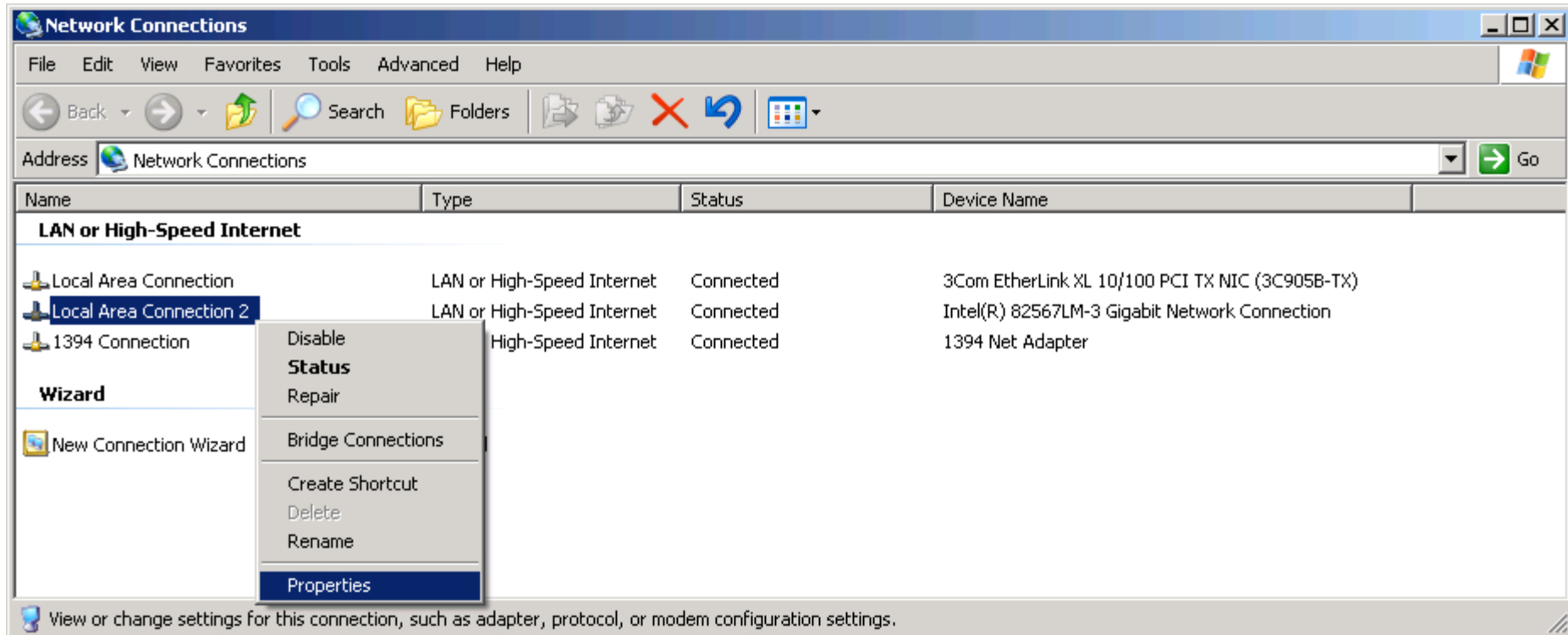
AC701 Setup



- **Connect a Ethernet cable to the AC701**
 - Connect this cable to your PC
 - Not shown, the UART should be connected

Run the LwIP Ethernet Design

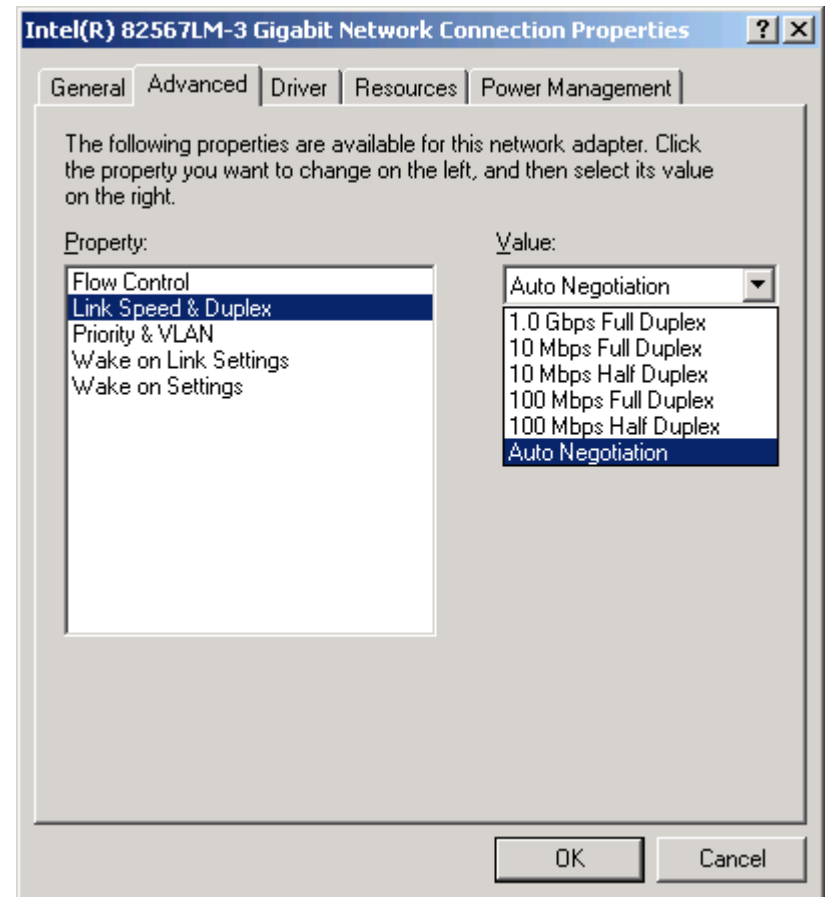
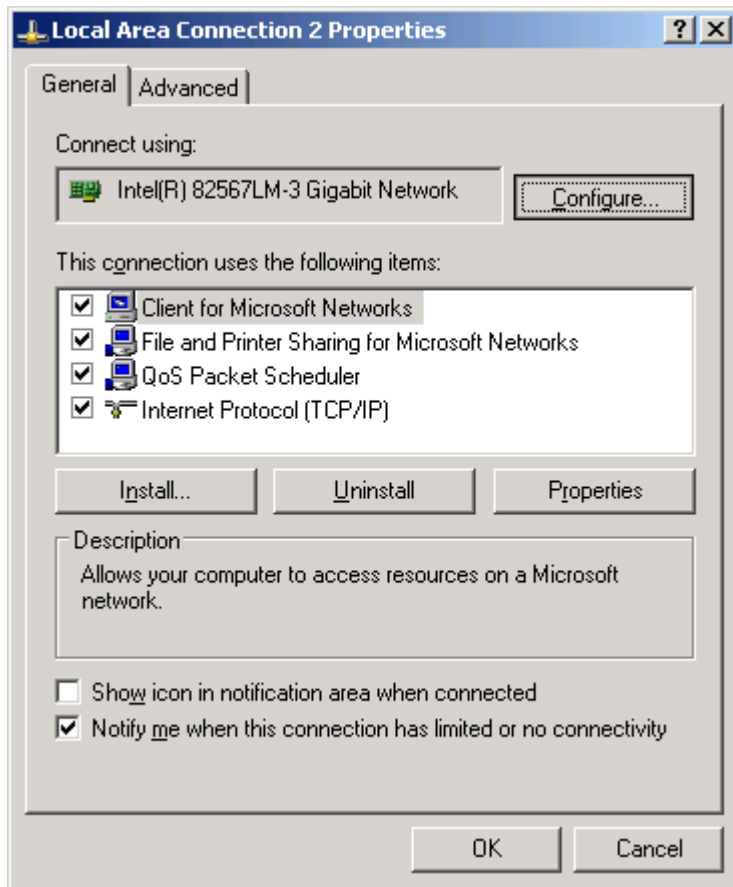
- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties



Run the LwIP Ethernet Design

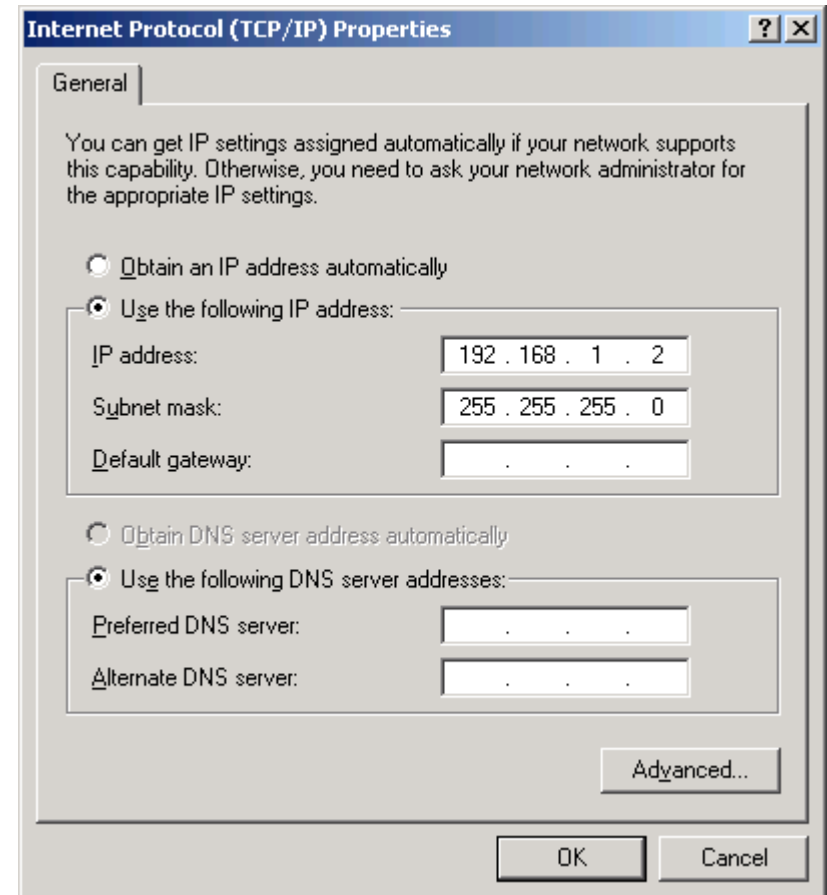
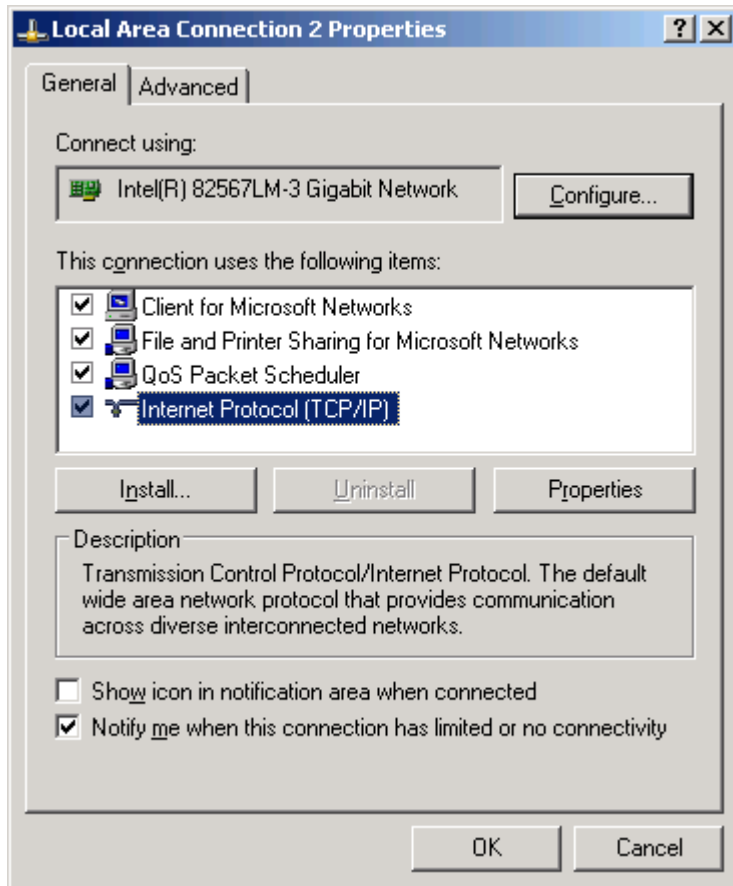
➤ Click Configure

- Set the Media Type to Auto for 1 Gbps then click OK



Run the LwIP Ethernet Design

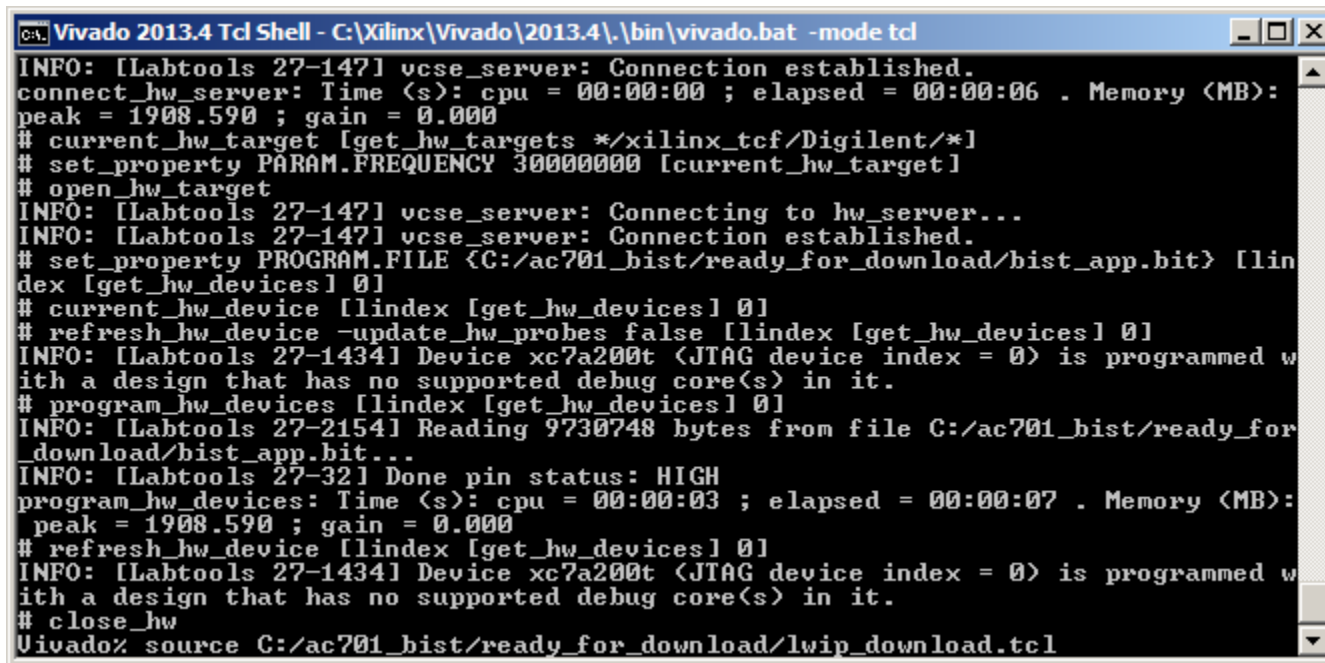
- Reopen the properties after the last step
- Set your host (PC) to this IP Address:



Run the LwIP Ethernet Design

- Download the LwIP bitstream
- In the Vivado Tcl Shell type:

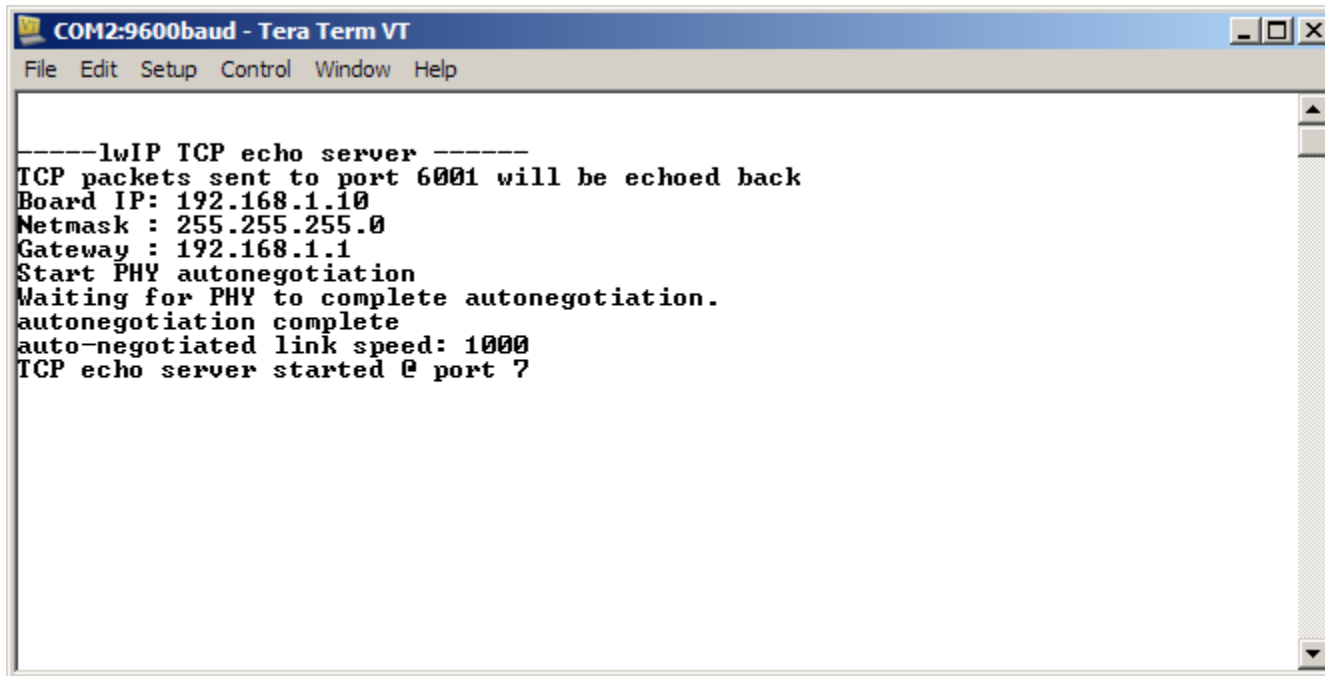
source C:/ac701_bist/ready_for_download/lwip_download.tcl



```
C:\Xilinx\Vivado\2013.4\bin\vivado.bat -mode tcl
INFO: [Labtools 27-147] vcse_server: Connection established.
connect_hw_server: Time (s): cpu = 00:00:00 ; elapsed = 00:00:06 . Memory (MB):
peak = 1908.590 ; gain = 0.000
# current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
# set_property PARAM.FREQUENCY 30000000 [current_hw_target]
# open_hw_target
INFO: [Labtools 27-147] vcse_server: Connecting to hw_server...
INFO: [Labtools 27-147] vcse_server: Connection established.
# set_property PROGRAM.FILE {C:/ac701_bist/ready_for_download/bist_app.bit} [lin
dex [get_hw_devices] 0]
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7a200t (JTAG device index = 0) is programmed w
ith a design that has no supported debug core(s) in it.
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-2154] Reading 9730748 bytes from file C:/ac701_bist/ready_for
_download/bist_app.bit...
INFO: [Labtools 27-321] Done pin status: HIGH
program_hw_devices: Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB):
peak = 1908.590 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7a200t (JTAG device index = 0) is programmed w
ith a design that has no supported debug core(s) in it.
# close_hw
Vivado% source C:/ac701_bist/ready_for_download/lwip_download.tcl
```

Run the LwIP Ethernet Design

➤ View LwIP echo server screen



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help

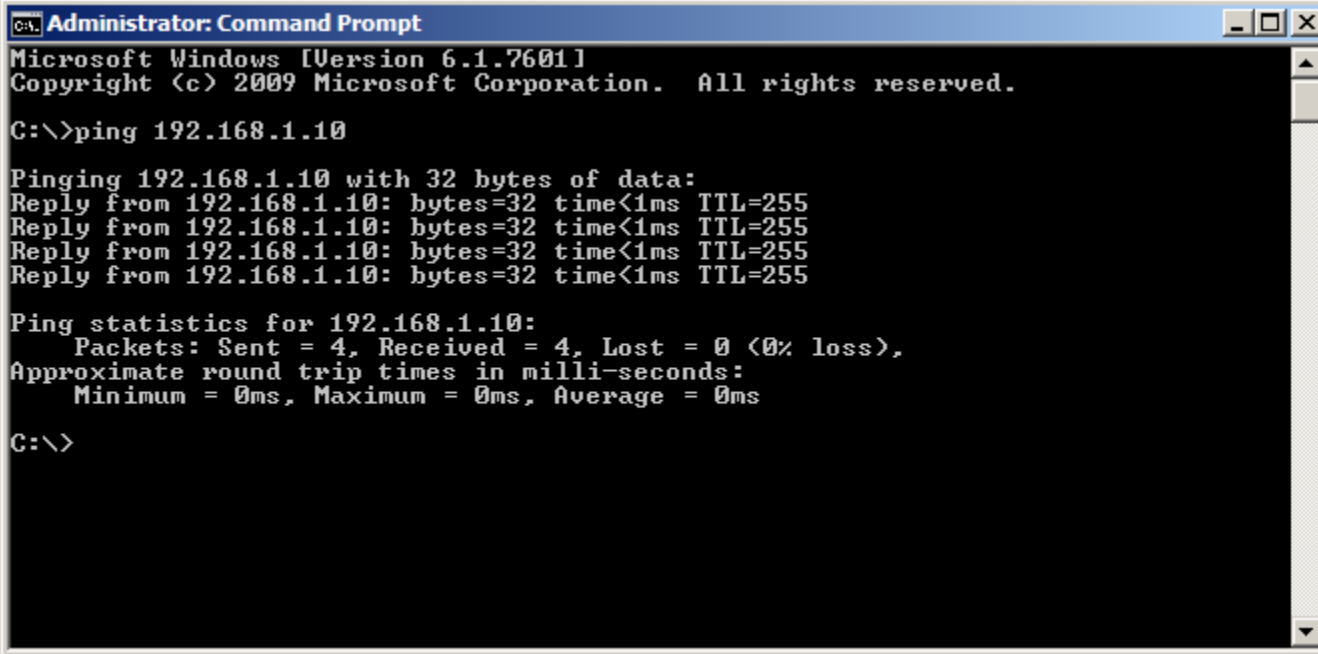
-----lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
auto-negotiated link speed: 1000
TCP echo server started @ port 7
```

Run the LwIP Ethernet Design

➤ From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

– Ping from PC host 192.168.1.2 to AC701 target 192.168.1.10



```
Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\>
```



References

References

➤ IP Integrator Documentation

- Vivado Design Suite Tcl Command Reference Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_3/ug835-vivado-tcl-commands.pdf
- Designing IP Subsystems Using IP Integrator
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_3/ug994-vivado-ip-subsystems.pdf
- IP Release Notes Guide
 - http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

➤ 7 Series Configuration

- 7 Series FPGAs Configuration User Guide
 - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Documentation

Documentation

➤ Artix-7

- Artix-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm>
- Design Advisory Master Answer Record for Artix-7 FPGAs
 - <http://www.xilinx.com/support/answers/51456.htm>

➤ AC701 Documentation

- Artix-7 FPGA AC701 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/EK-A7-AC701-G.htm>
- AC701 Getting Started Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/2013_2/ug967-ac701-eval-kit-getting-started.pdf
- AC701 User Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/ug952-ac701-a7-eval-bd.pdf