AC701 Built-In Self Test Flash Application

December 2013

XTP194

Revision History

Date	Version	Description
12/18/13	6.0	Recompiled for 2013.4.
10/23/13	5.0	Recompiled for 2013.3. Converted to IPI, added RGMII interface and LwIP.
06/19/13	4.0	Recompiled for 2013.2. AR55431, AR55531 and AR55738 fixed.
04/03/13	3.0	Recompiled for 2013.1. Added AR55431, AR55531 and AR55738. AR53420 Fixed.
02/04/13	2.1	As per AR54044, added 2012.4 device pack. Added AR53420 and AR54223.
12/18/12	2.0	Recompiled for 2012.4
10/23/12	1.0	Initial Version.

Overview

- Xilinx AC701 Board
- Software Requirements
- AC701 Setup
- AC701 BIST (Built-In Self Test)
- Compile AC701 BIST Design
- Program AC701 with BIST Design
- Run the LwIP Ethernet Design
- References
  - IP Release Notes Guide XTP025

Note: This presentation applies to the AC701

AC701 BIST Design Description

- **Description**
  - The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.
- **Block Design Source**
  - RDF0220 - AC701 BIST Design Files (2013.4 C) zip file
  - Available through http://www.xilinx.com/ac701

Note: Presentation applies to the AC701

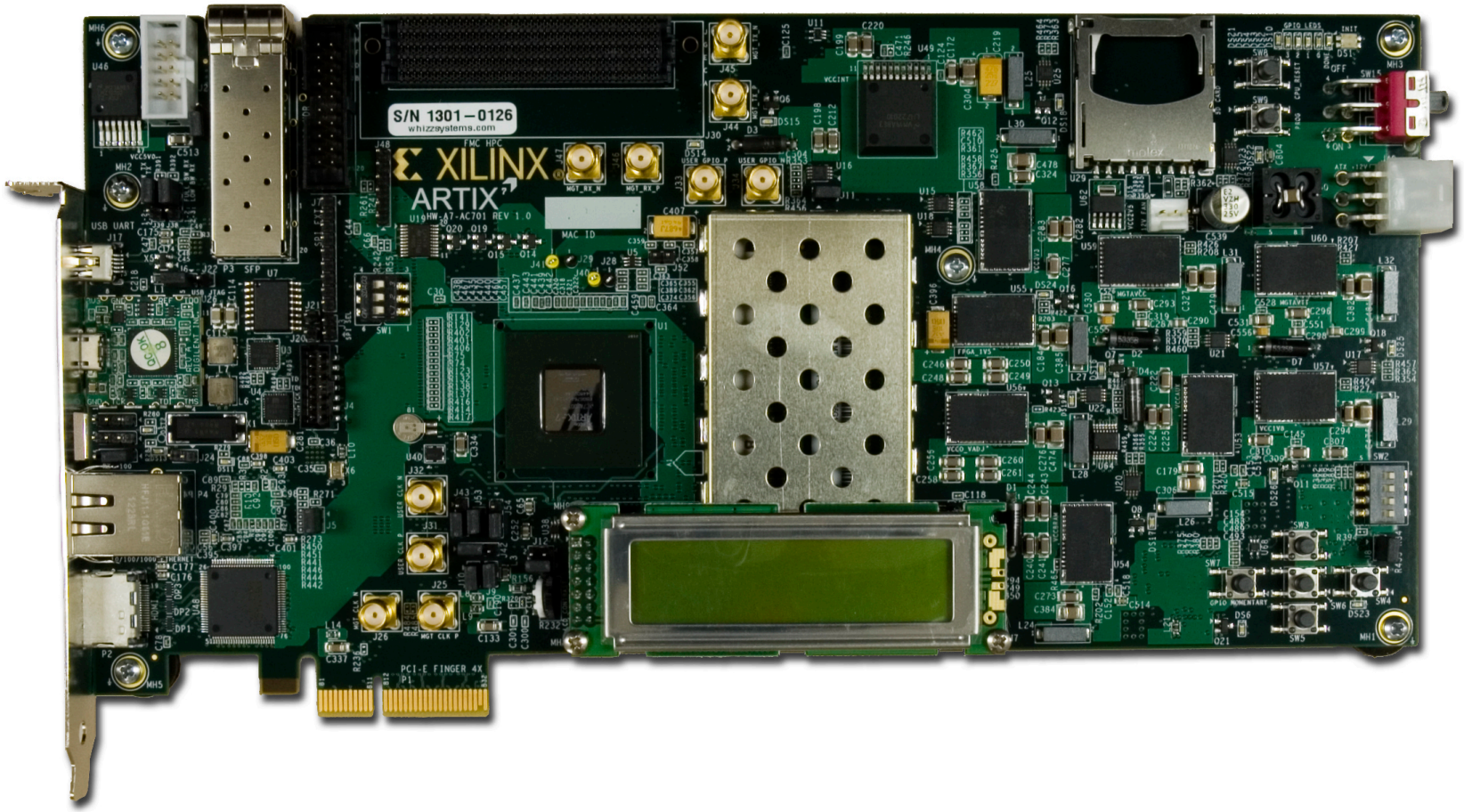
AC701 BIST Design Description

Block Design IP

- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus, LMB BRAM Controller, Block Memory Generator, Proc Sys Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect, AXI Timer
- Memory: AXI BRAM Controller, MIG 7 Series, AXI DMA
- Peripherals: AXI Ethernet, AXI IIC, AXI GPIO, AXI UART 16550, XADC Wizard
- Other IP: Clocking Wizard, Constant, Concat, gte2_top
  - Vivado Design Suite Tcl Command Reference Guide (UG835)
  - Designing IP Subsystems Using IP Integrator (UG994)

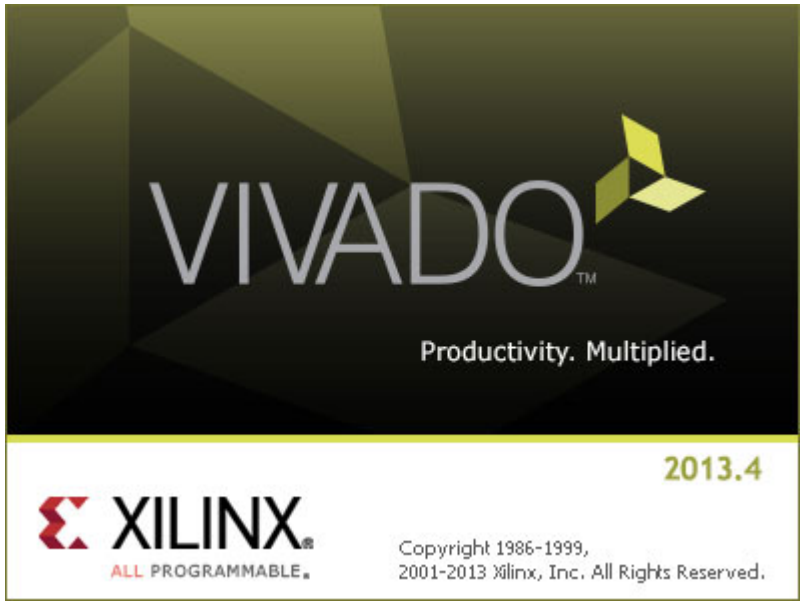
Note: Presentation applies to the AC701

Xilinx AC701 Board



Vivado Software Requirements

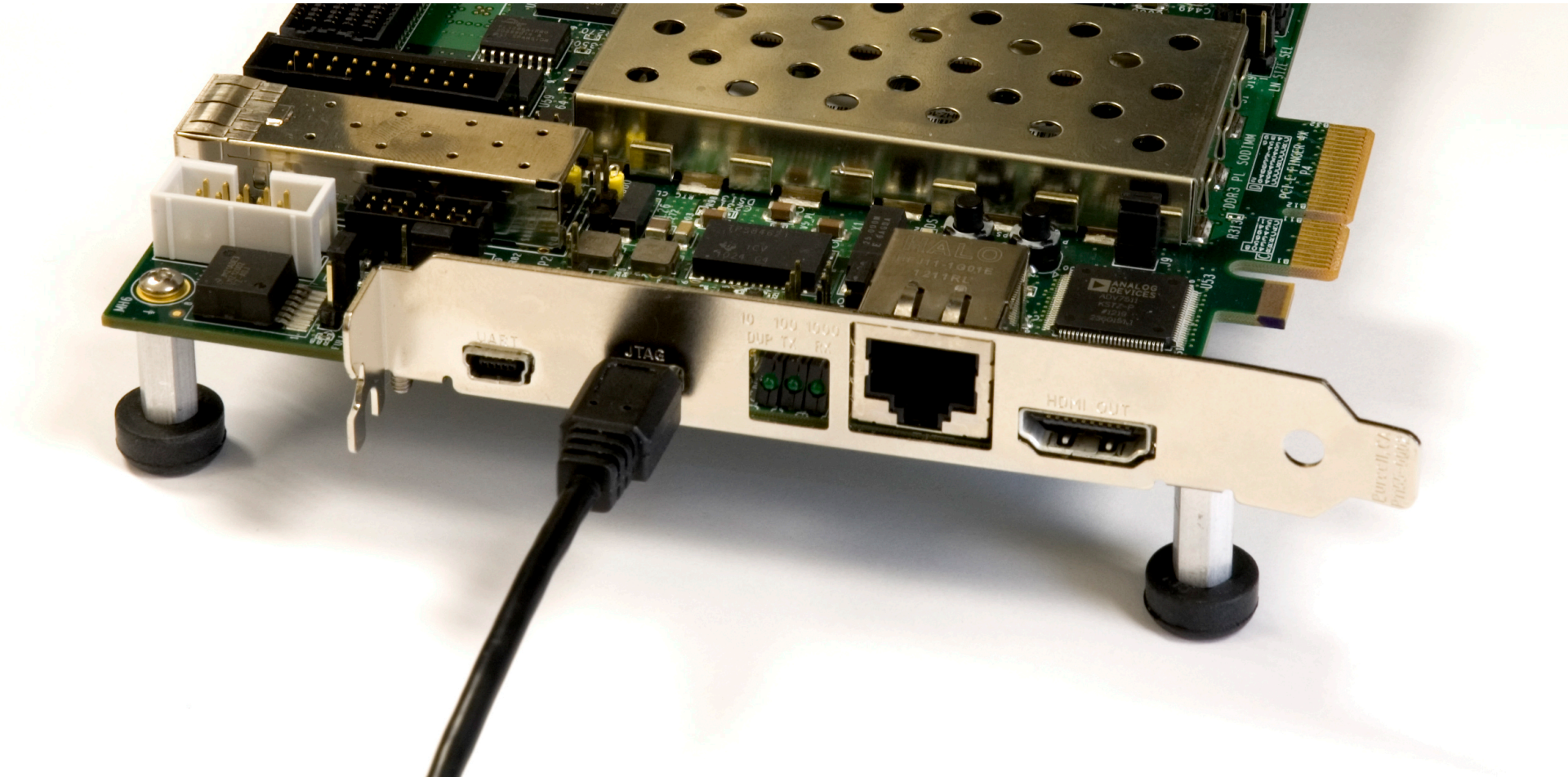
- **Xilinx Vivado Design Suite 2013.4, Design Edition + SDK**
  - Combined installer



Note: Presentation applies to the AC701

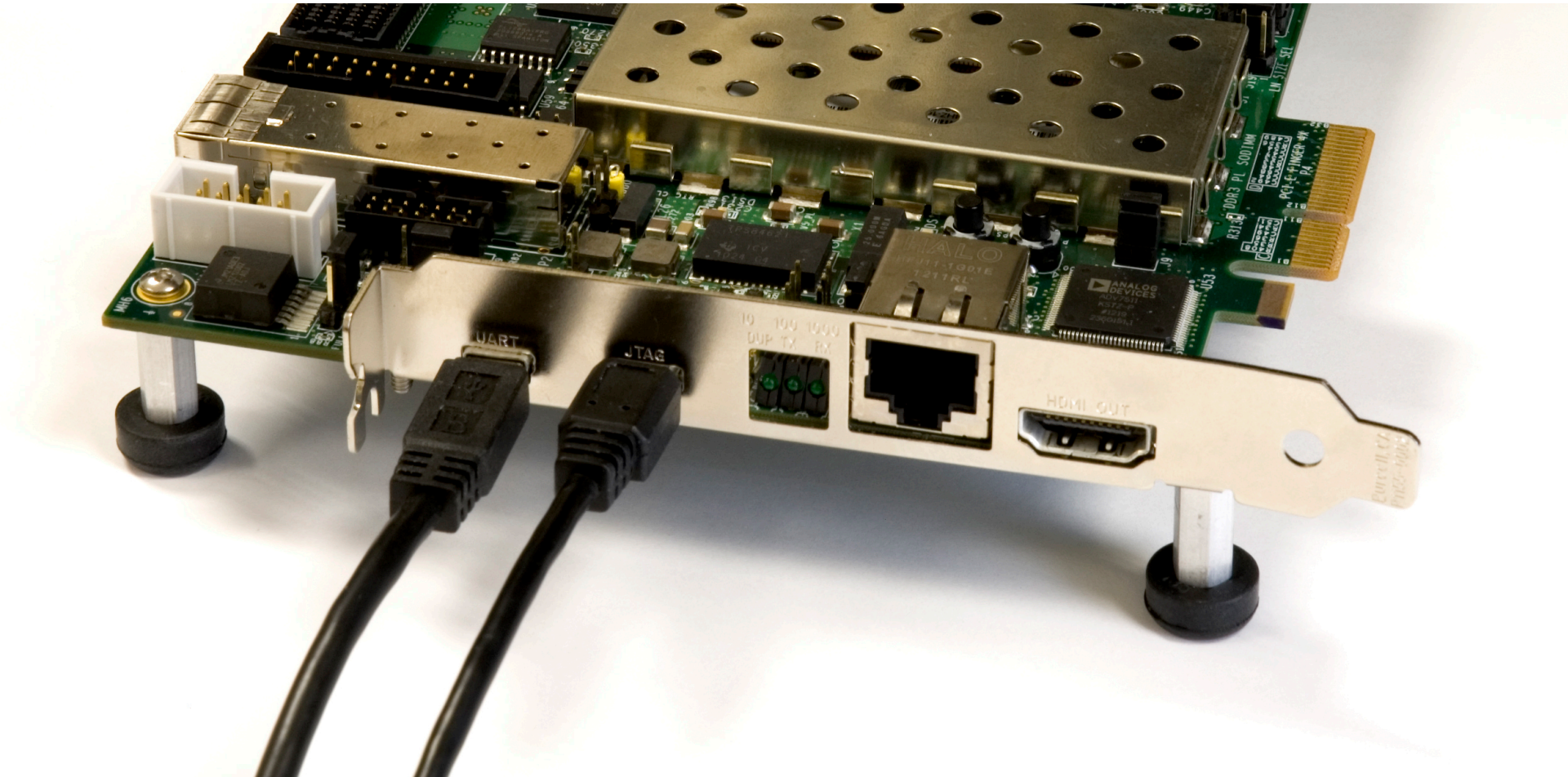
AC701 Setup

- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board**
  - Connect this cable to your PC



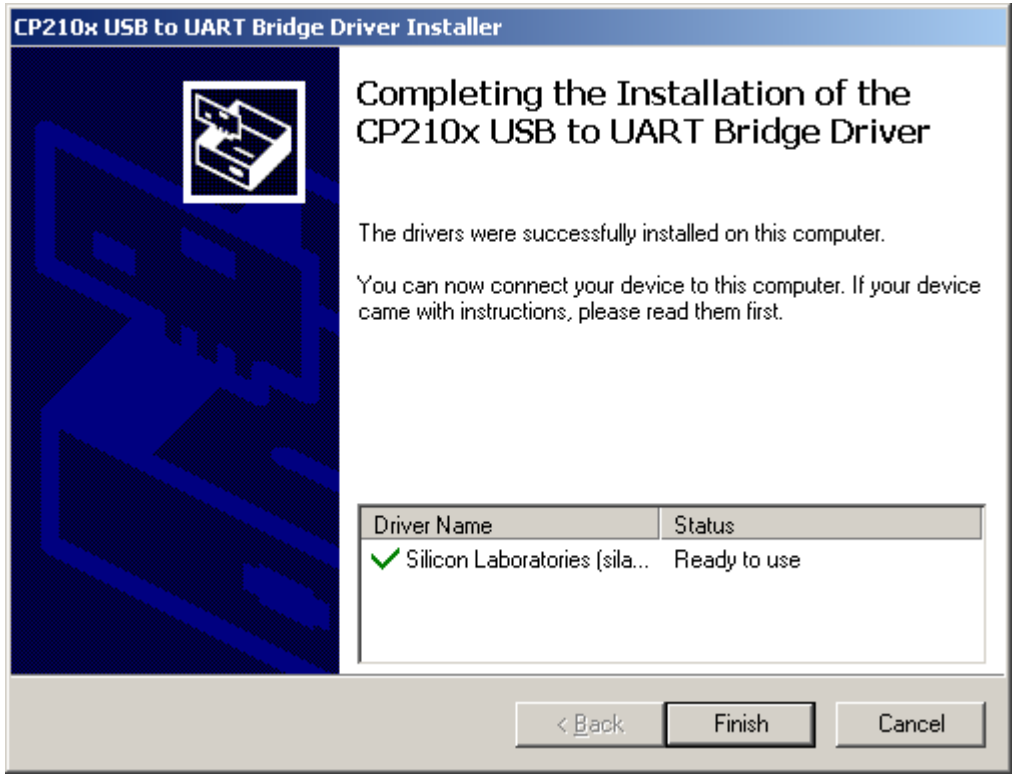
AC701 Setup

- **Connect a USB Type-A to Mini-B cable to the USB UART connector on the AC701 board**
  - Connect this cable to your PC
  - Power on the AC701 board for UART Drivers Installation



AC701 Setup

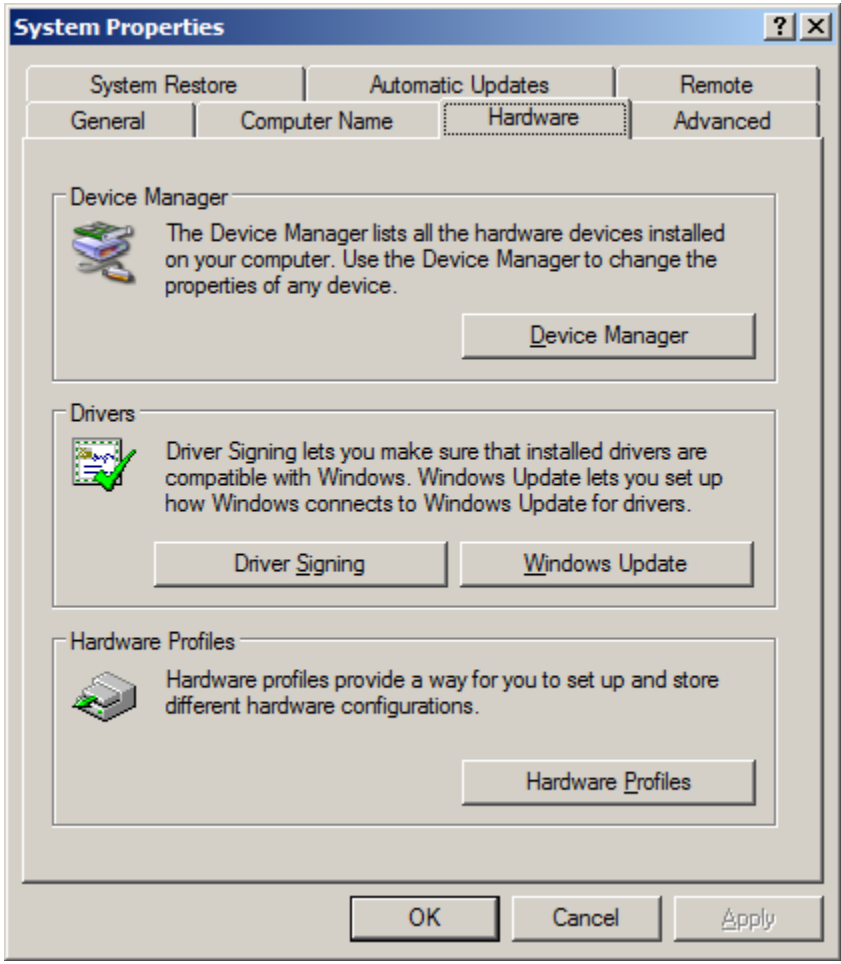
- **Install USB UART Drivers**
  - Go to http://www.silabs.com
  - Search for Virtual port drivers



Note: Presentation applies to the AC701

AC701 Setup

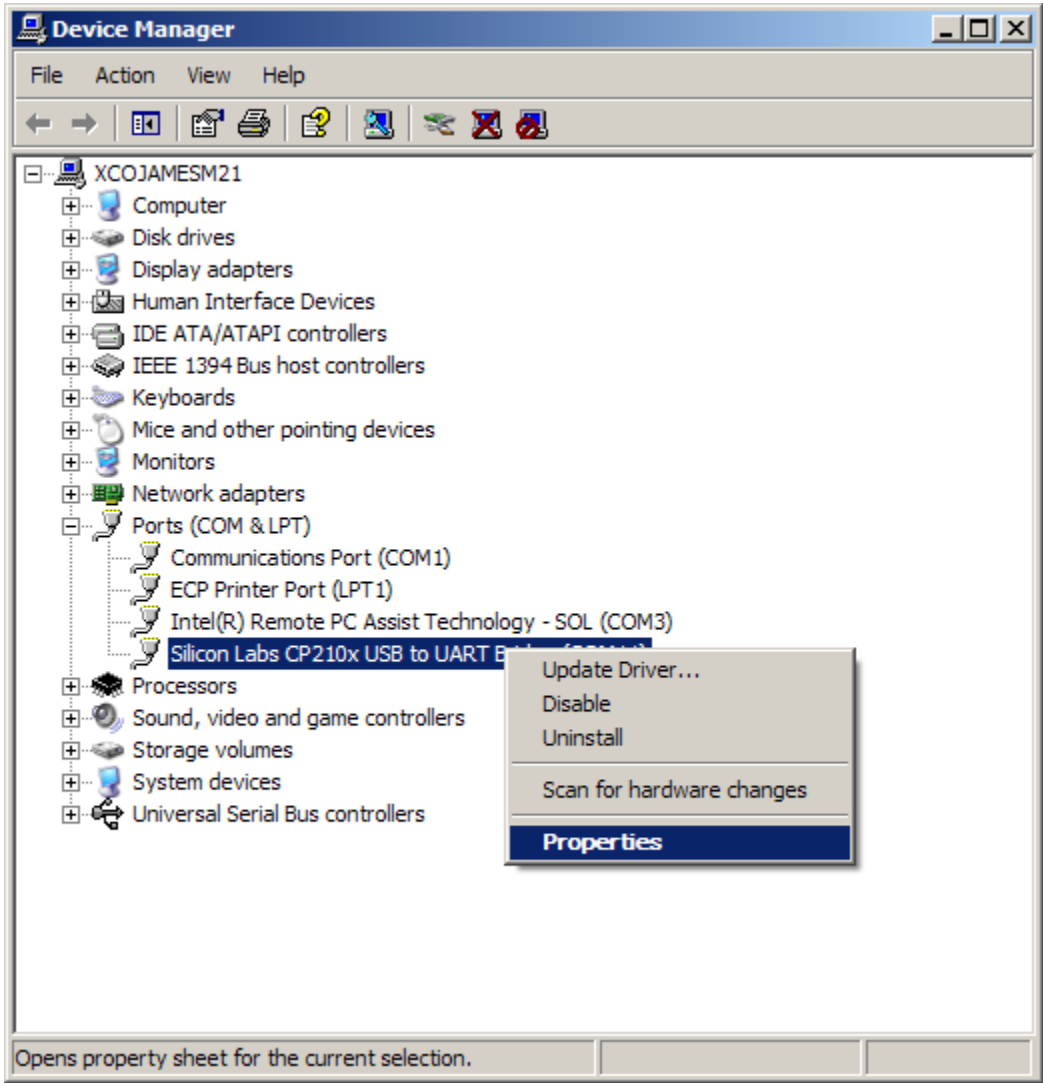
- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager



Note: Presentation applies to the AC701

AC701 Setup

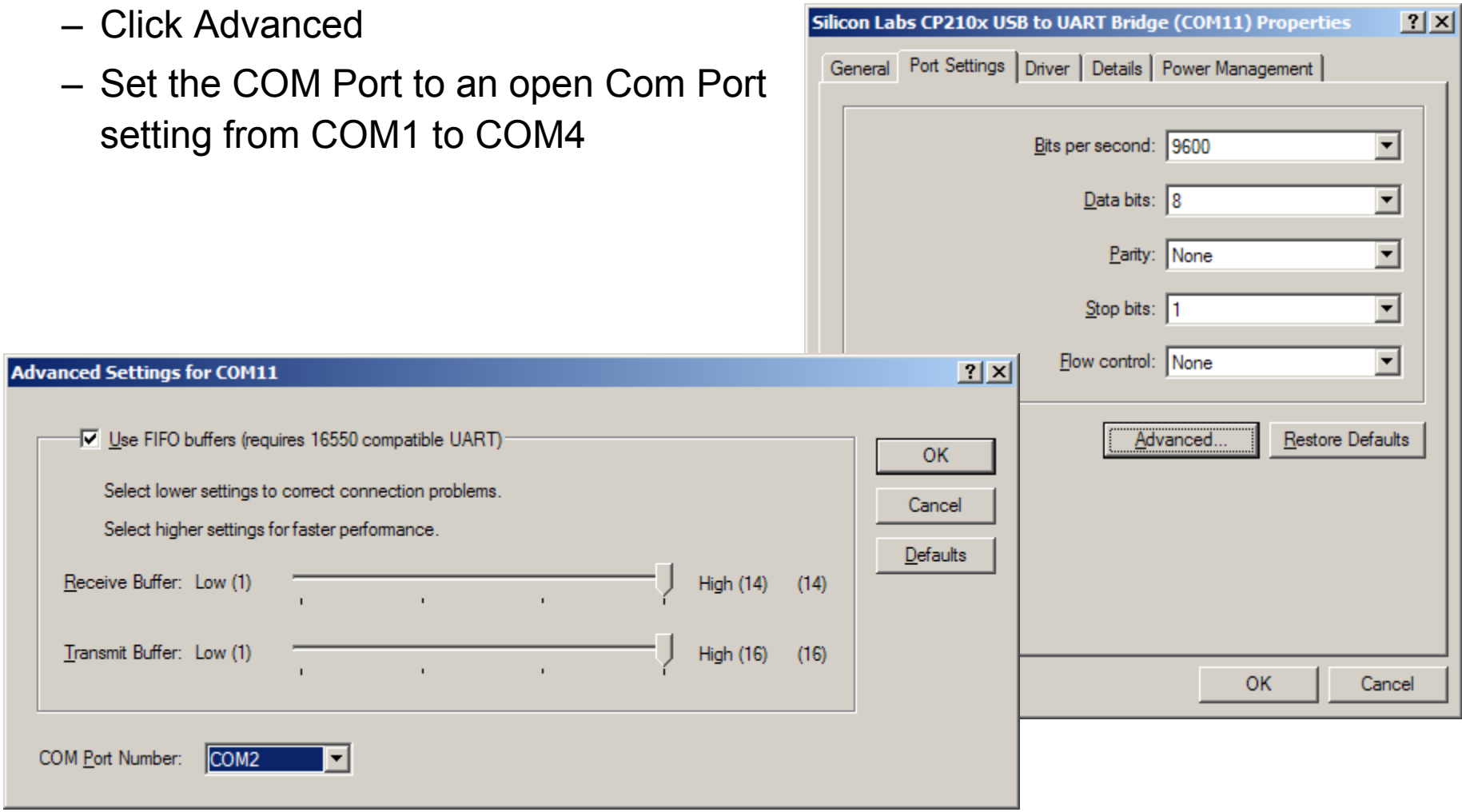
- **Expand the Ports Hardware**
  - Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties



Note: Presentation applies to the AC701

AC701 Setup

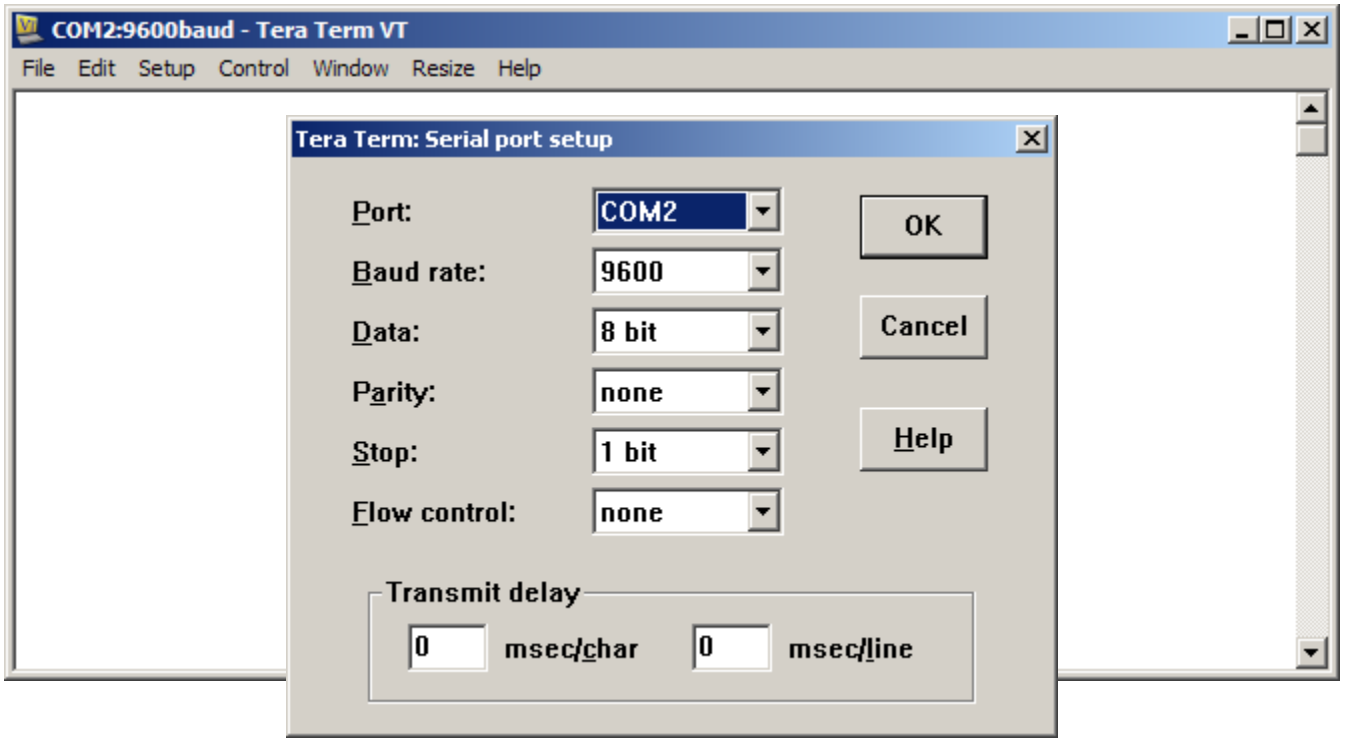
- **Under Port Settings tab**
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4



Note: Presentation applies to the AC701

AC701 Setup

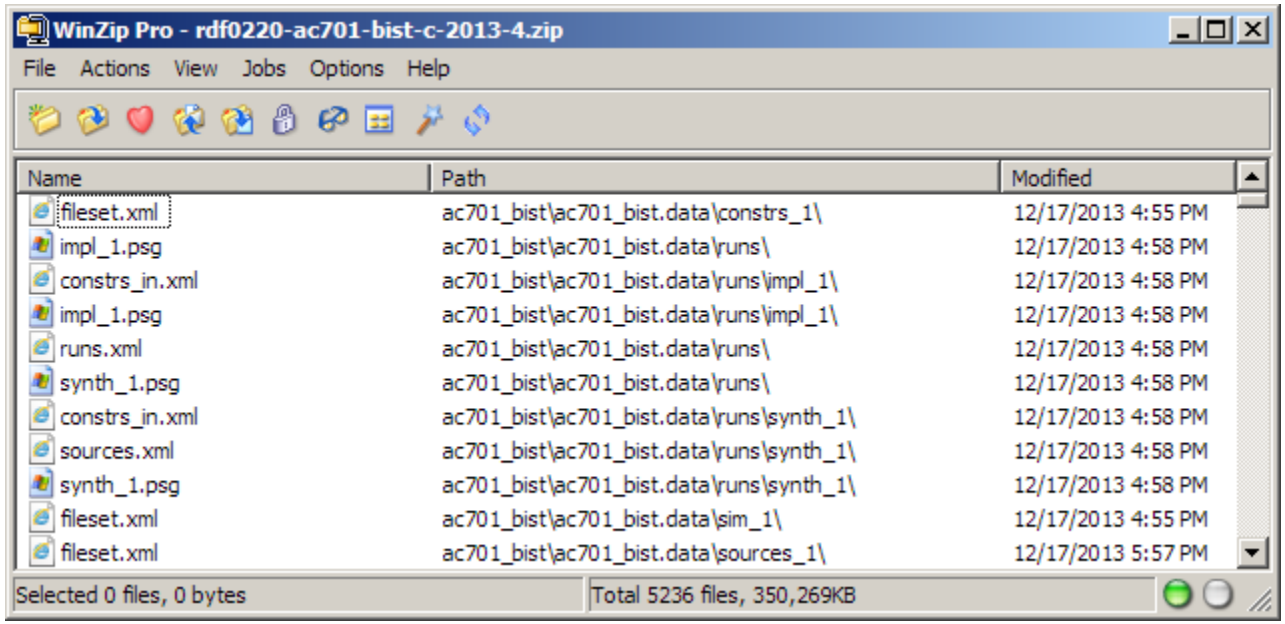
- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 9600



Note: Presentation applies to the AC701

AC701 Setup

- **Unzip the RDF0220 - AC701 BIST Design Files (2013.4 C) zip file**
  - Available through http://www.xilinx.com/ac701

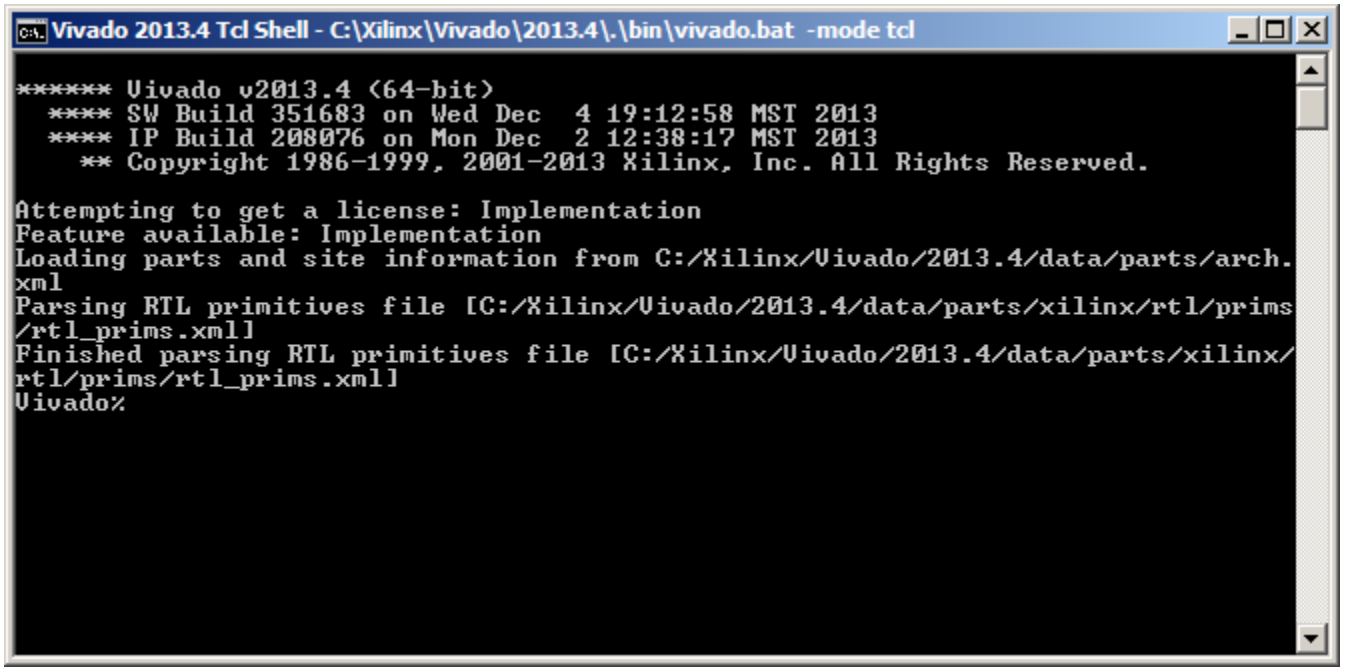


Note: Presentation applies to the AC701

AC701 BIST

- Open a Vivado Tcl Shell:

  Start → All Programs → Xilinx Design Tools → Vivado 2013.4 → Vivado 2013.4 Tcl Shell

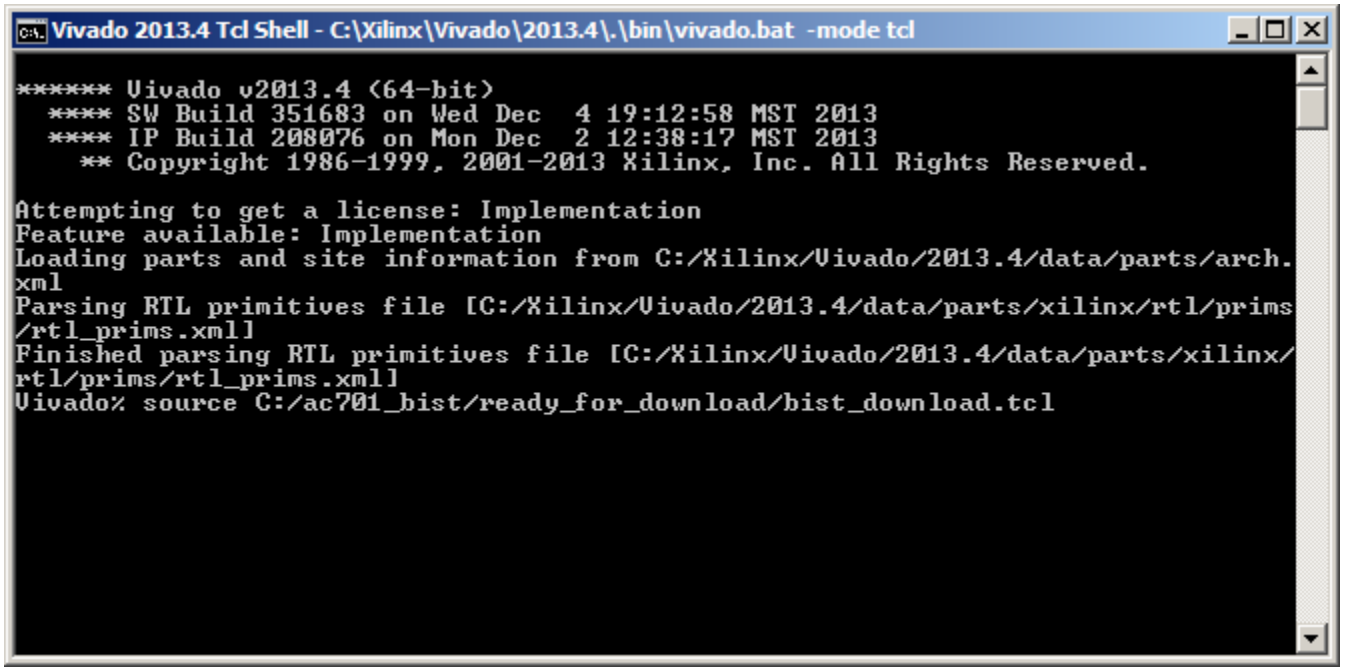


Note: Presentation applies to the AC701

AC701 BIST

- Download the BIST bitstream
- In the Vivado Tcl Shell type:

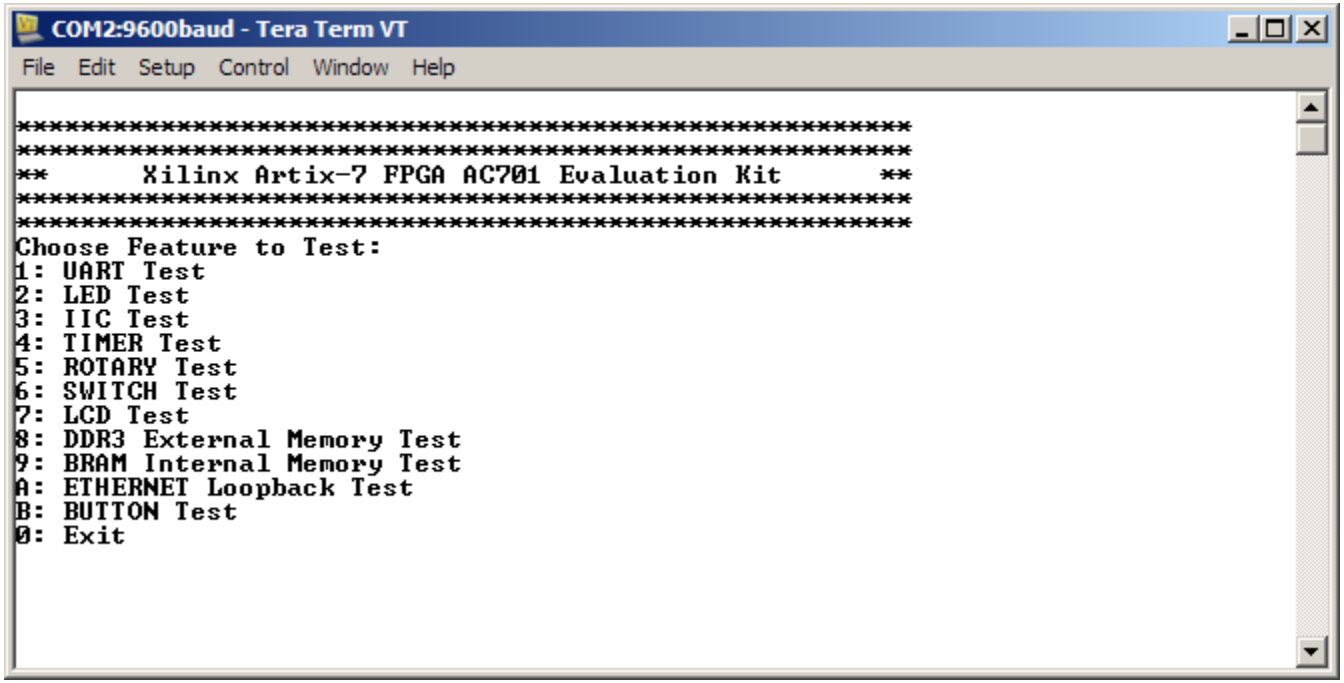
  source C:/ac701_bist/ready_for_download/bist_download.tcl



Note: Presentation applies to the AC701

AC701 BIST

- View initial BIST screen



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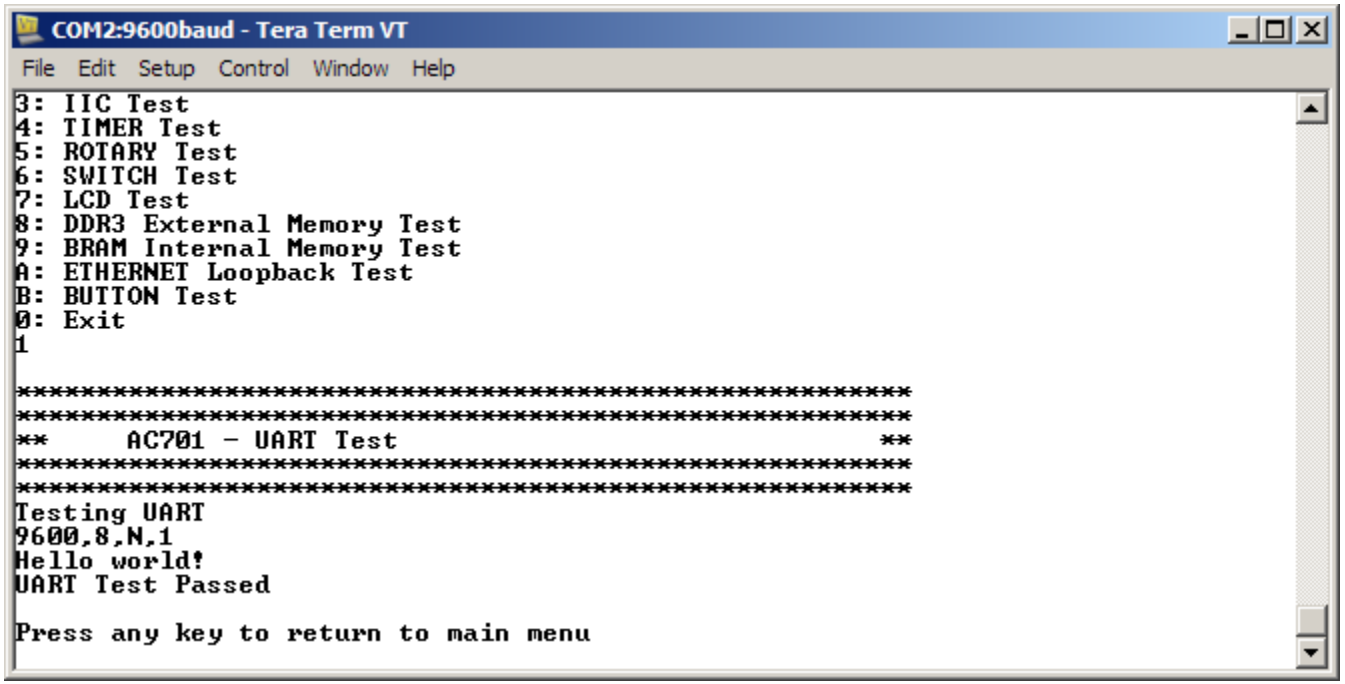
AC701 BIST

UART Test

- Type “**1**” to start the UART Test
- After each test, press any key to return to the main menu



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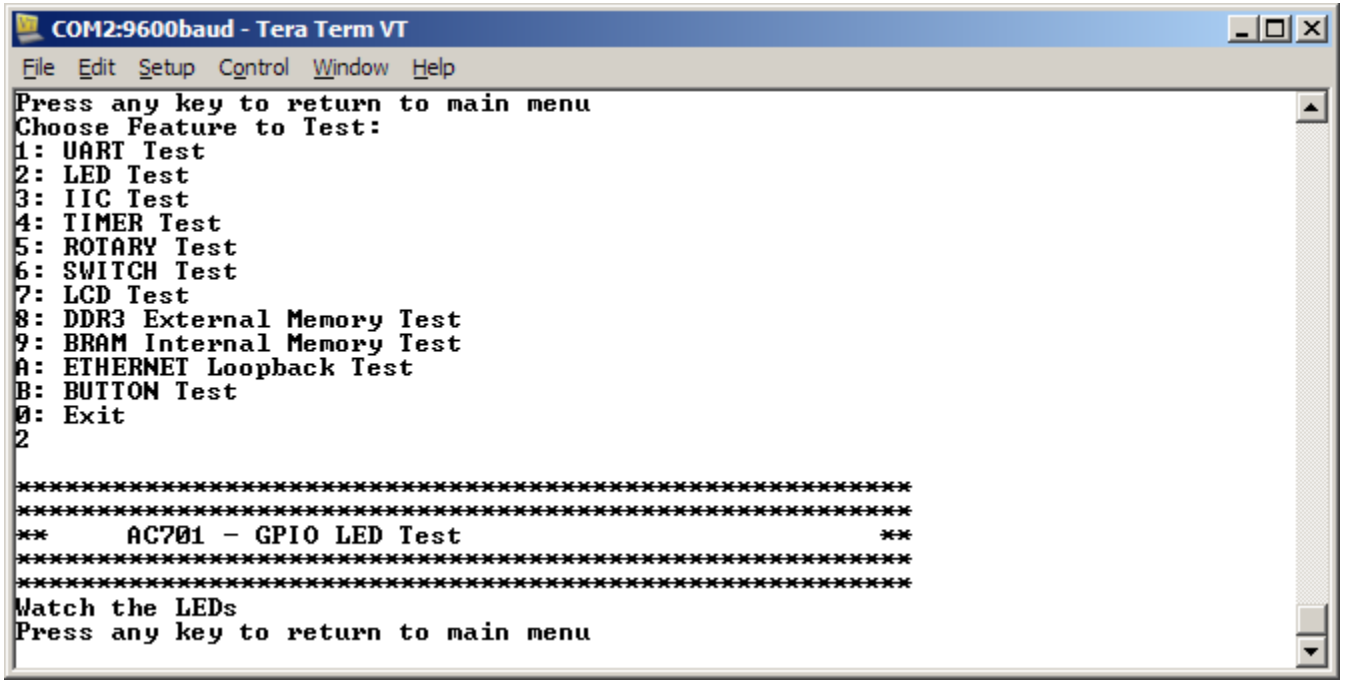
AC701 BIST

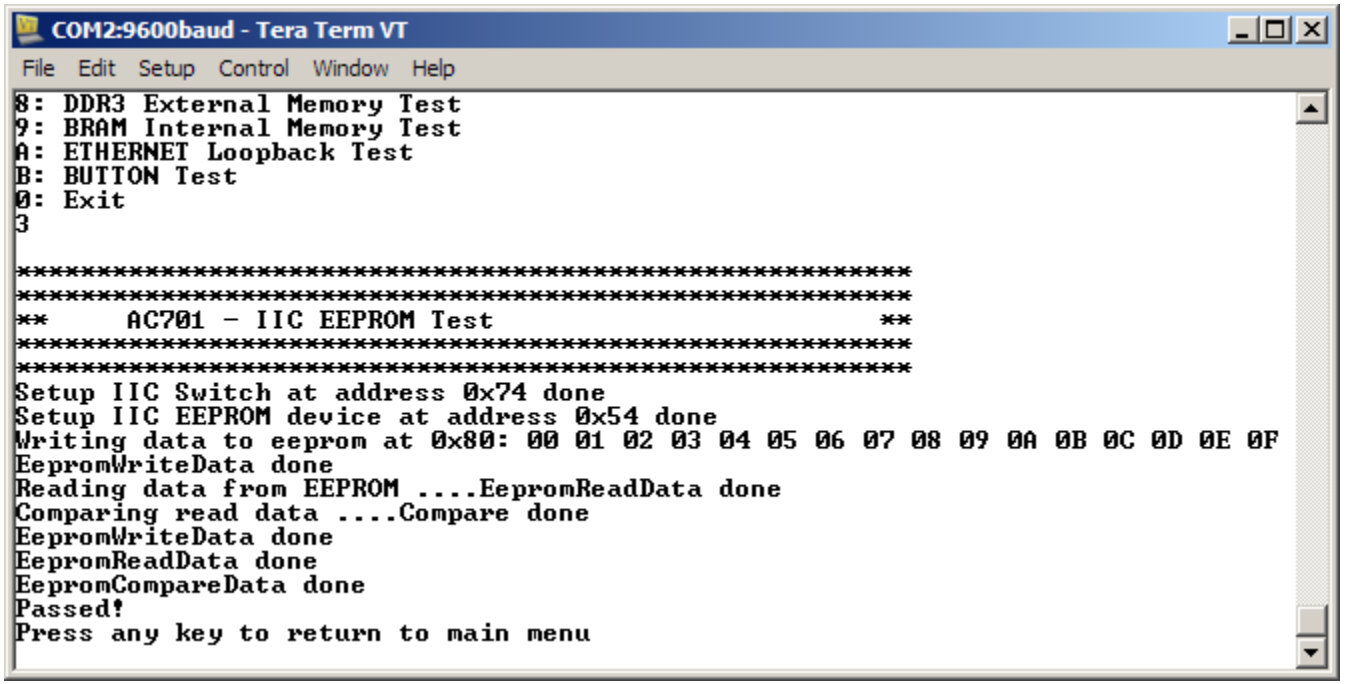
- **LED Test**
  - Type **2** to begin LED Test
- **View Walking 1's pattern on GPIO LEDs**
  - Sequence repeats twice



Note: Presentation applies to the AC701

AC701 BIST

- IIC Test
  - Type **3** to begin IIC Test



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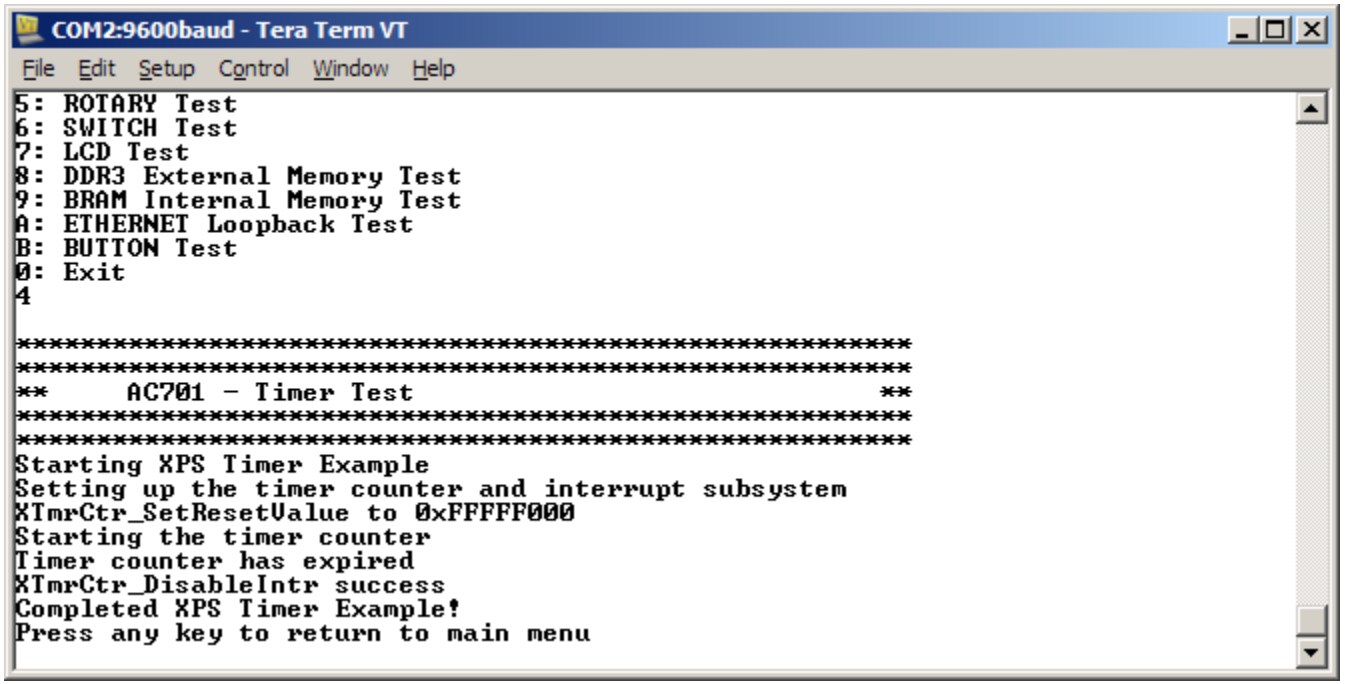
AC701 BIST

- **Timer Test**
  - Type **4** to begin Timer Test

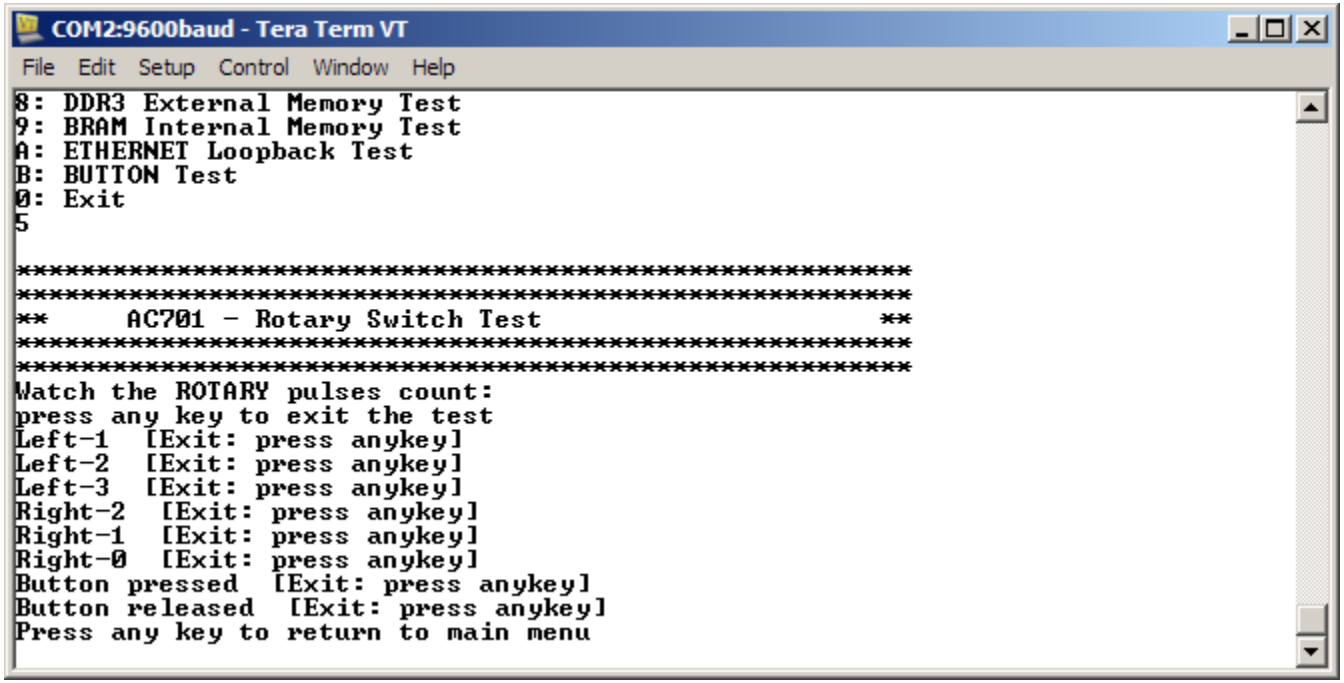


Note: Presentation applies to the AC701

AC701 BIST

Rotary Test

- Type **5** to begin Rotary Test
- Turn the rotary switch (under the LCD) back and forth

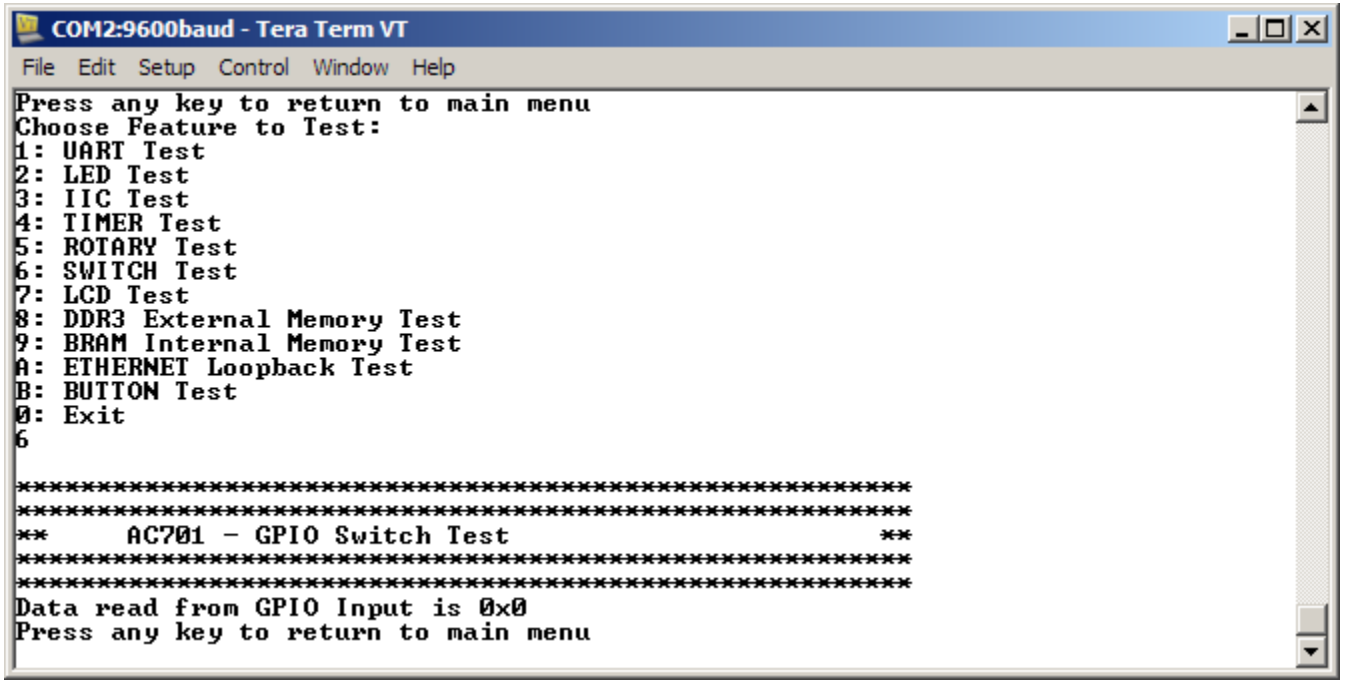


Note: Presentation applies to the AC701

AC701 BIST

GPIO Switch Test

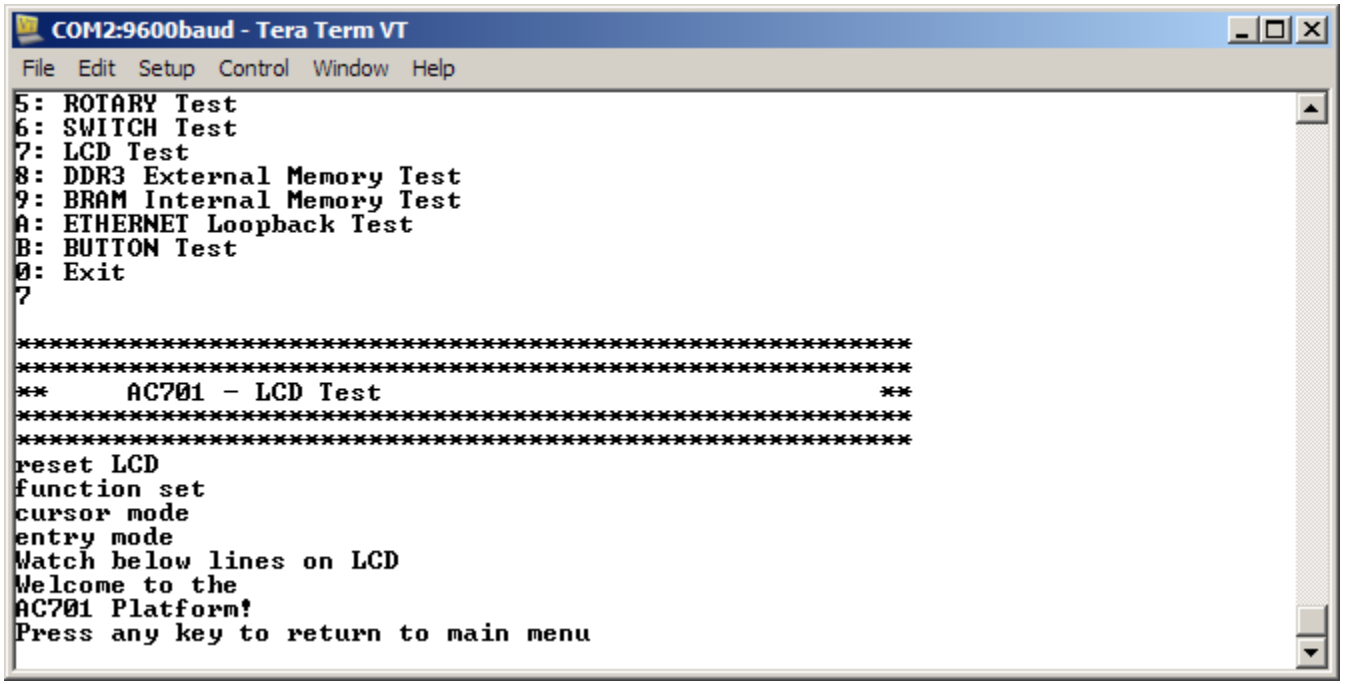
- Set 4-position GPIO DIP Switch (SW2)
- Type **6** to begin GPIO Switch Test
  - Reads switch settings



Note: Presentation applies to the AC701

AC701 BIST

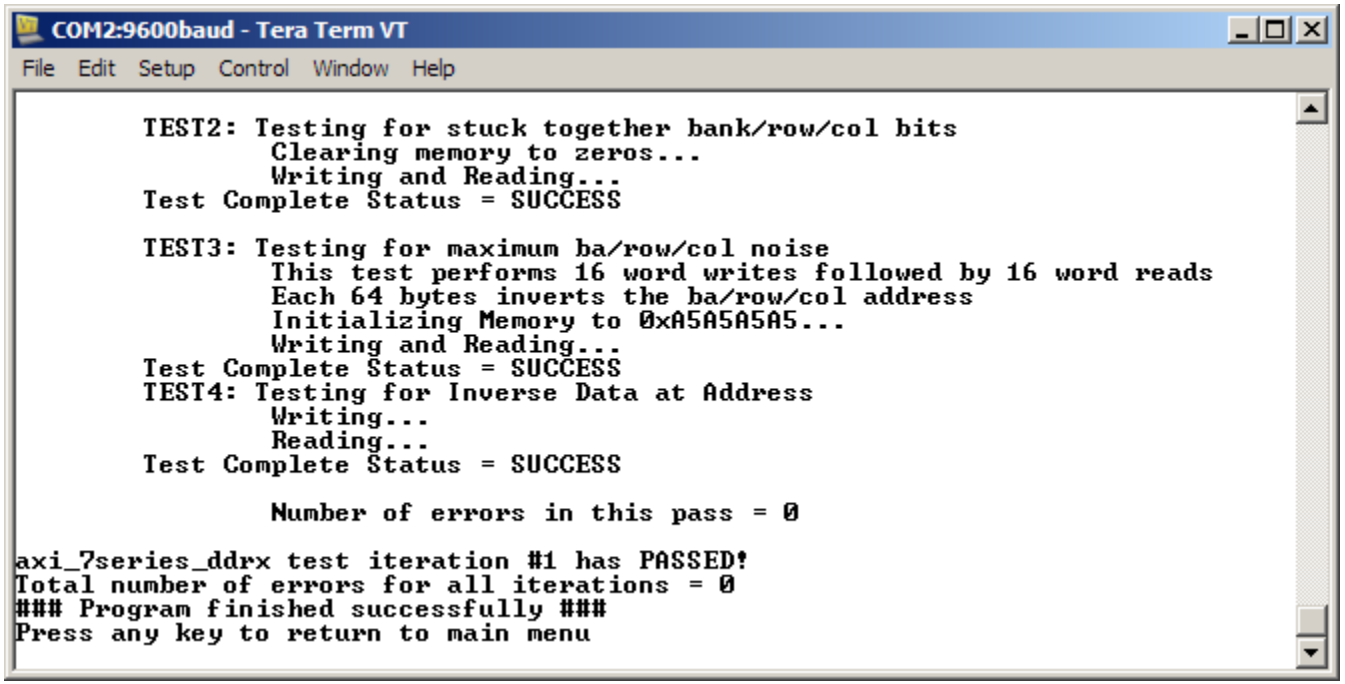
- **LCD Test**
  - Type **7** to begin LCD Test



Note: Presentation applies to the AC701

AC701 BIST

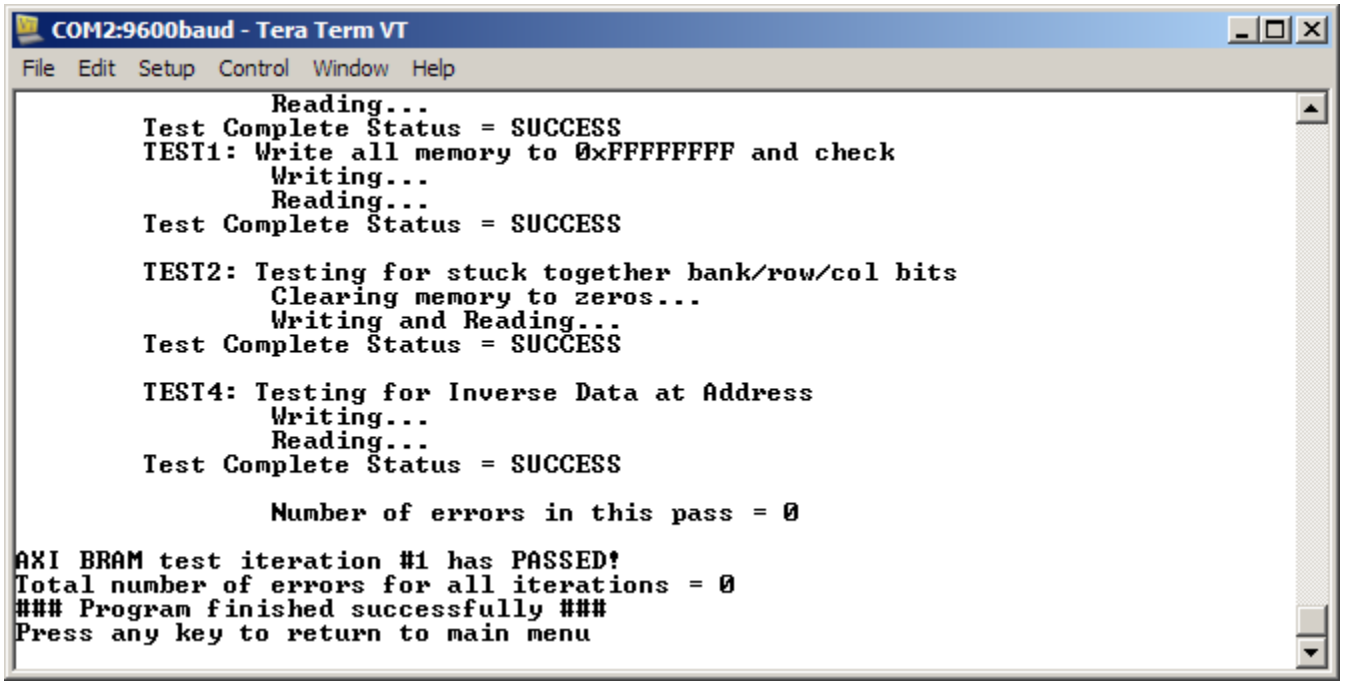
- **External Memory Test**
  - Type **8** to begin External Memory Test



Note: Presentation applies to the AC701

AC701 BIST

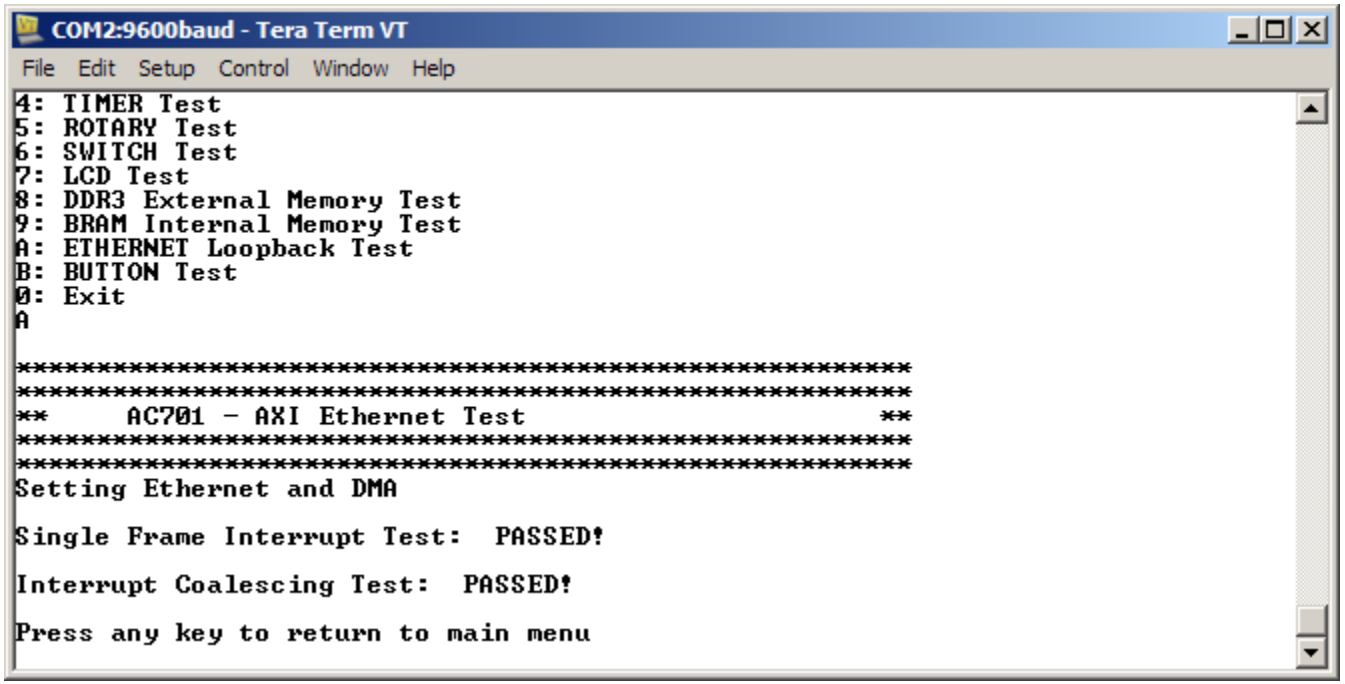
- **Internal Memory Test**
  - Type **9** to begin BRAM Memory Test



Note: Presentation applies to the AC701

AC701 BIST

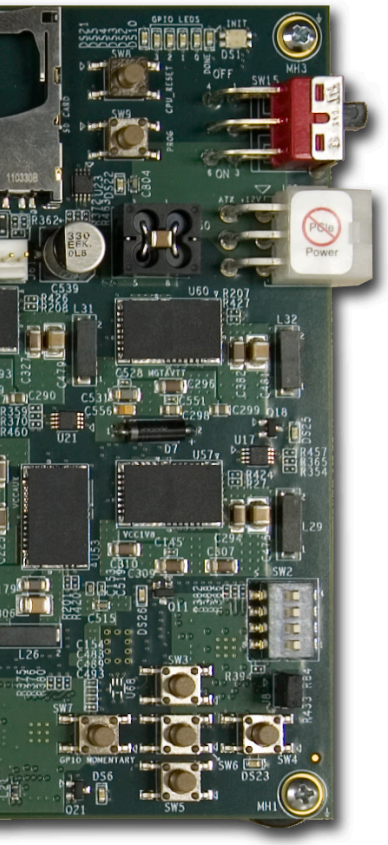
- **Ethernet Test**
  - Type **A** to begin AXI Ethernet Test



Note: Presentation applies to the AC701

AC701 BIST

- **Button Test**
  - Type **B** to begin Button Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Help

```
A: ETHERNET Loopback Test
B: BUTTON Test
0: Exit
B

**************************************************************
**************************************************************
**      AC701 - Button Test                                 **
**************************************************************
**************************************************************
Press west button

Press south button

Press east button

Press north button

Press center button

Press any button

Press any key to return to main menu
```

Note: Presentation applies to the AC701

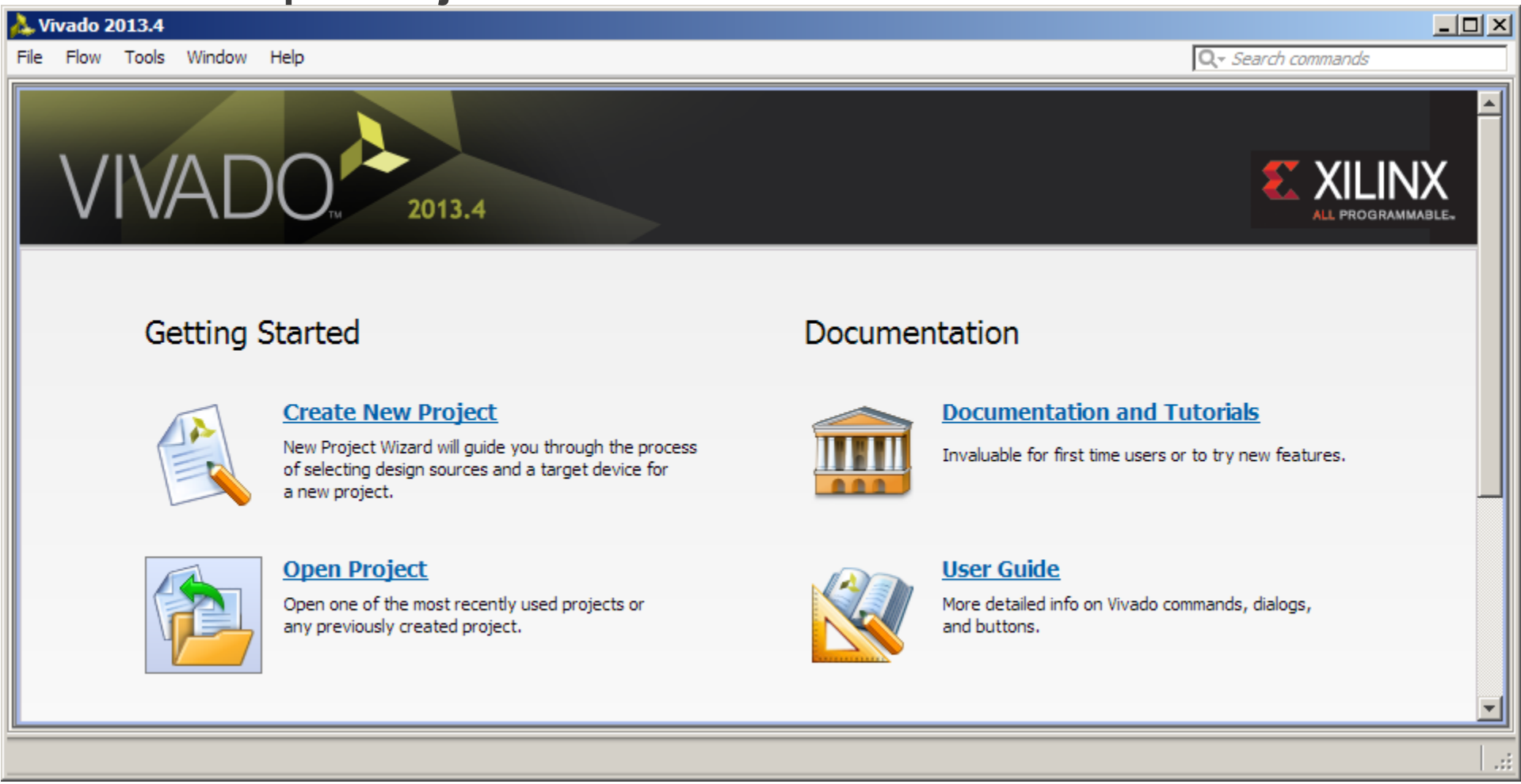
Compile AC701 BIST Design

Compile AC701 BIST Design

- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2013.4 → Vivado

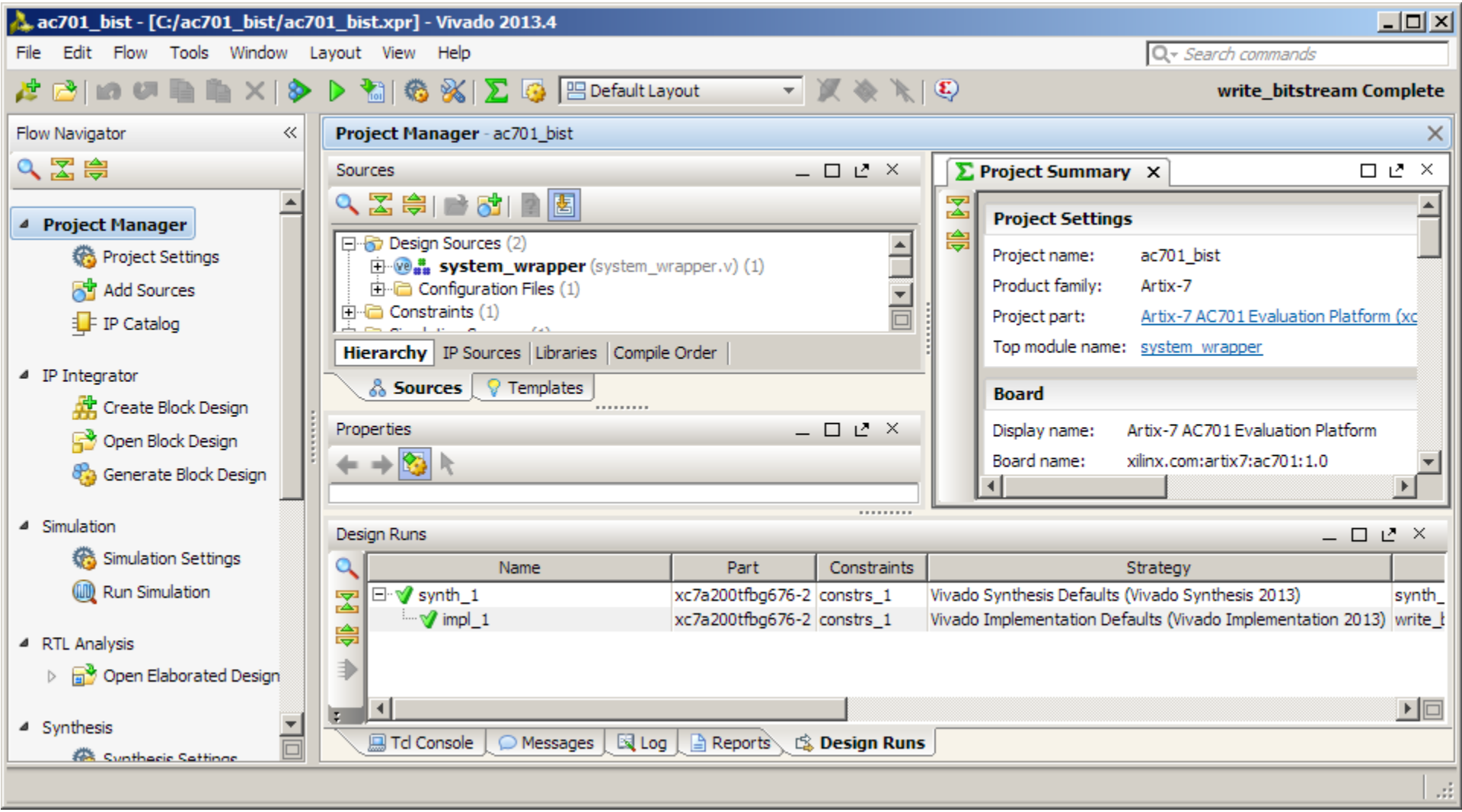
- Select Open Project



Note: Presentation applies to the AC701

Compile AC701 BIST Design

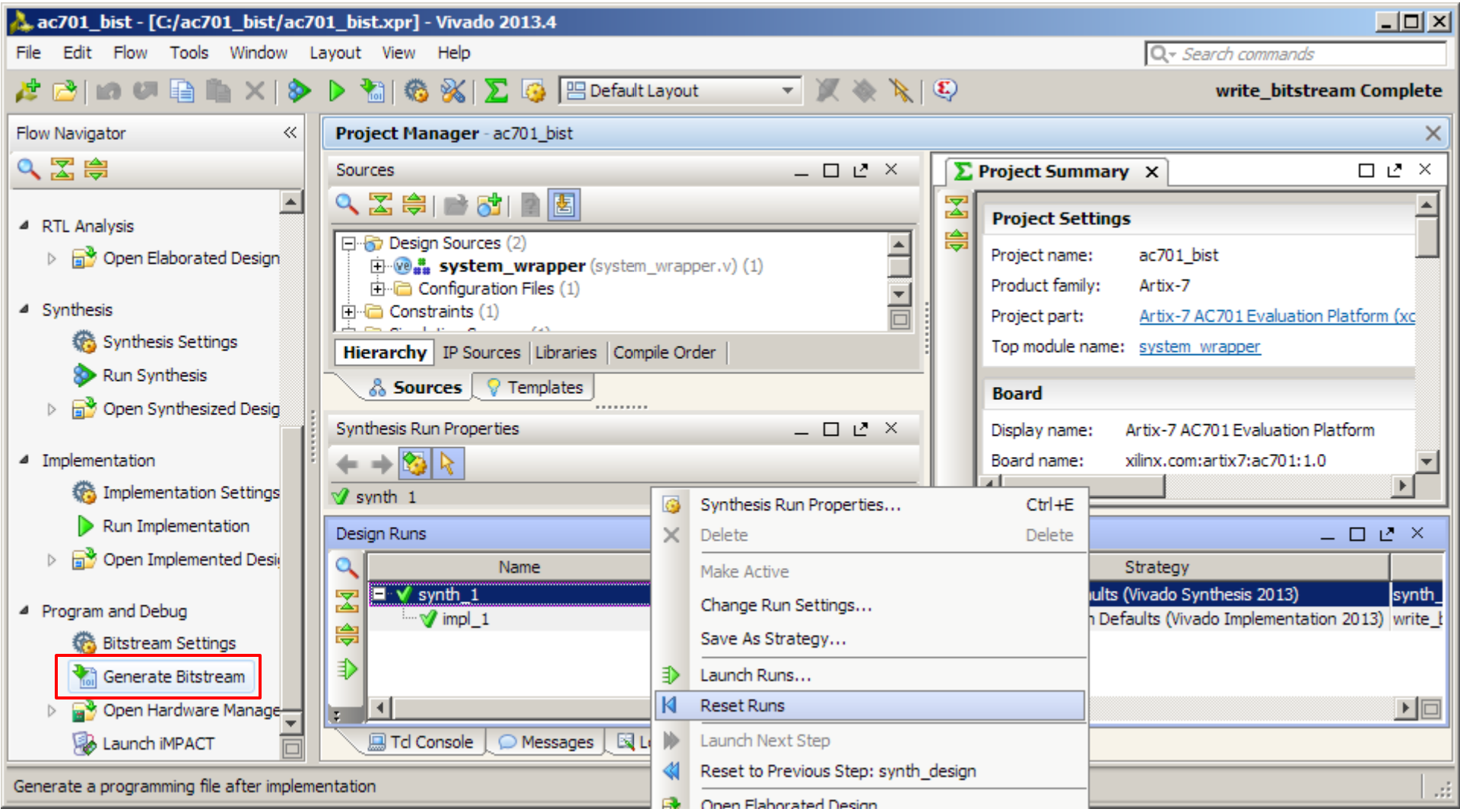
- Open the AC701 Design:
  - **<Design Name>\ac701_bist.xpr**



Note: Presentation applies to the AC701

Compile AC701 BIST Design

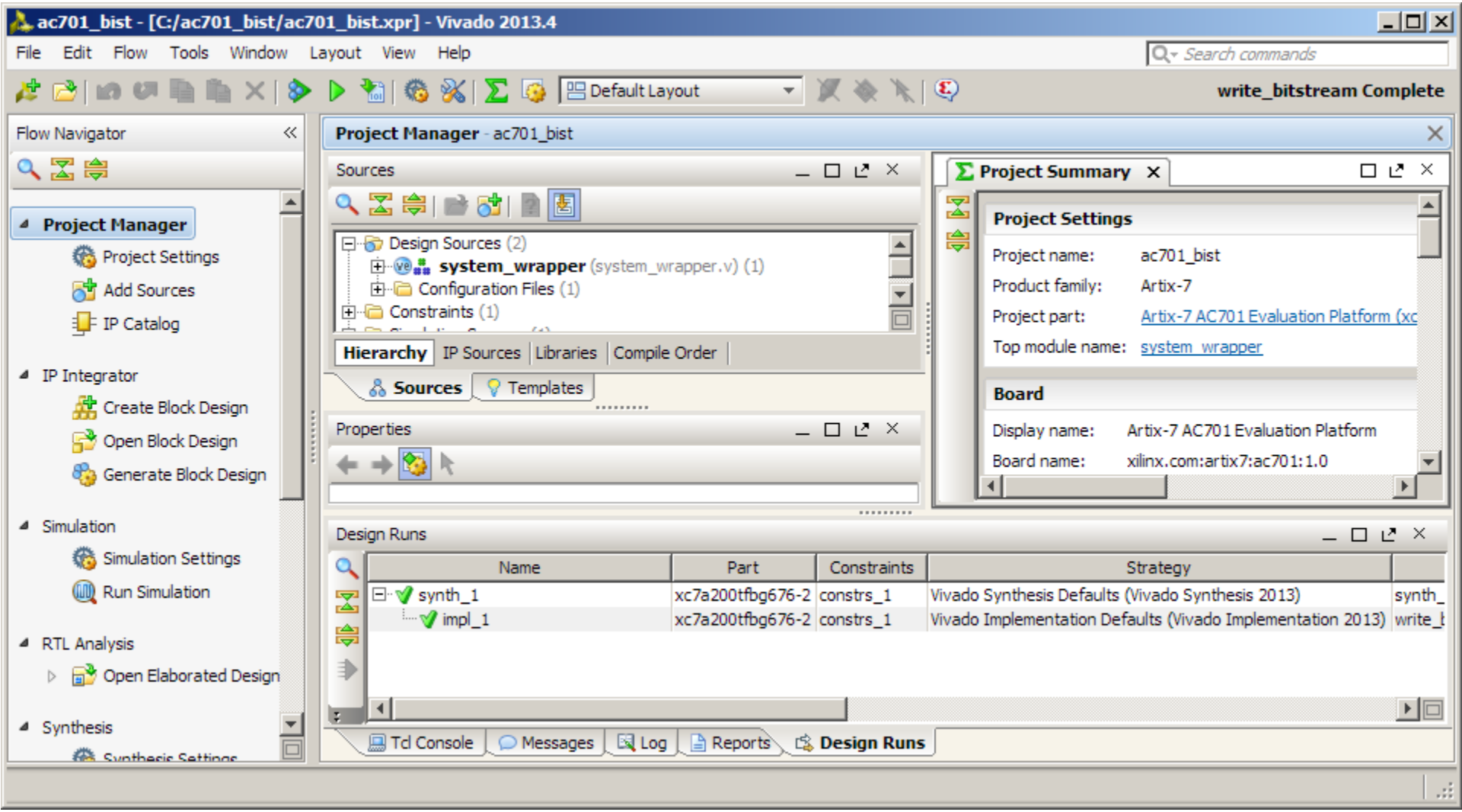
- **The design is fully implemented; you can recompile, or export to SDK**
  - To recompile, right-click **synth_1**, select **Reset Runs** then **Generate Bitstream**



Note: Presentation applies to the AC701

Compile AC701 BIST Design

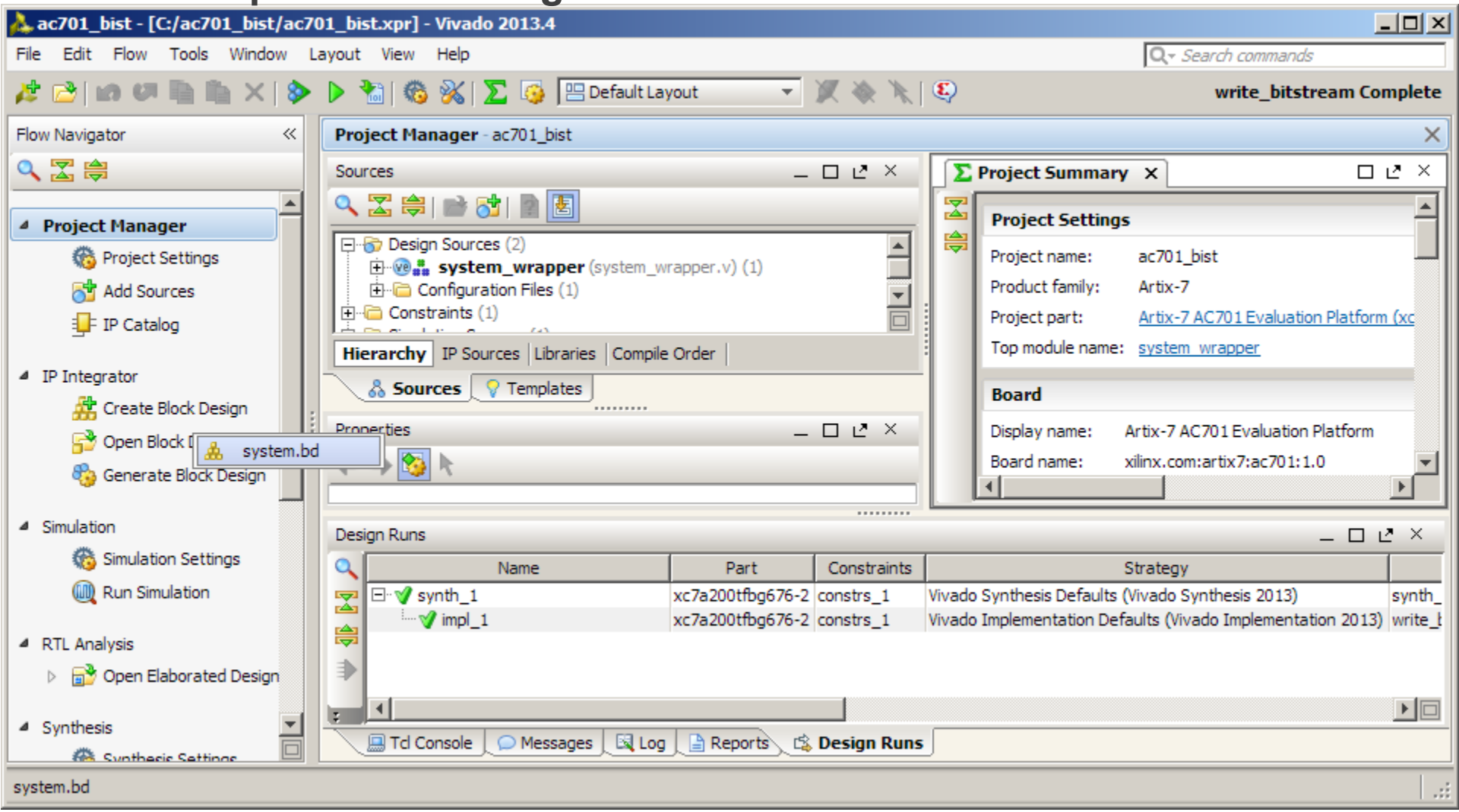
- Once done, both the Synthesis and Implementation will have green check marks



Note: Presentation applies to the AC701

Compile AC701 BIST Design

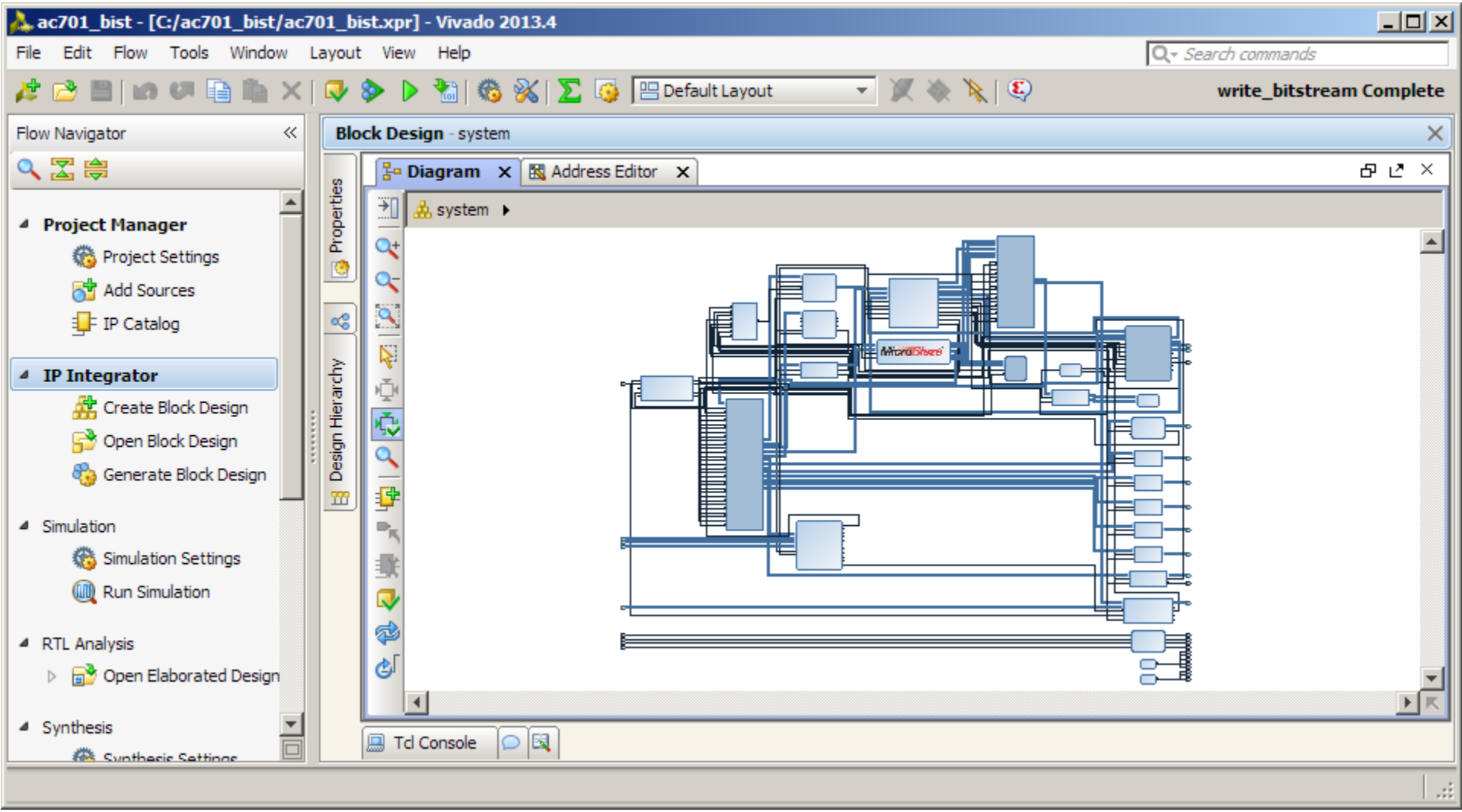
- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design



Note: Presentation applies to the AC701

Compile AC701 BIST Design

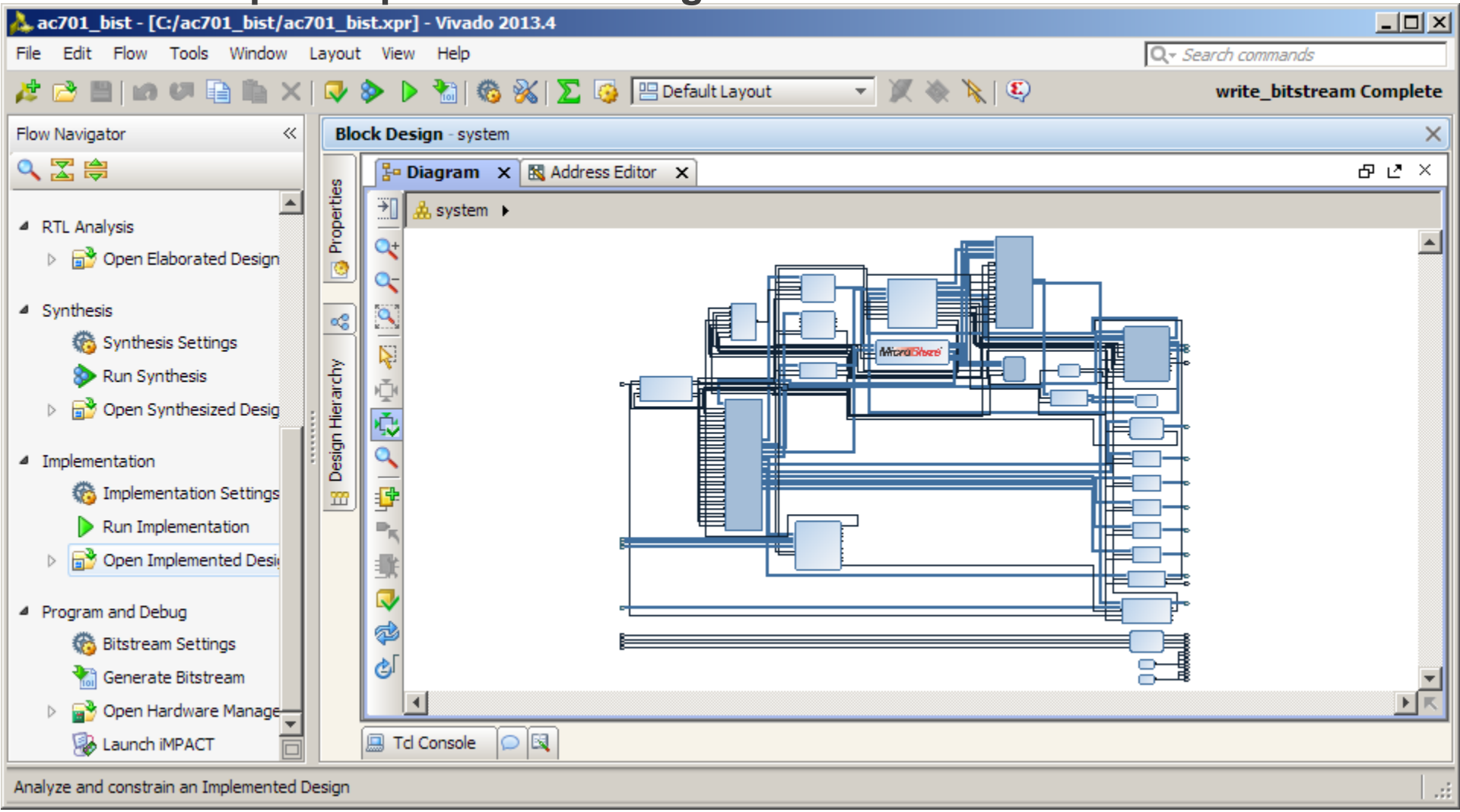
- All the IP Blocks used in the design can be seen in this view



Note: Presentation applies to the AC701

Compile AC701 BIST Design

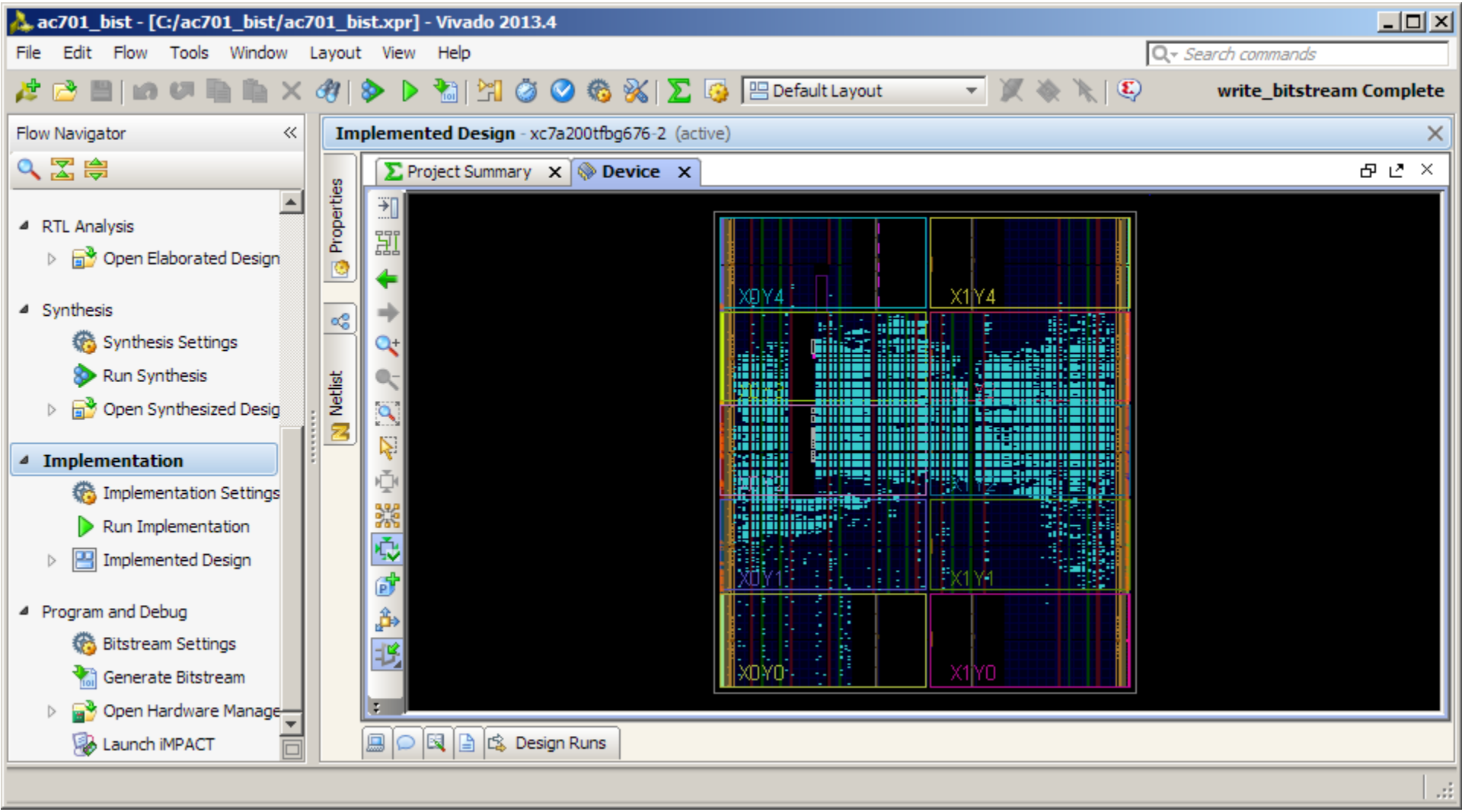
- To export to SDK, the Block and Implemented designs must be open
- Click Open Implemented Design



Note: Presentation applies to the AC701

Compile AC701 BIST Design

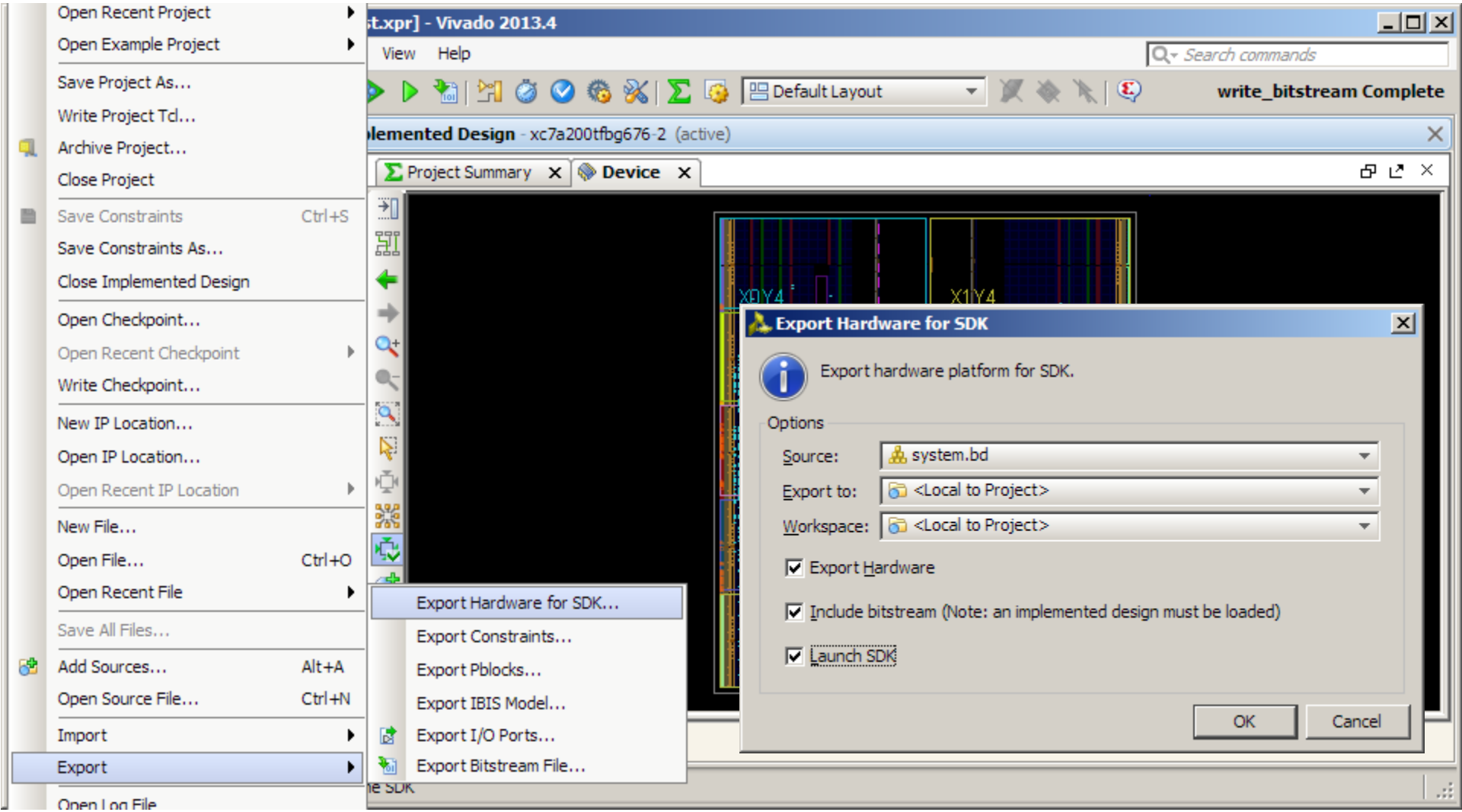
View Implemented Design



Note: Presentation applies to the AC701

Compile AC701 BIST Design

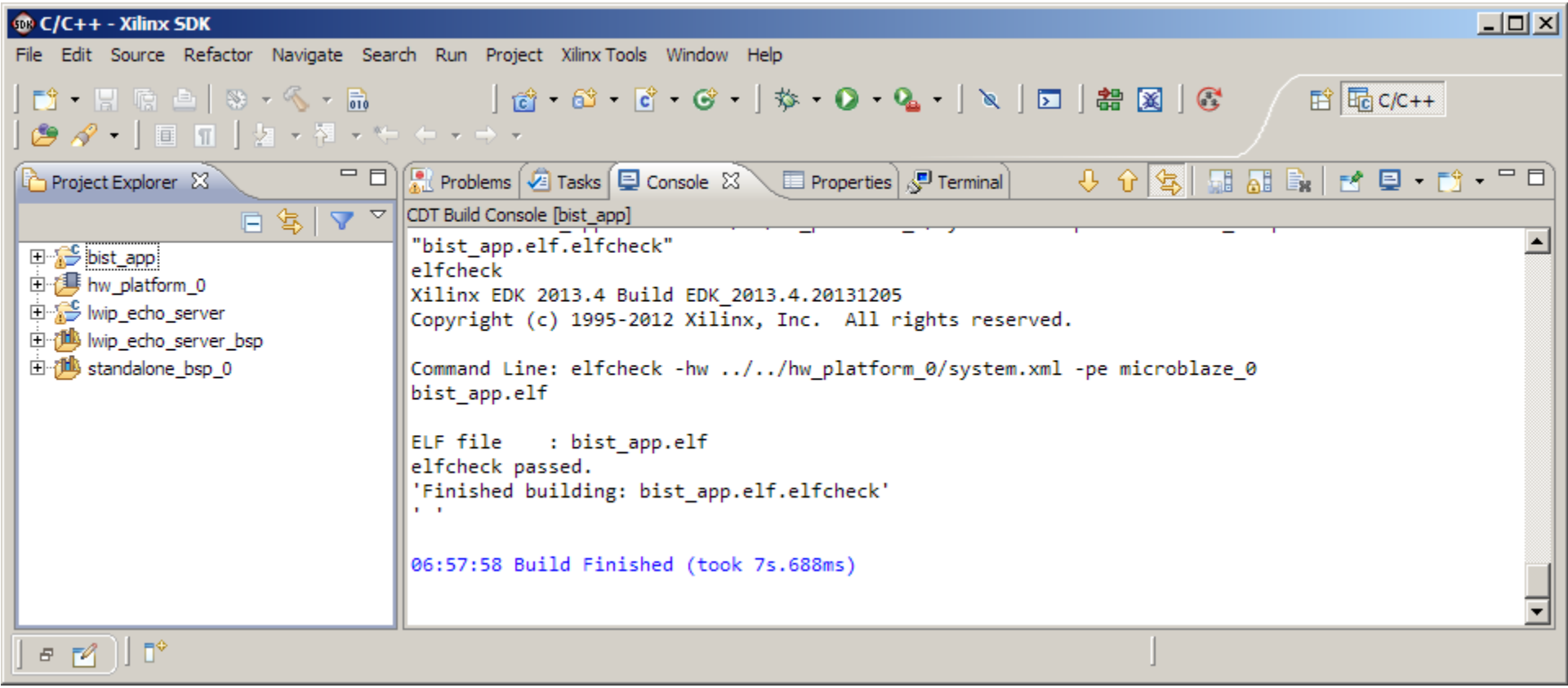
- Select File → Export → Export hardware for SDK…
- Select Launch SDK and click OK



Note: Presentation applies to the AC701

Compile AC701 Software in SDK

- **SDK Software Compile - Build ELF files in SDK**
  - Project builds automatically
  - When done, close SDK and return to Vivado

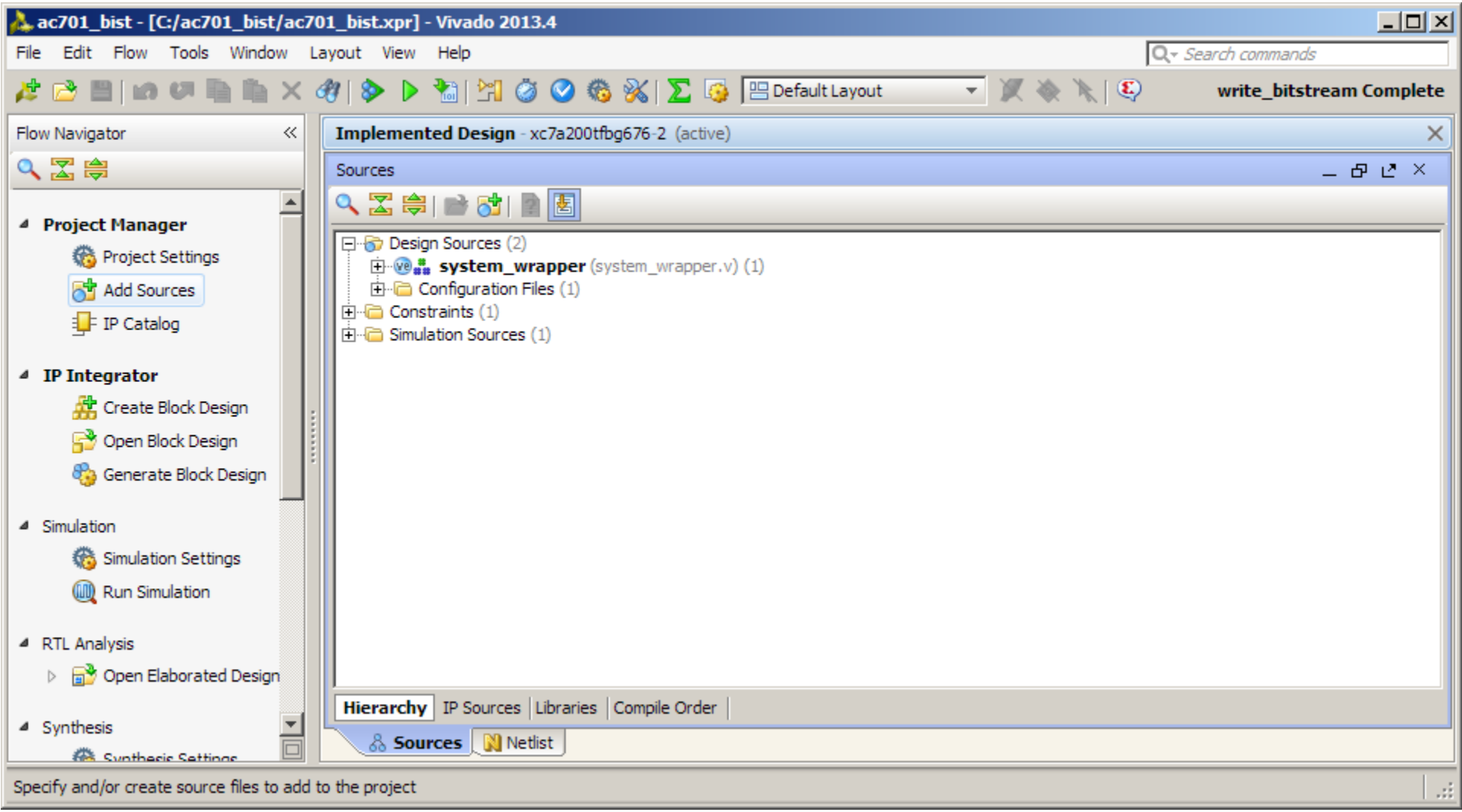


Note: Presentation applies to the AC701

Program AC701 with BIST Design

Program AC701 with BIST Design

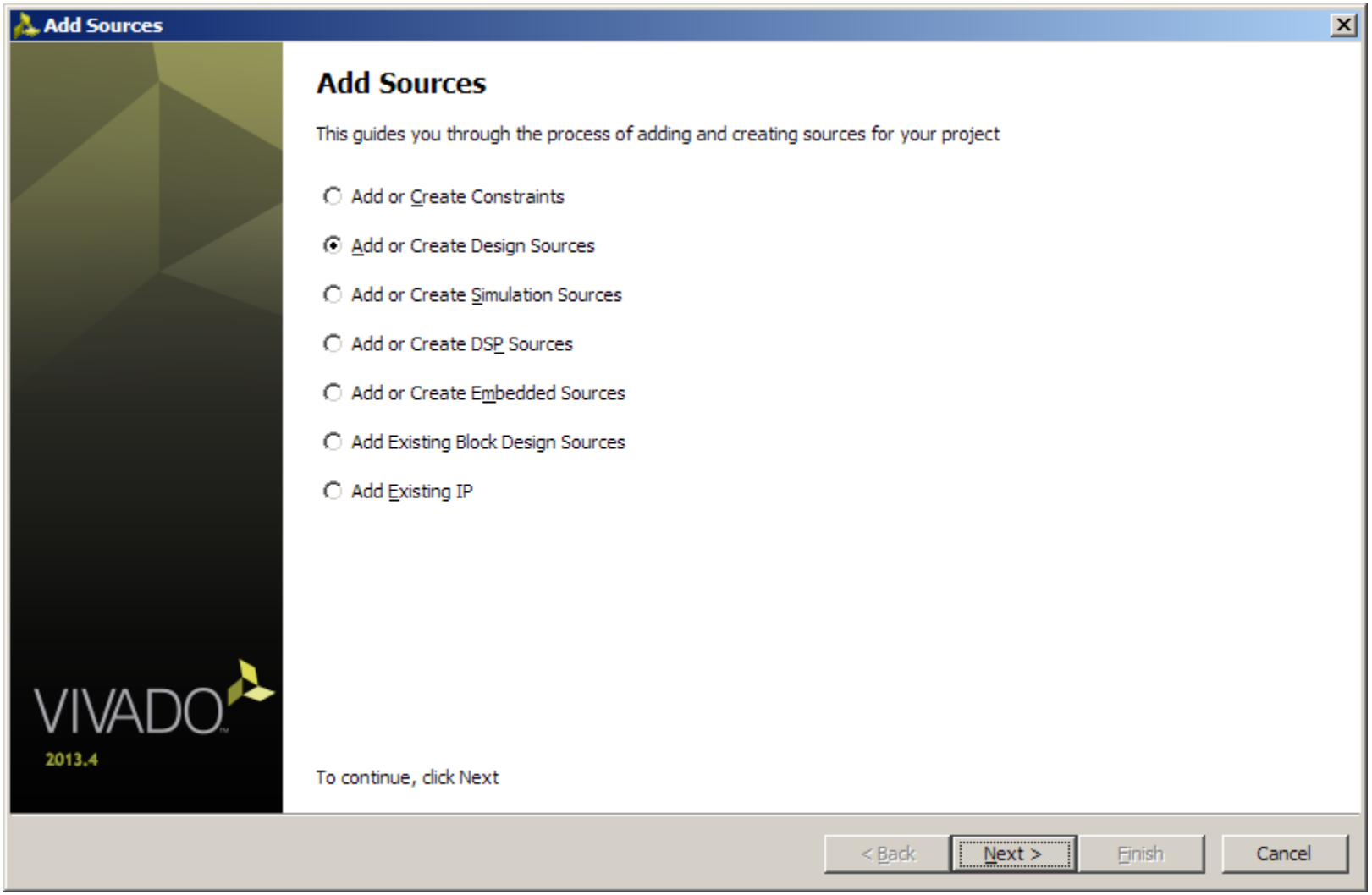
- Select Add Sources



Note: Presentation applies to the AC701

Program AC701 with BIST Design

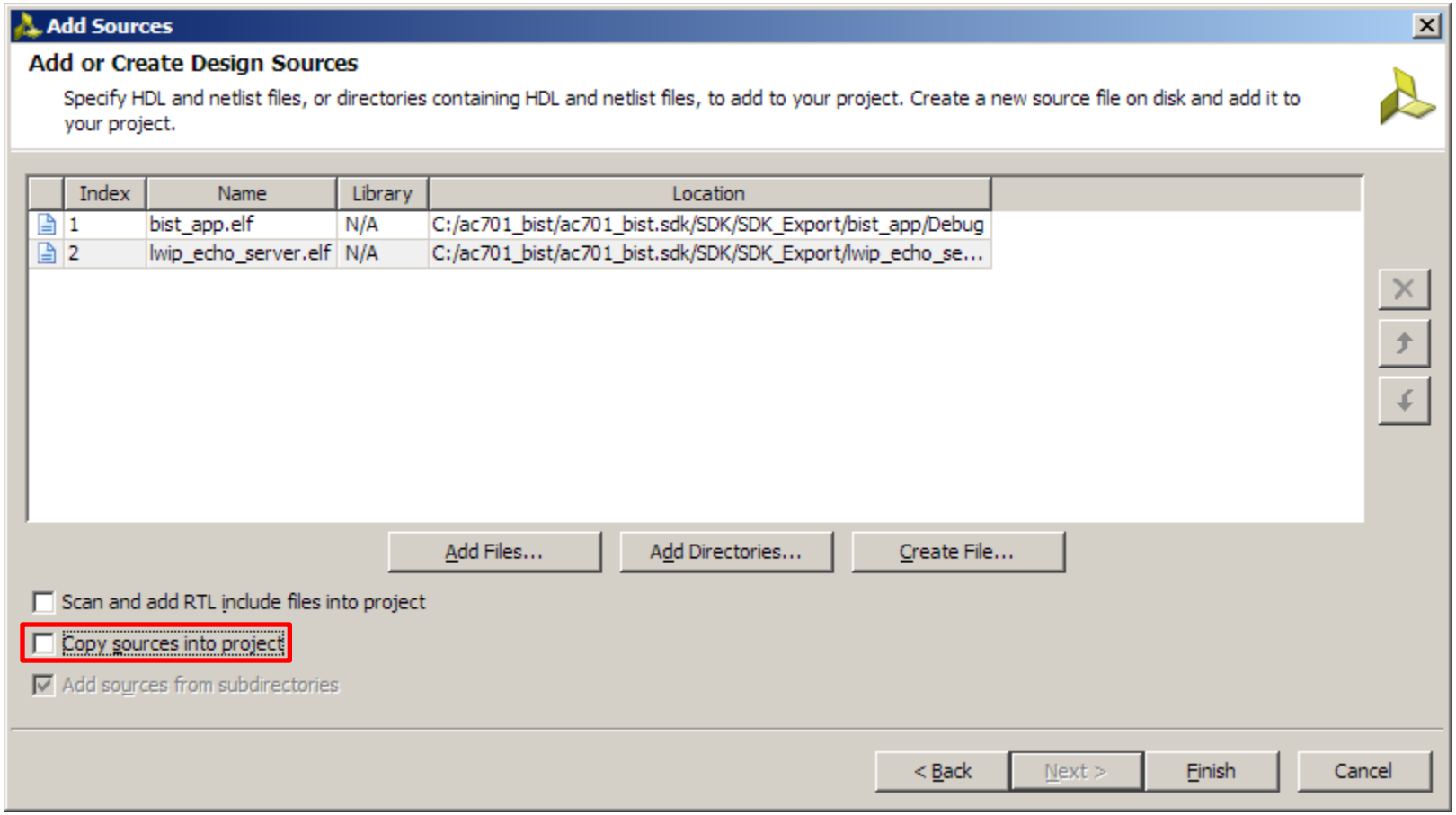
- Select Add or Create Design Sources



Note: Presentation applies to the AC701

Program AC701 with BIST Design

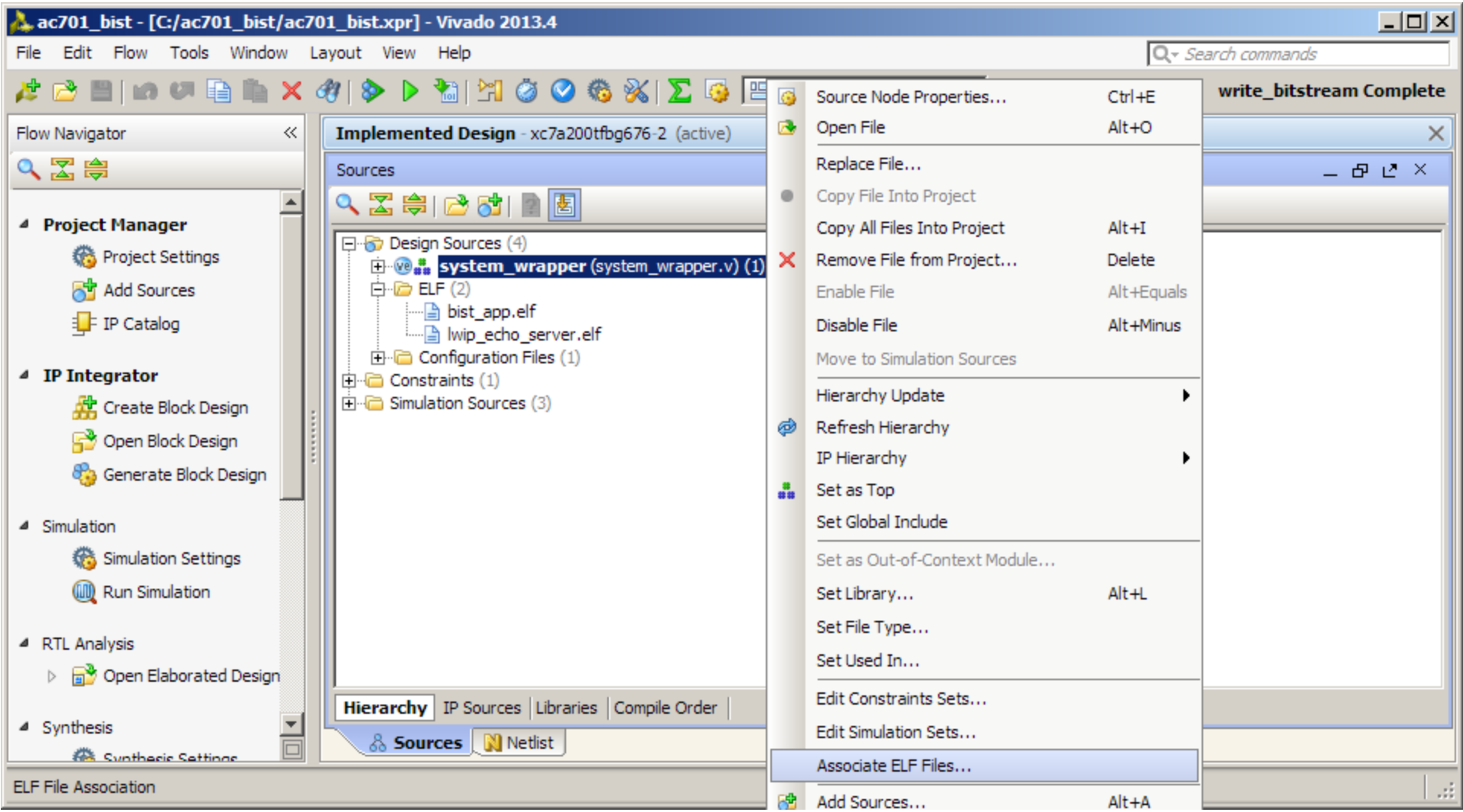
- Add bist_app.elf and lwip_echo_server.elf from the SDK tree
- Make sure Copy sources into project is deselected
- Click Finish



Note: Presentation applies to the AC701

Program AC701 with BIST Design

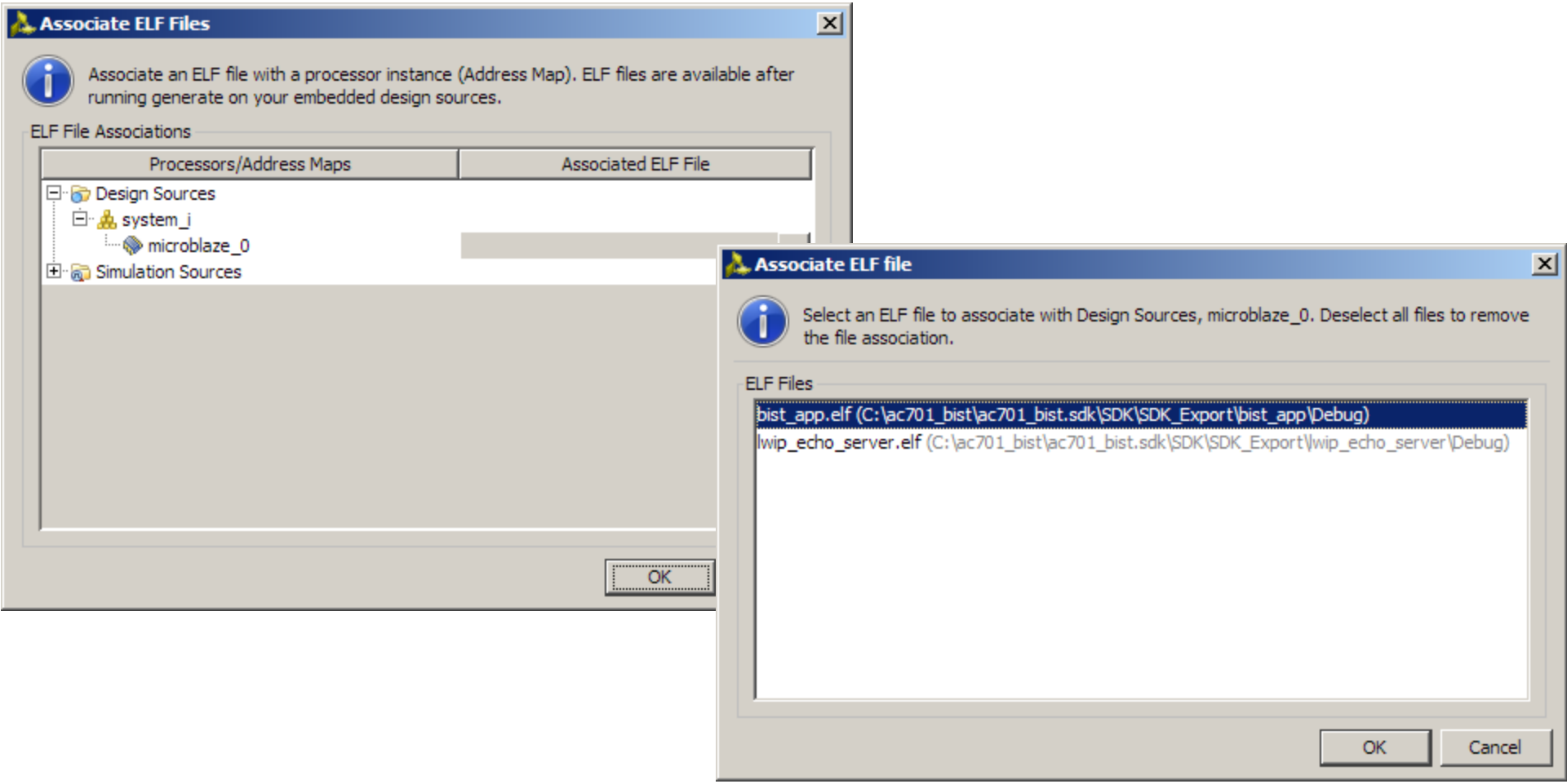
- Right-click on the Design and select Associate ELF Files…



Note: Presentation applies to the AC701

Program AC701 with BIST Design

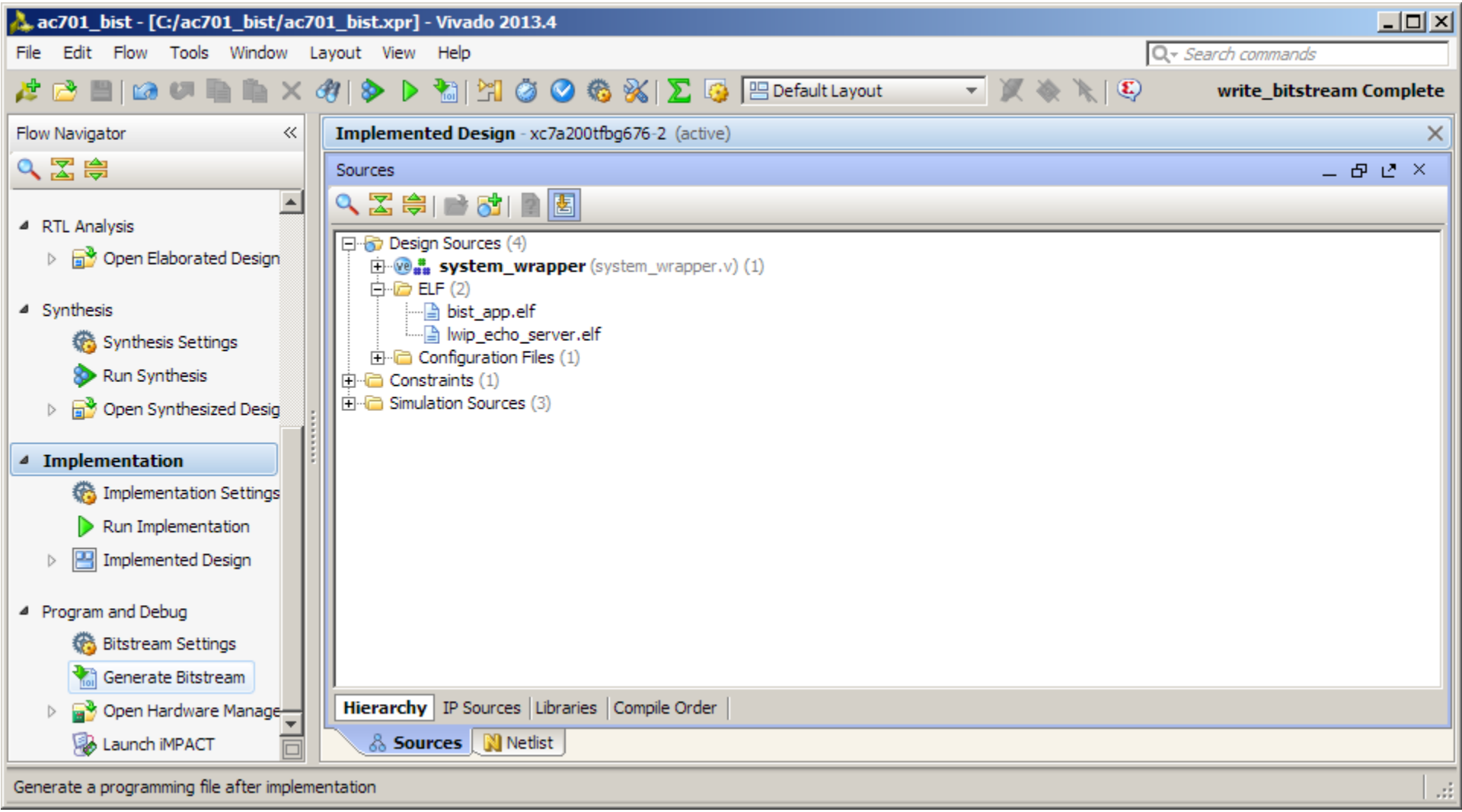
- Click the button to the right; select the bist_app.elf then click OK twice



Note: Presentation applies to the AC701

Program AC701 with BIST Design

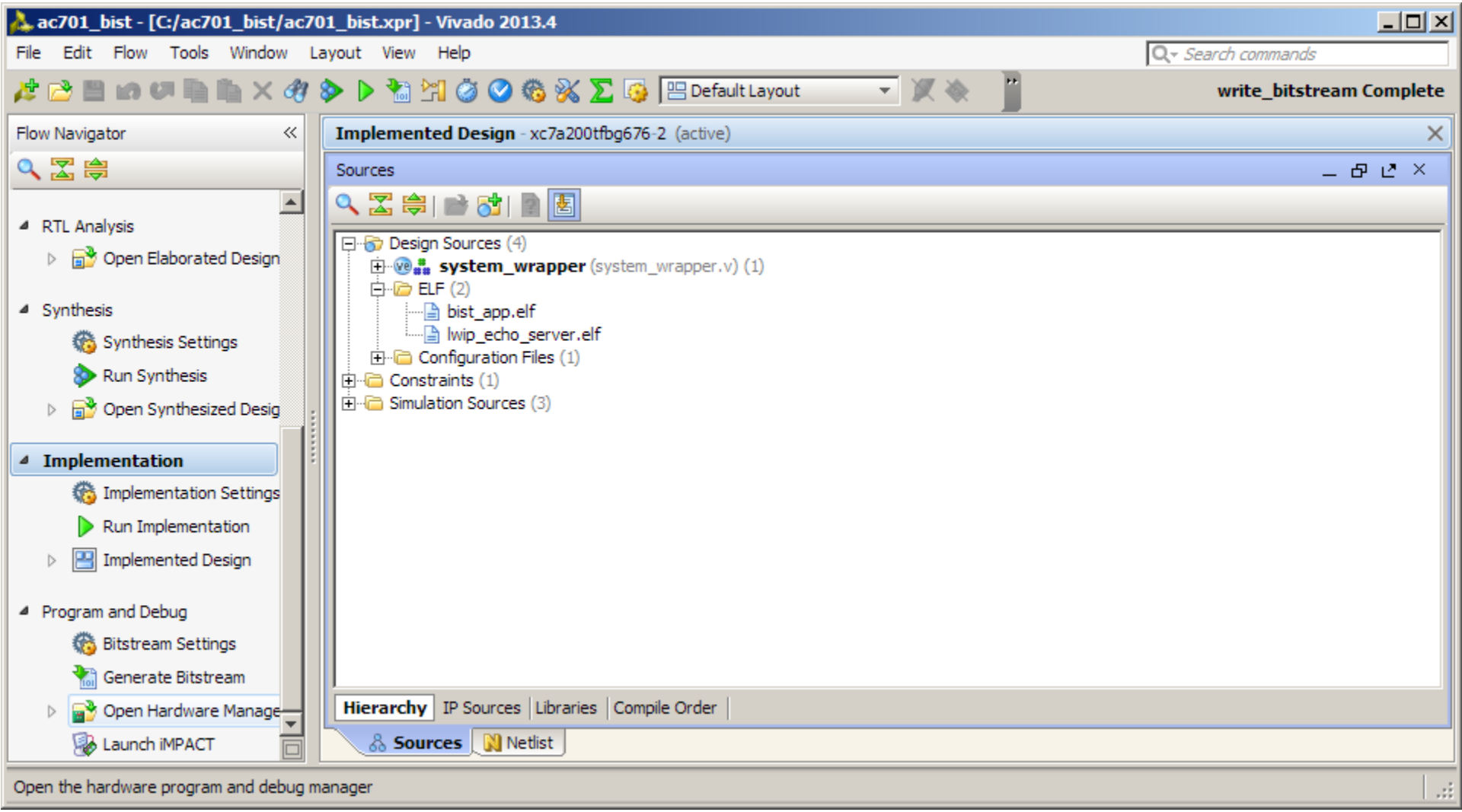
- **Select Generate Bitstream**
  - This creates a bitstream with the BIST ELF file



Note: Presentation applies to the AC701

Program AC701 with BIST Design

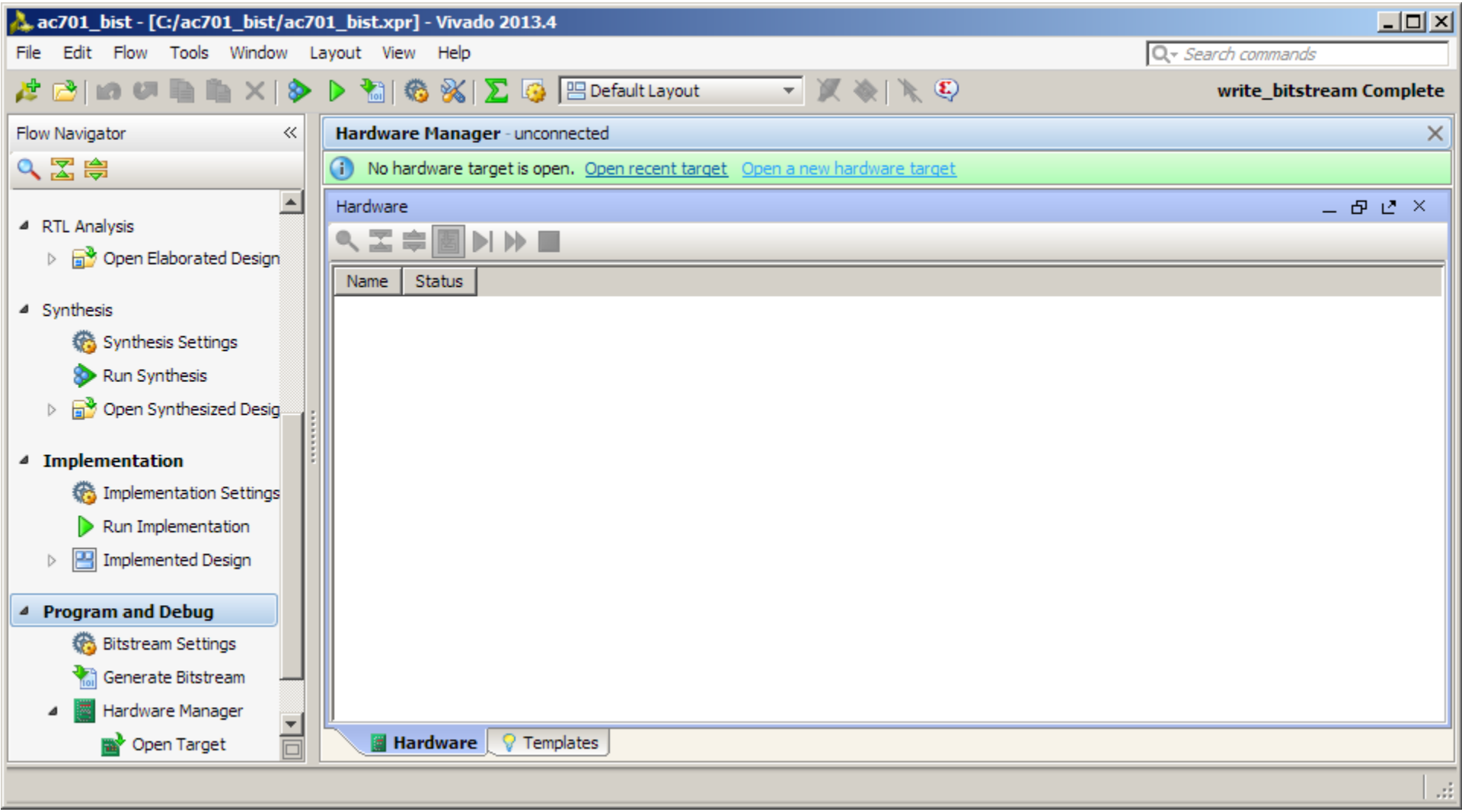
- Click Open Hardware Manager



Note: Presentation applies to the AC701

Program AC701 with BIST Design

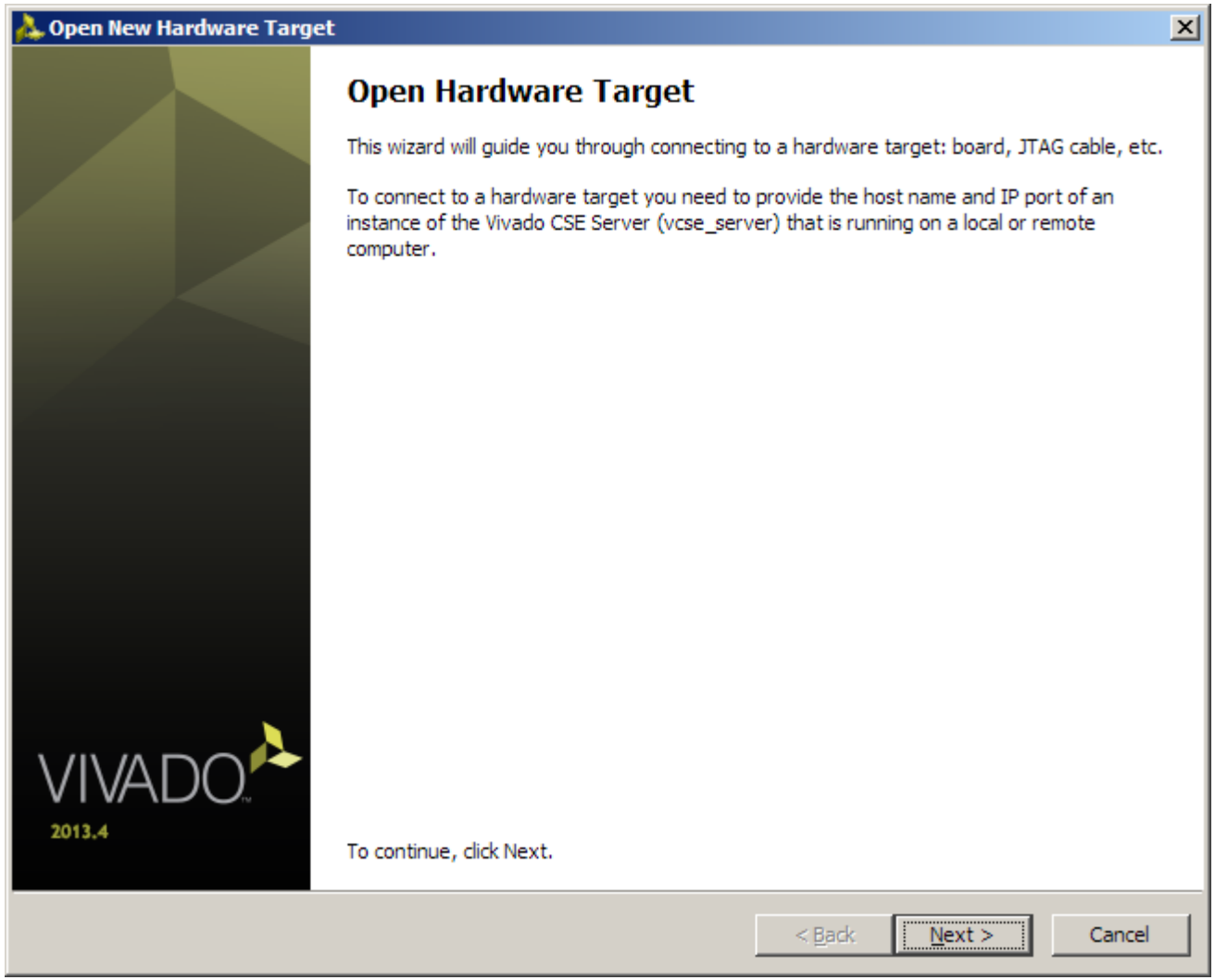
- Click Open a new hardware target



Note: Presentation applies to the AC701

Program AC701 with BIST Design

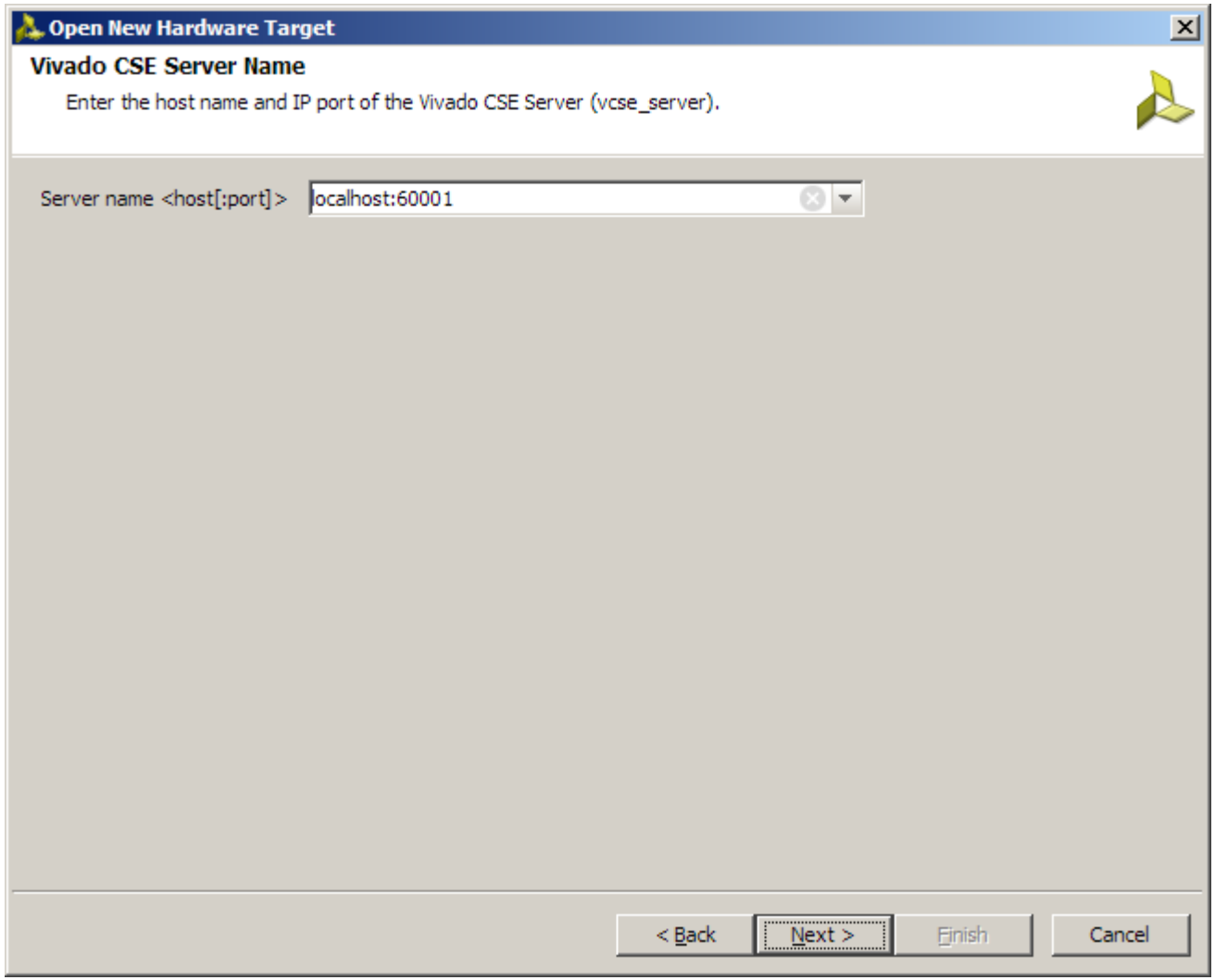
- Click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

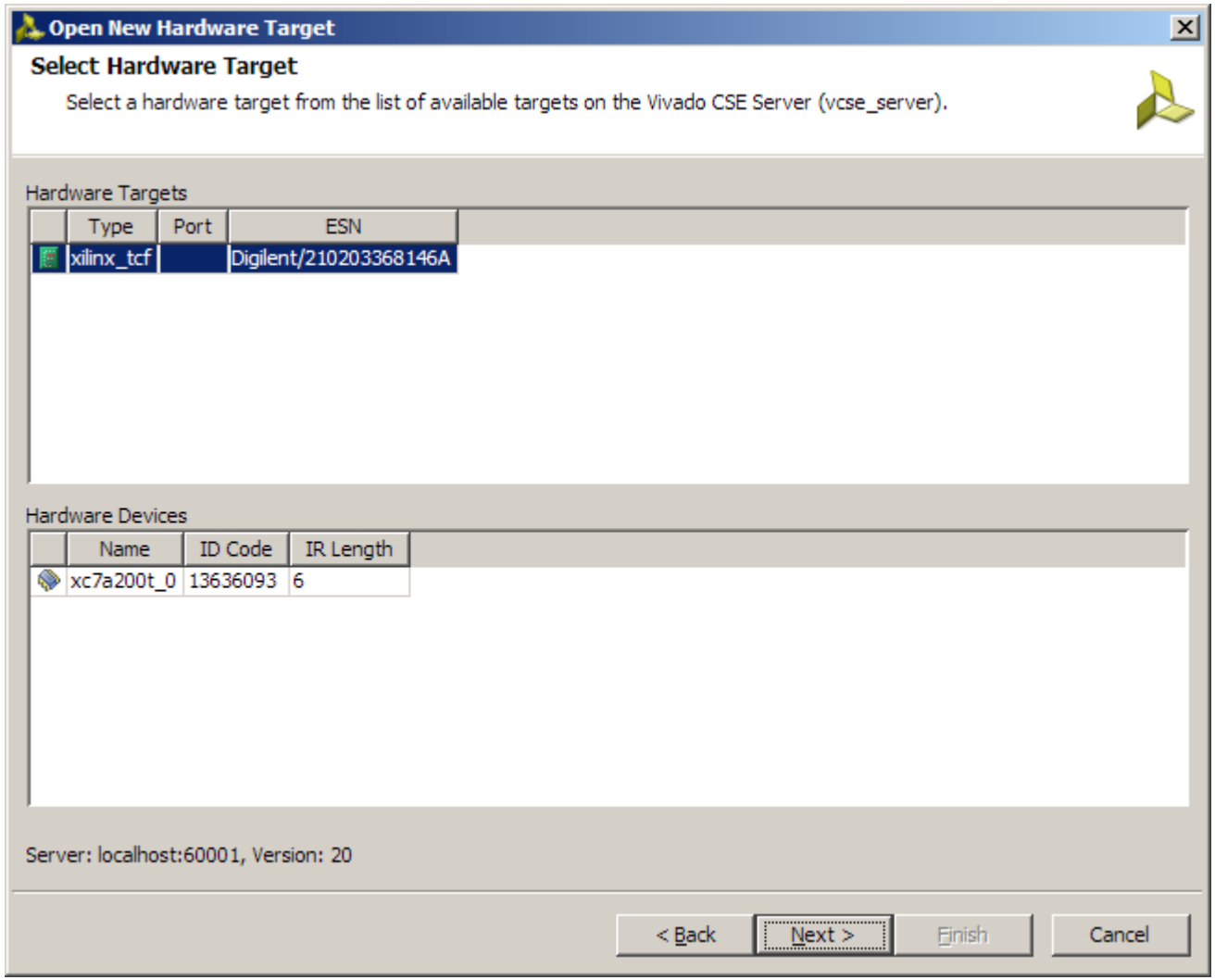
- Click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

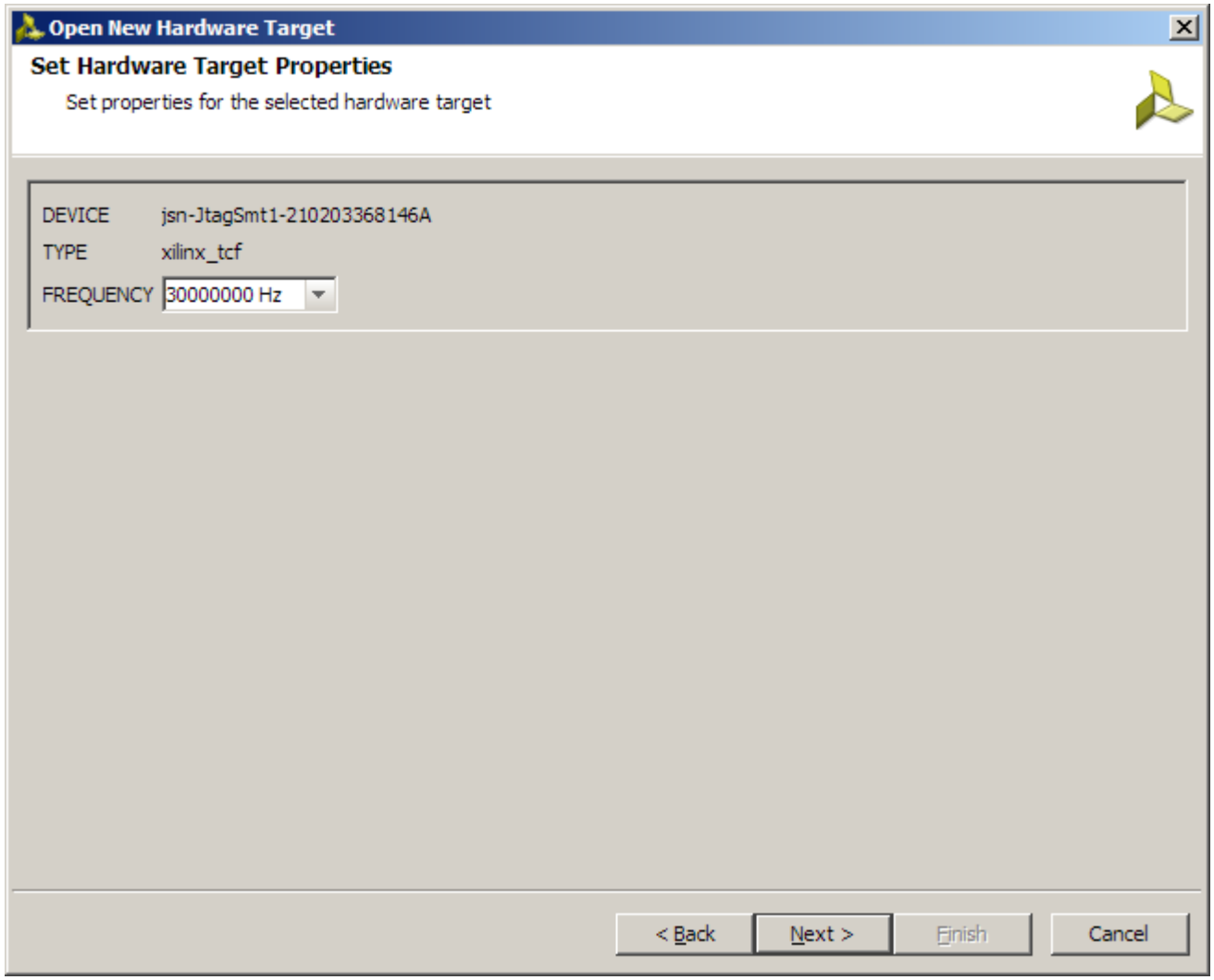
- Click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

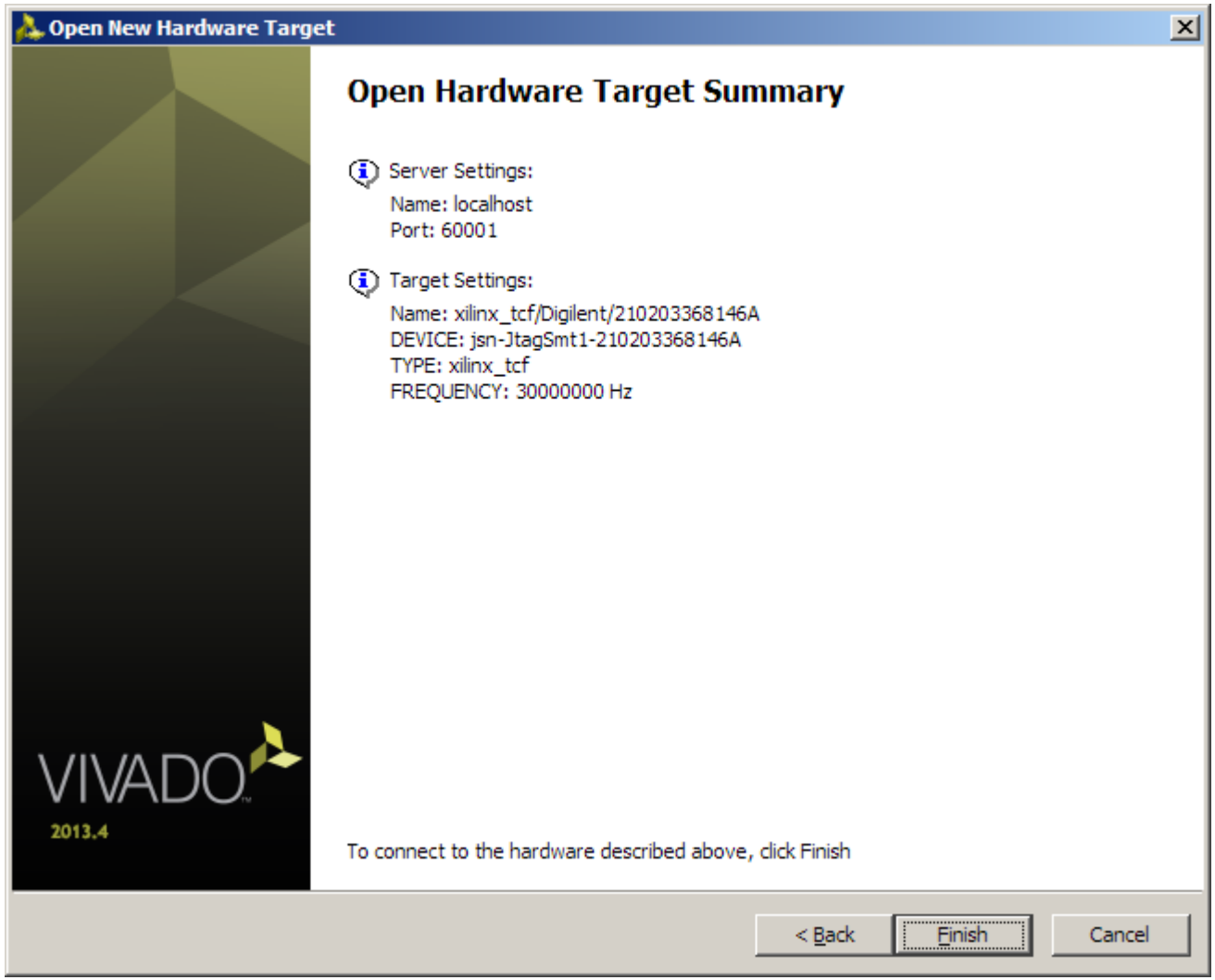
- Set the FREQUENCY to 30000000 Hz (30 MHz) and click Next



Note: Presentation applies to the AC701

Program AC701 with BIST Design

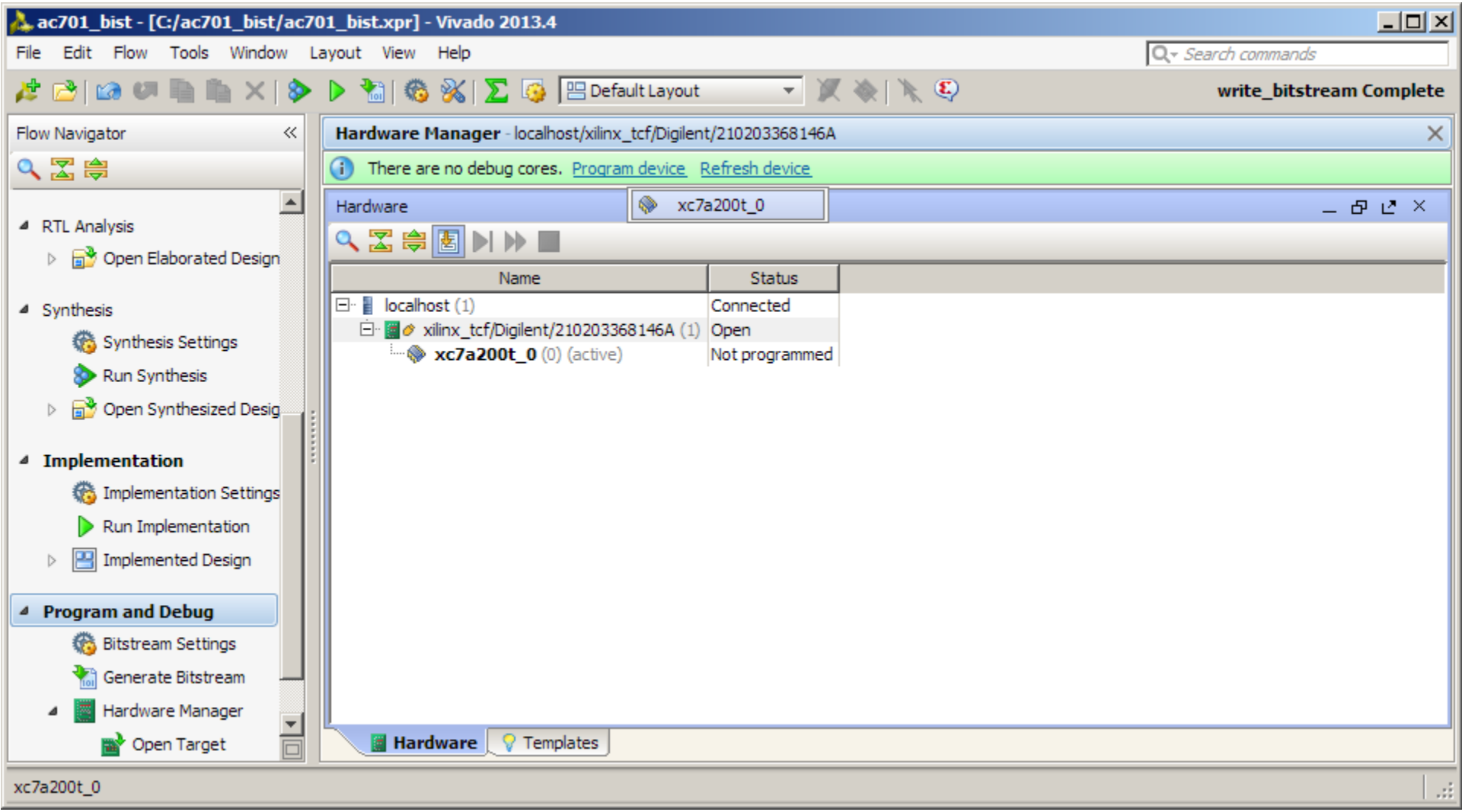
- Click Finish



Note: Presentation applies to the AC701

Program AC701 with BIST Design

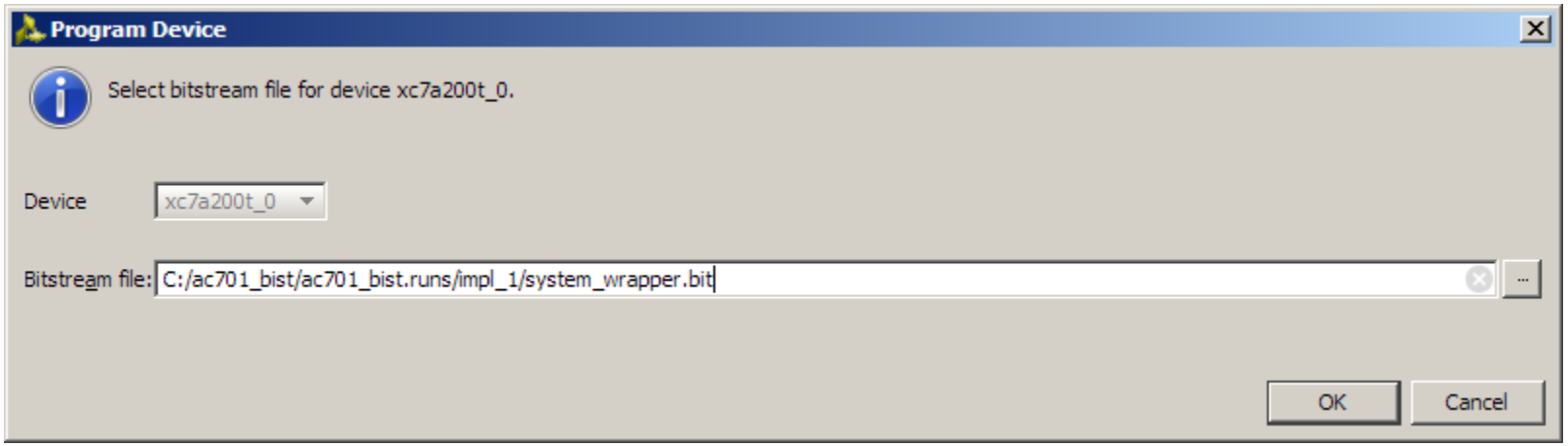
- Select Program device → xc7a200t_0



Note: Presentation applies to the AC701

Program AC701 with BIST Design

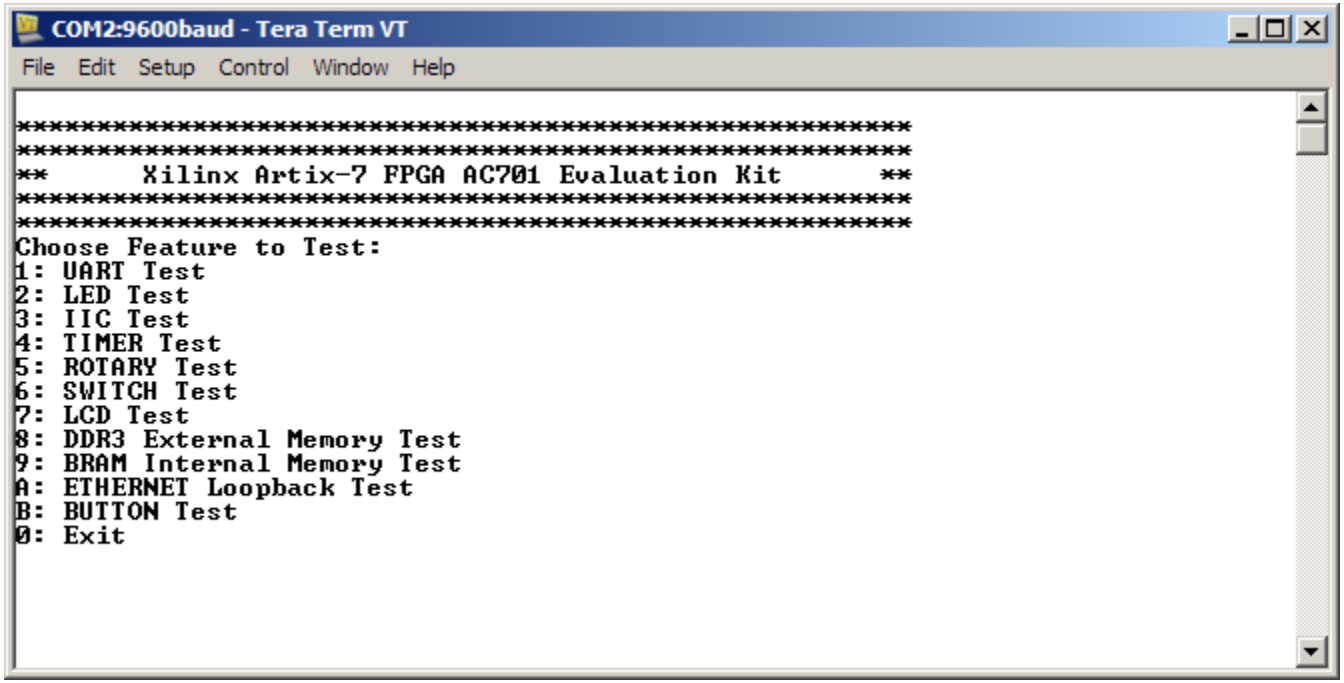
- Program Device defaults to impl_1 bitstream
- Click Program



Note: Presentation applies to the AC701

Program AC701 with BIST Design

- BIST Application runs in the terminal window

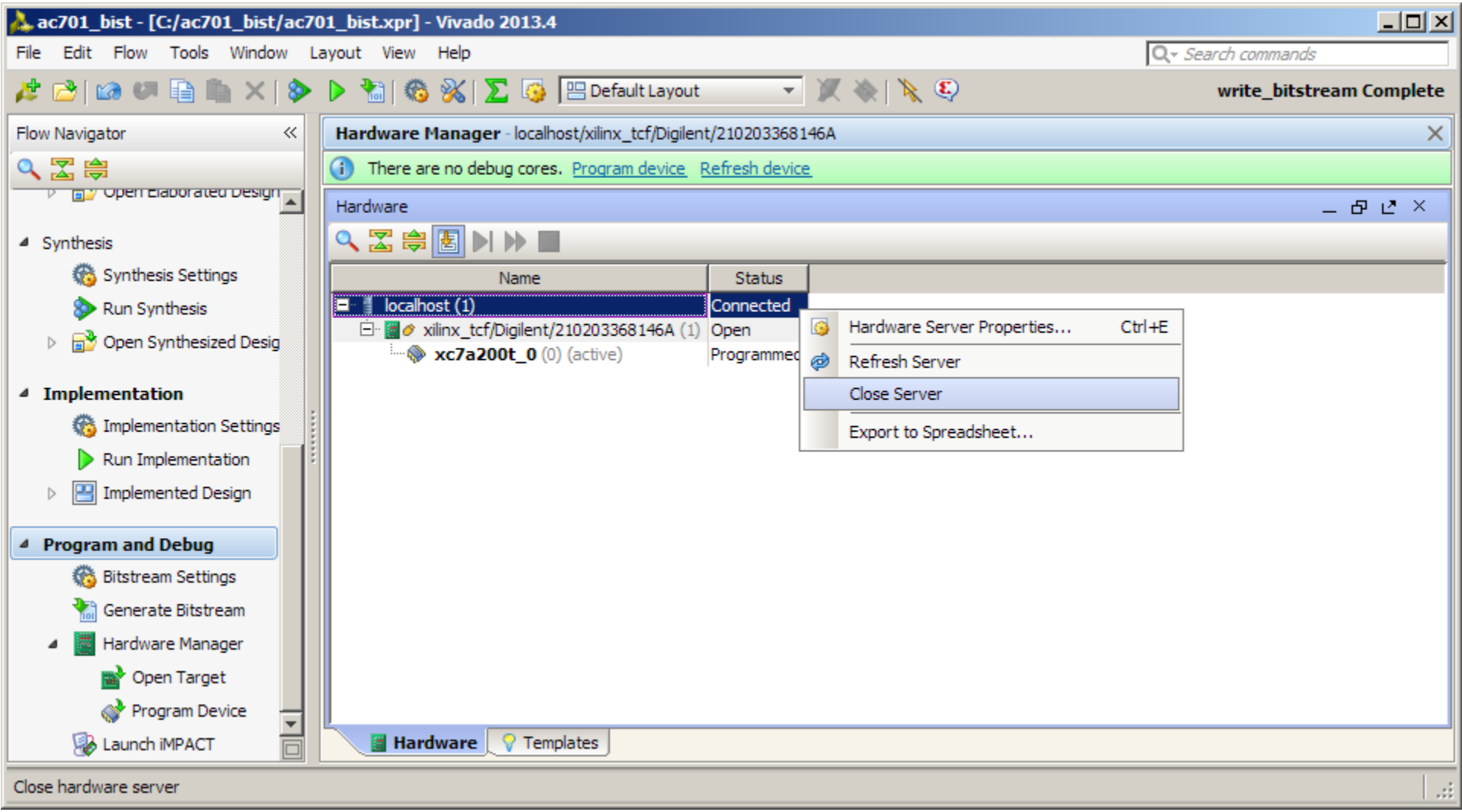


Note: Presentation applies to the AC701

Program AC701 with BIST Design

Close the Server

- Closing the localhost server allows access by a different Vivado instance



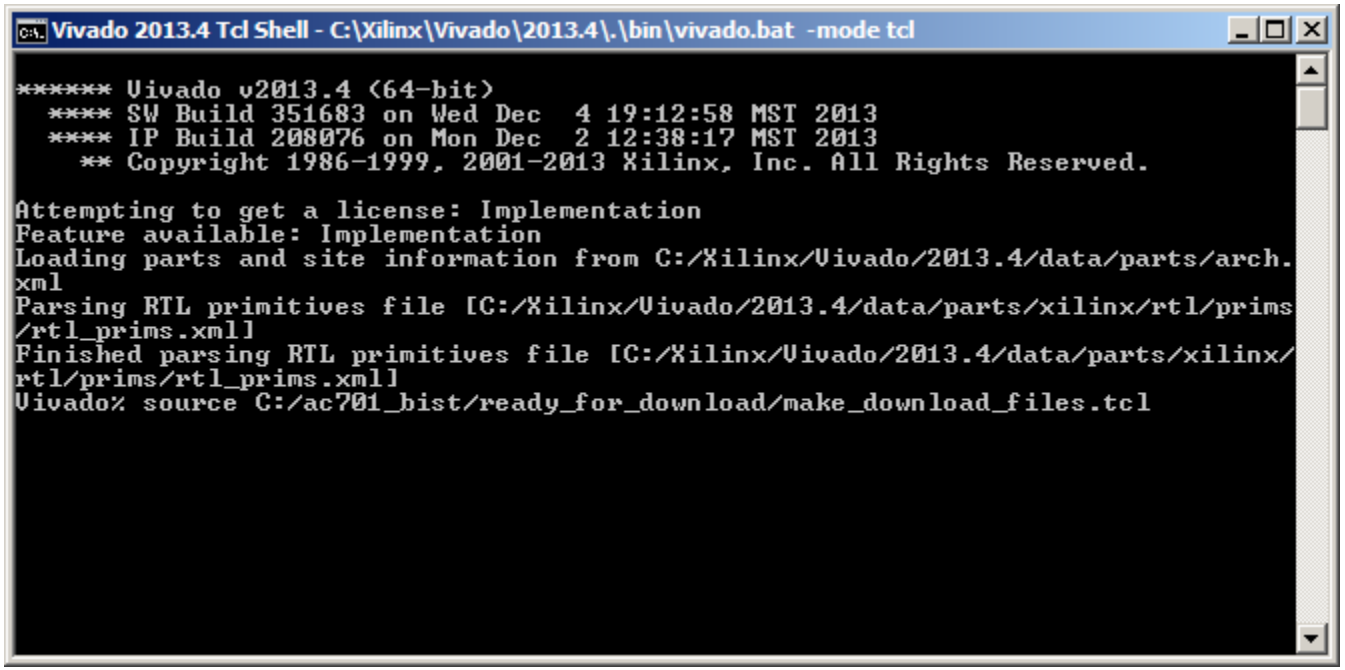
Note: Presentation applies to the AC701

Program AC701 with BIST Design

- Repeat this process using Tcl scripts
- Open a Vivado Tcl shell and type:

  source C:/ac701_bist/ready_for_download/make_download_files.tcl

- This script uses Tcl commands to add the ELF files to the BIST project , then generate both the BIST and LwIP bitstreams

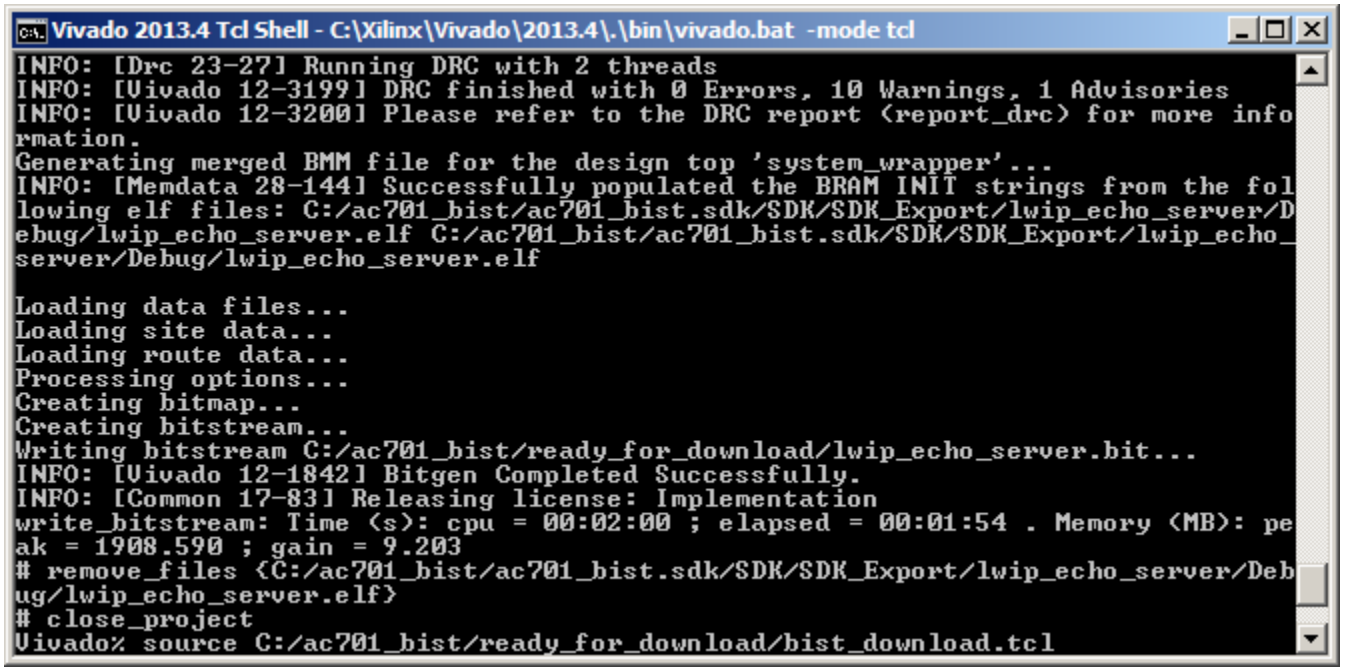


Note: Presentation applies to the AC701

Program AC701 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:

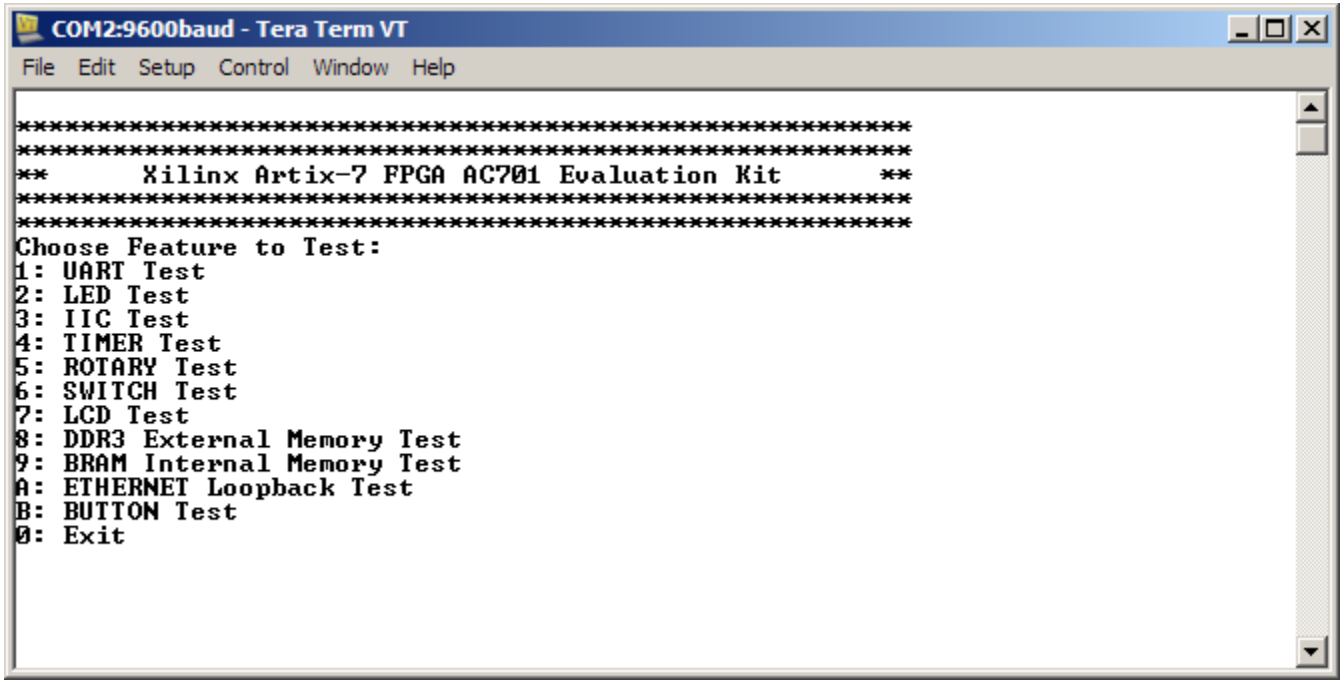
  source C:/ac701_bist/ready_for_download/bist_download.tcl



Note: Presentation applies to the AC701

Program AC701 with BIST Design

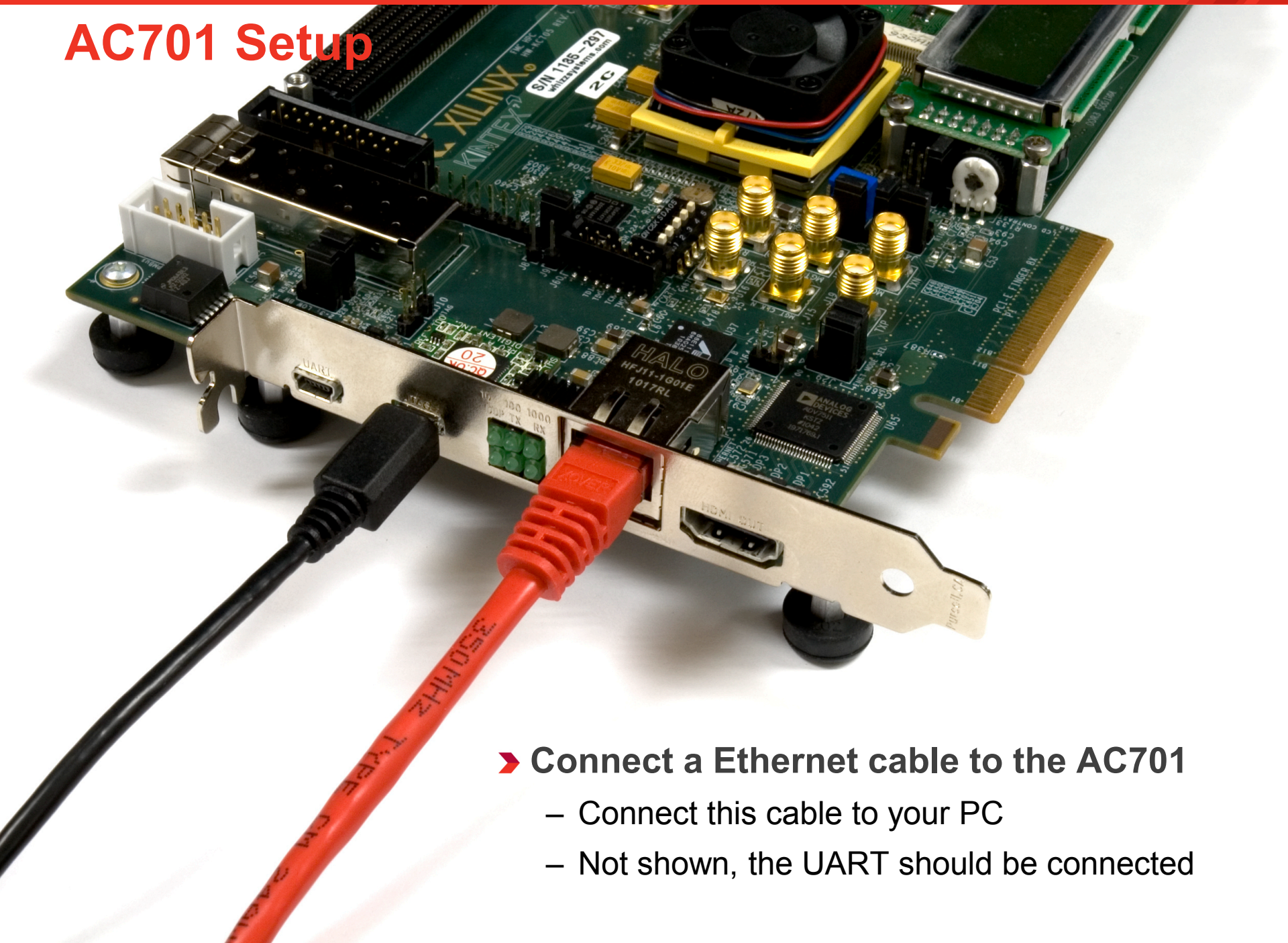
- BIST Application runs in the terminal window



Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

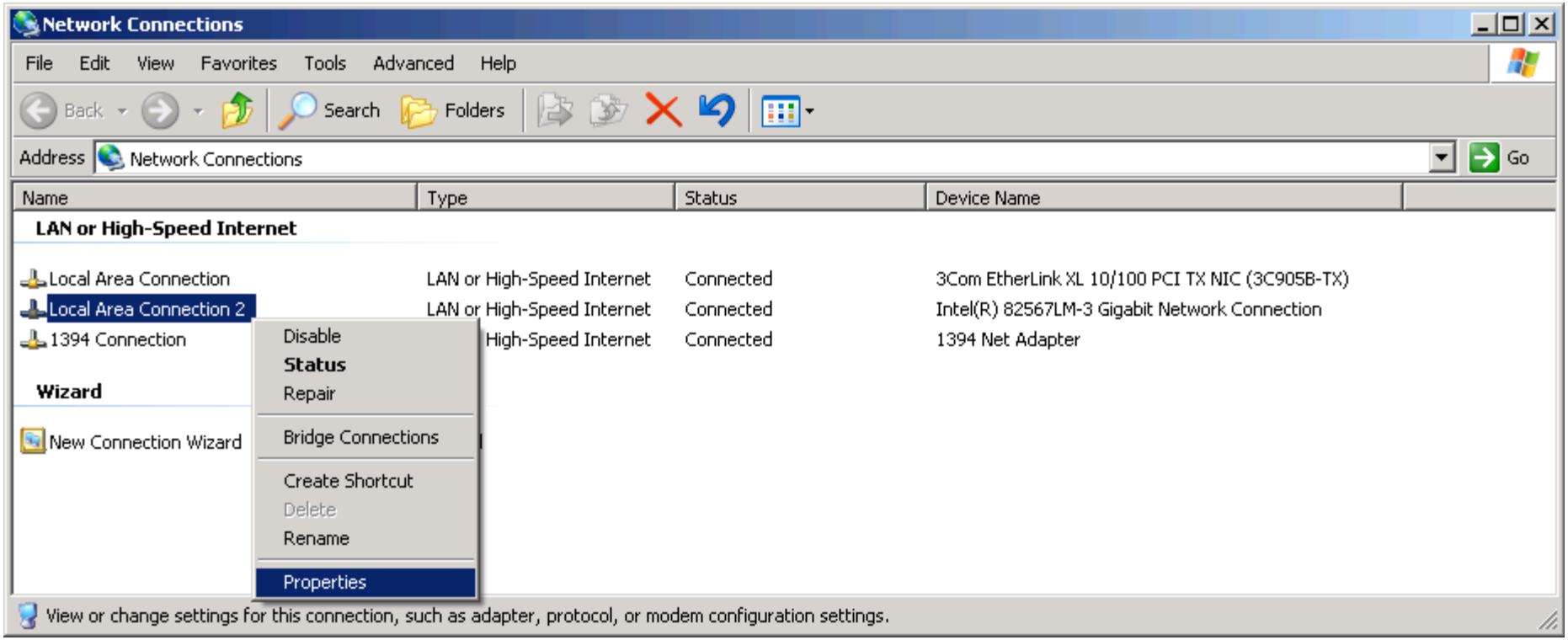
AC701 Setup



- **Connect a Ethernet cable to the AC701**
  - Connect this cable to your PC
  - Not shown, the UART should be connected

Run the LwIP Ethernet Design

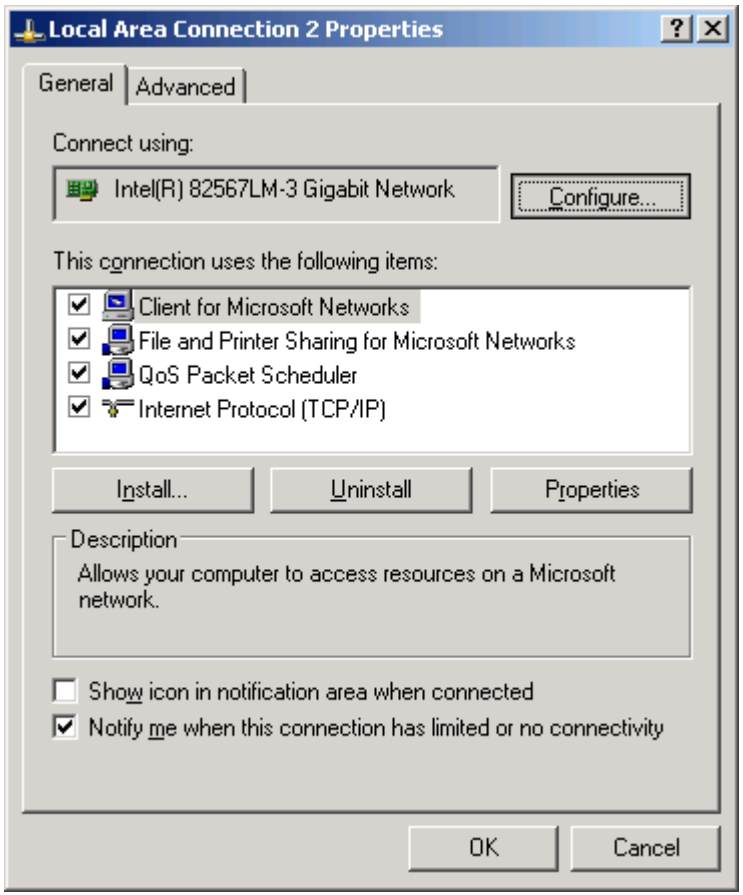
- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties

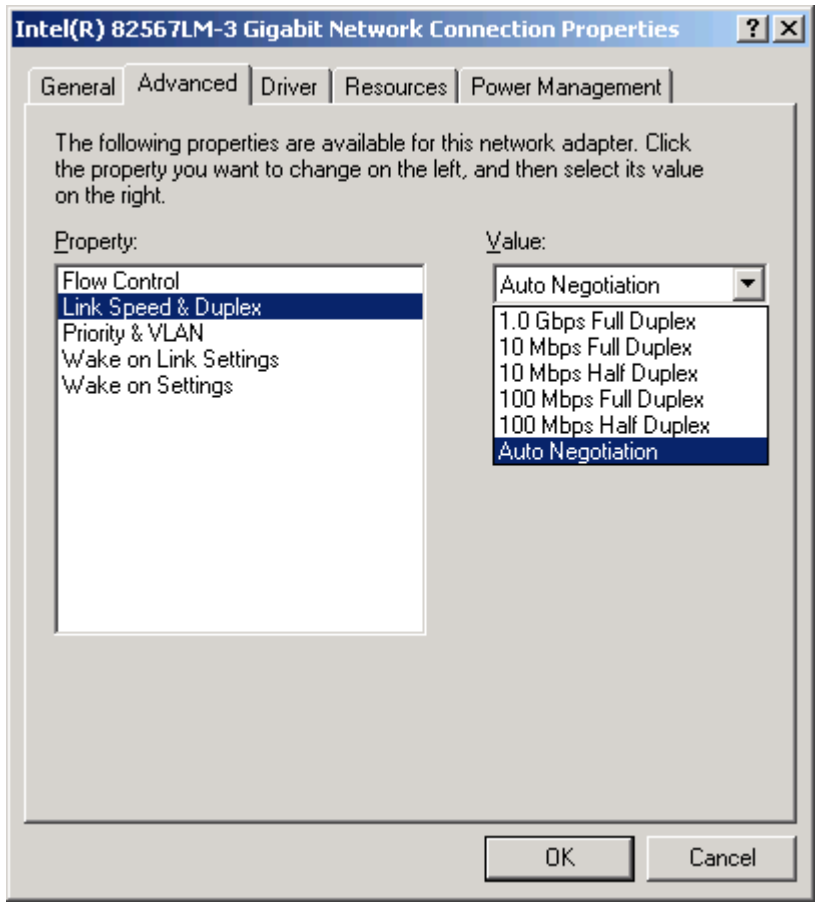


Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

- **Click Configure**
  - Set the Media Type to Auto for 1 Gbps then click OK

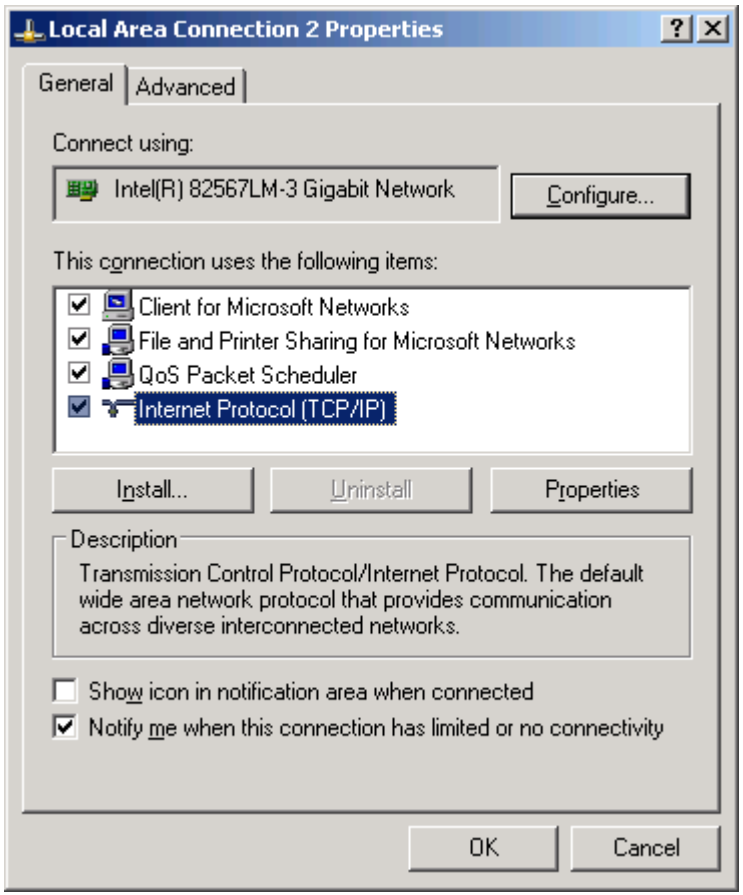


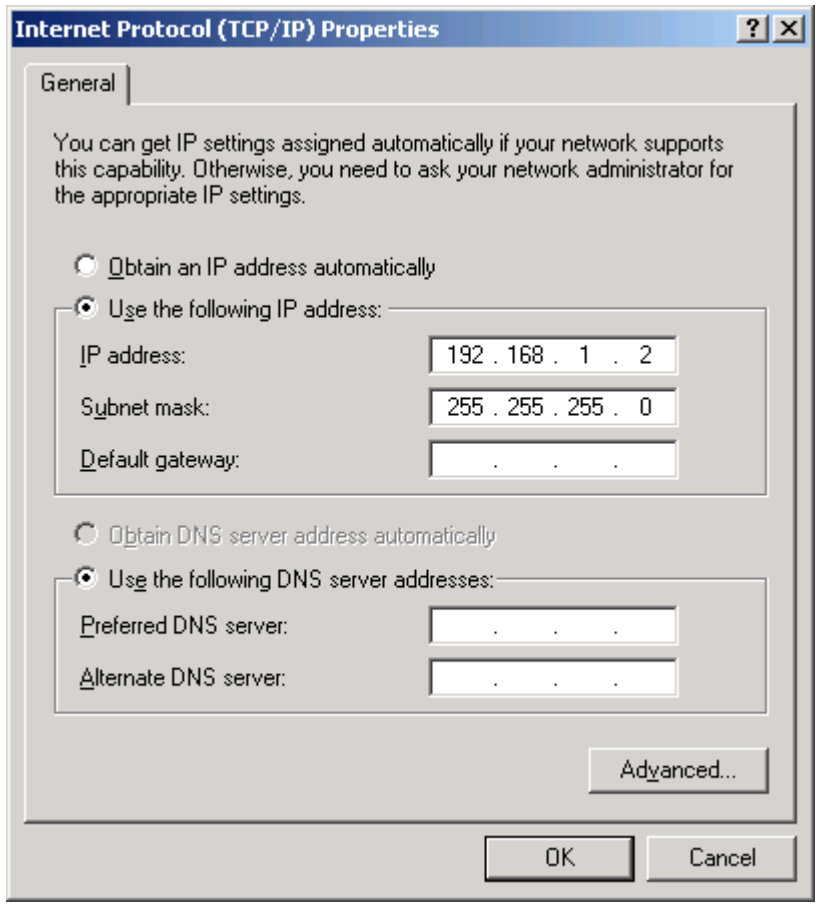


Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:



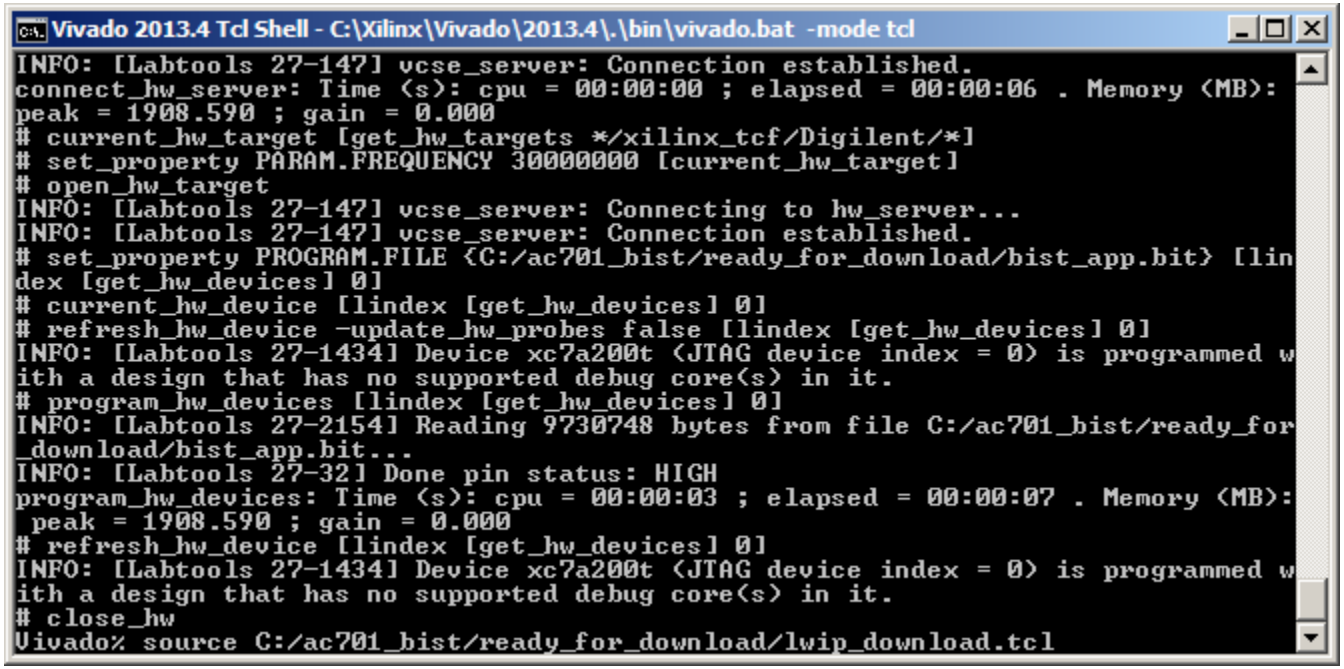


Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

- Download the LwIP bitstream
- In the Vivado Tcl Shell type:

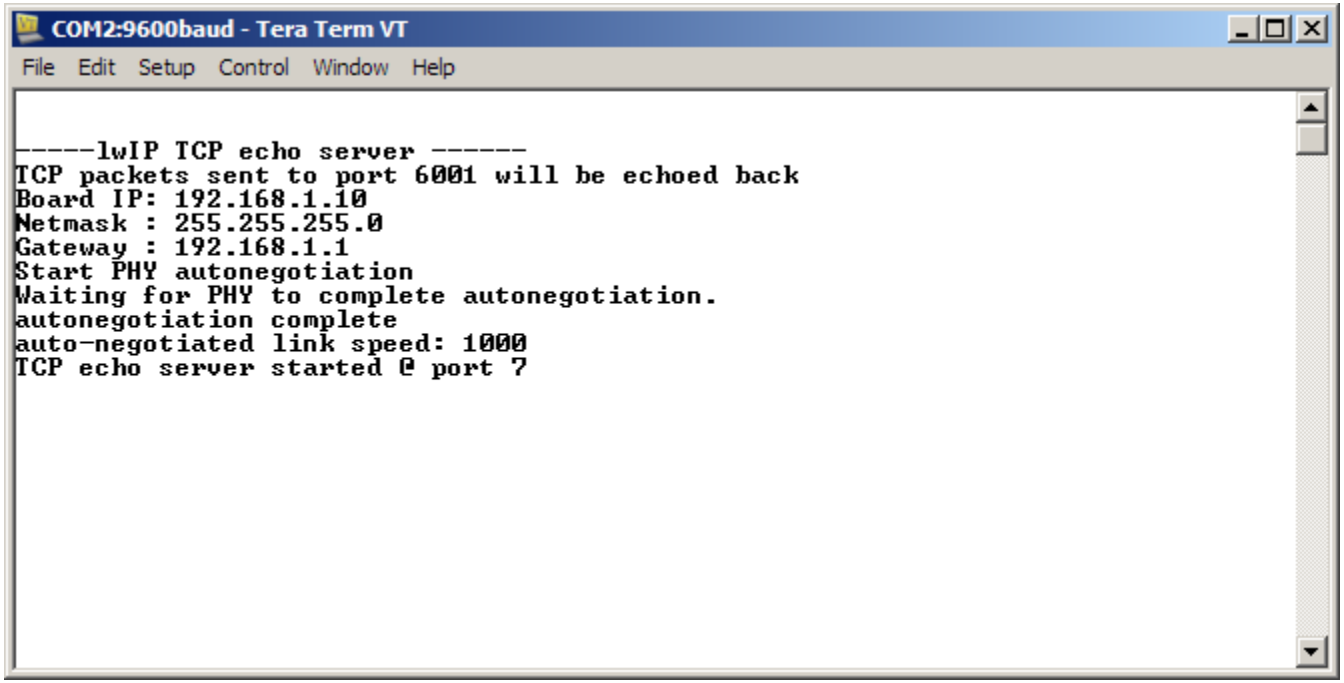
  source C:/ac701_bist/ready_for_download/lwip_download.tcl



Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

- View LwIP echo server screen



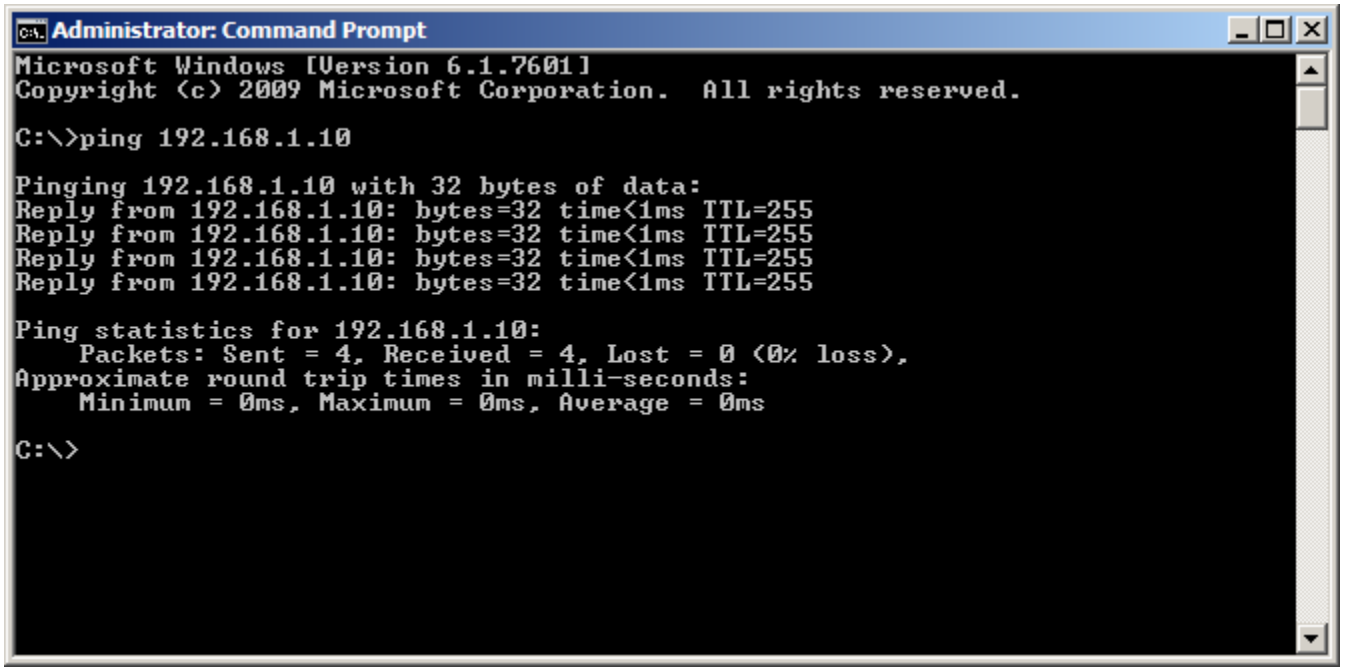
Note: Presentation applies to the AC701

Run the LwIP Ethernet Design

- From a DOS window on the PC Host, enter the command:

  ping 192.168.1.10

  – Ping from PC host 192.168.1.2 to AC701 target 192.168.1.10



Note: Presentation applies to the AC701

References

References

- **IP Integrator Documentation**
  - Vivado Design Suite Tcl Command Reference Guide
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_3/ug835-vivado-tcl-commands.pdf
  - Designing IP Subsystems Using IP Integrator
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2013_3/ug994-vivado-ip-subsystems.pdf
  - IP Release Notes Guide
    - http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf
- **7 Series Configuration**
  - 7 Series FPGAs Configuration User Guide
    - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Documentation

Documentation

- **Artix-7**
  - Artix-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm
  - Design Advisory Master Answer Record for Artix-7 FPGAs
    - http://www.xilinx.com/support/answers/51456.htm
- **AC701 Documentation**
  - Artix-7 FPGA AC701 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-A7-AC701-G.htm
  - AC701 Getting Started Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/2013_2/ug967-ac701-eval-kit-getting-started.pdf
  - AC701 User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/ug952-ac701-a7-eval-bd.pdf