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# **AC701 MIG Design Creation**

**April 2015**

**XTP225**

# Revision History

Date	Version	Description
04/30/14	11.0	Regenerated for 2015.1.
11/24/14	10.0	Regenerated for 2014.4.
10/08/14	9.0	Regenerated for 2014.3.
06/09/14	8.0	Regenerated for 2014.2.
04/16/14	7.0	Regenerated for 2014.1.
12/18/13	6.0	Regenerated for 2013.4.
10/23/13	5.0	Regenerated for 2013.3.
06/19/13	4.0	Regenerated for 2013.2. AR55531 fixed.
04/03/13	3.0	Regenerated for 2013.1. AR53420 fixed. Added AR55531.
02/04/13	2.1	As per AR54044, added 2012.4 device pack. Added AR53420 and AR54223.
12/18/12	2.0	Regenerated for 2012.4
10/23/12	1.0	Initial Version.

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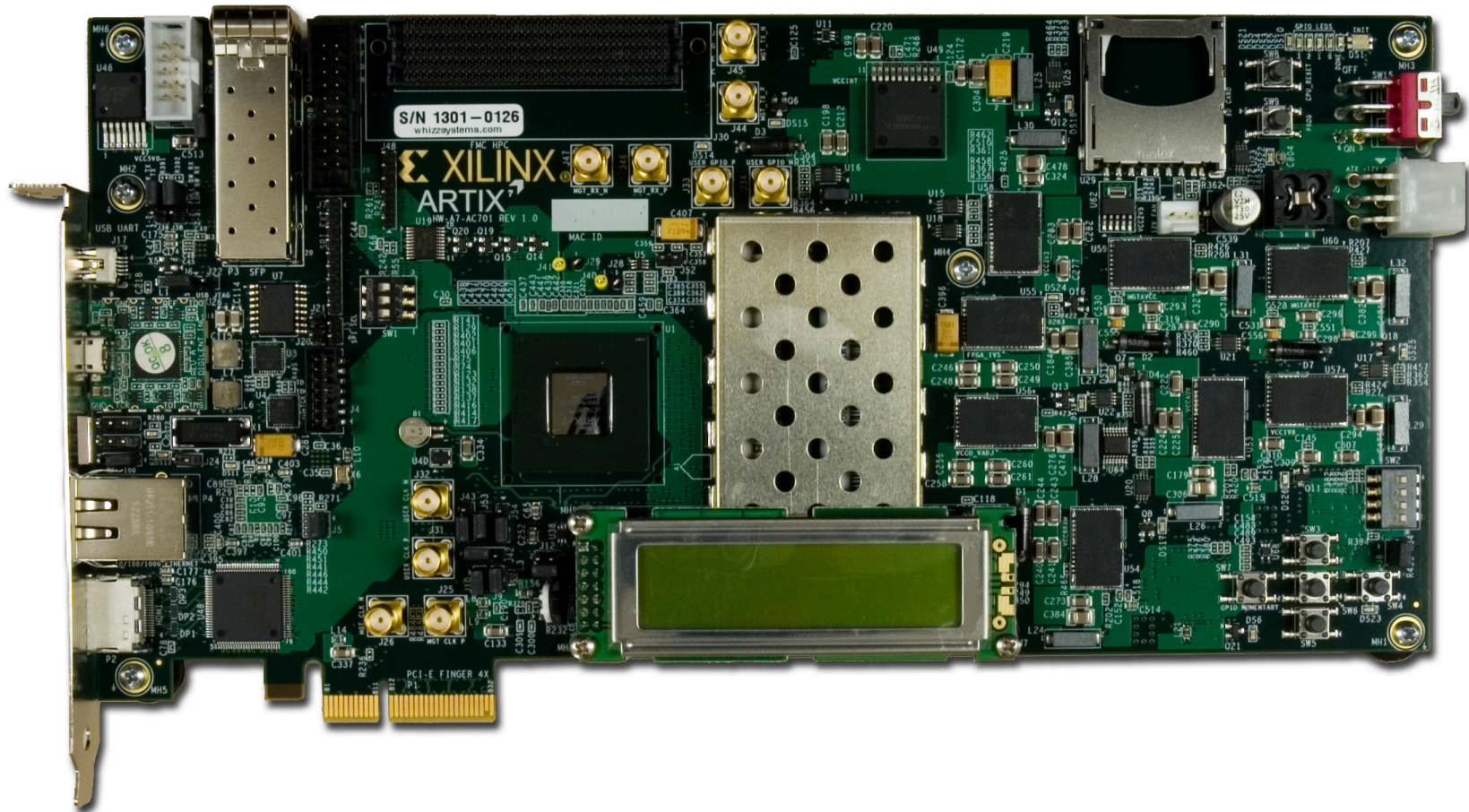
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# Overview

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- **AC701 Setup**
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- **References**

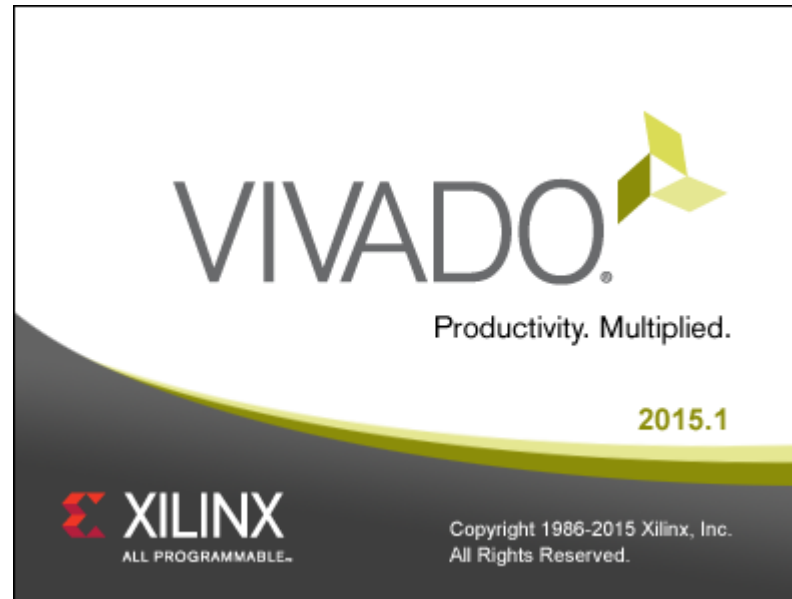
# Xilinx AC701 Board





# Vivado Software Requirements

➤ Xilinx Vivado Design Suite 2015.1, Design Edition

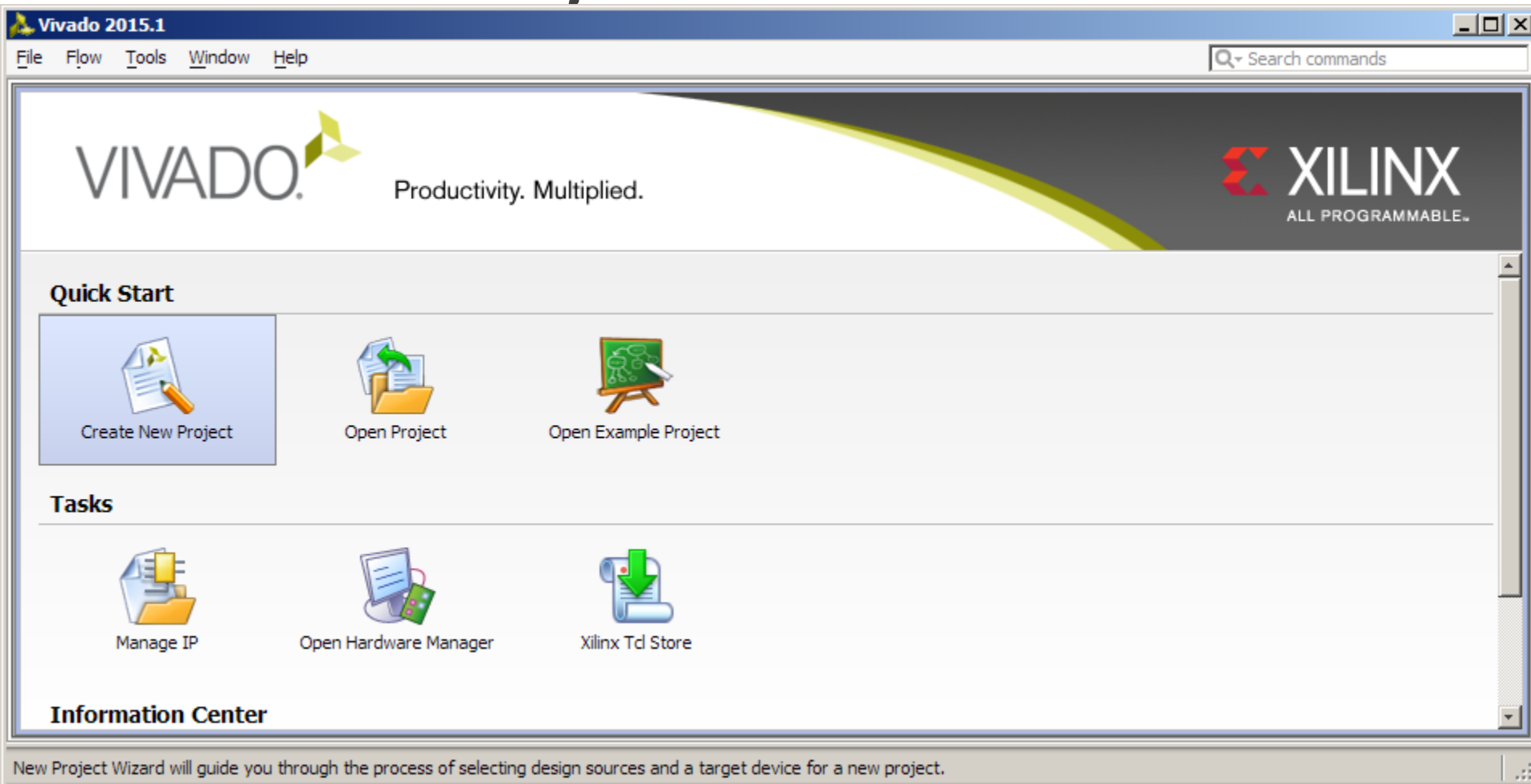


# Generate MIG Example Design

## ➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

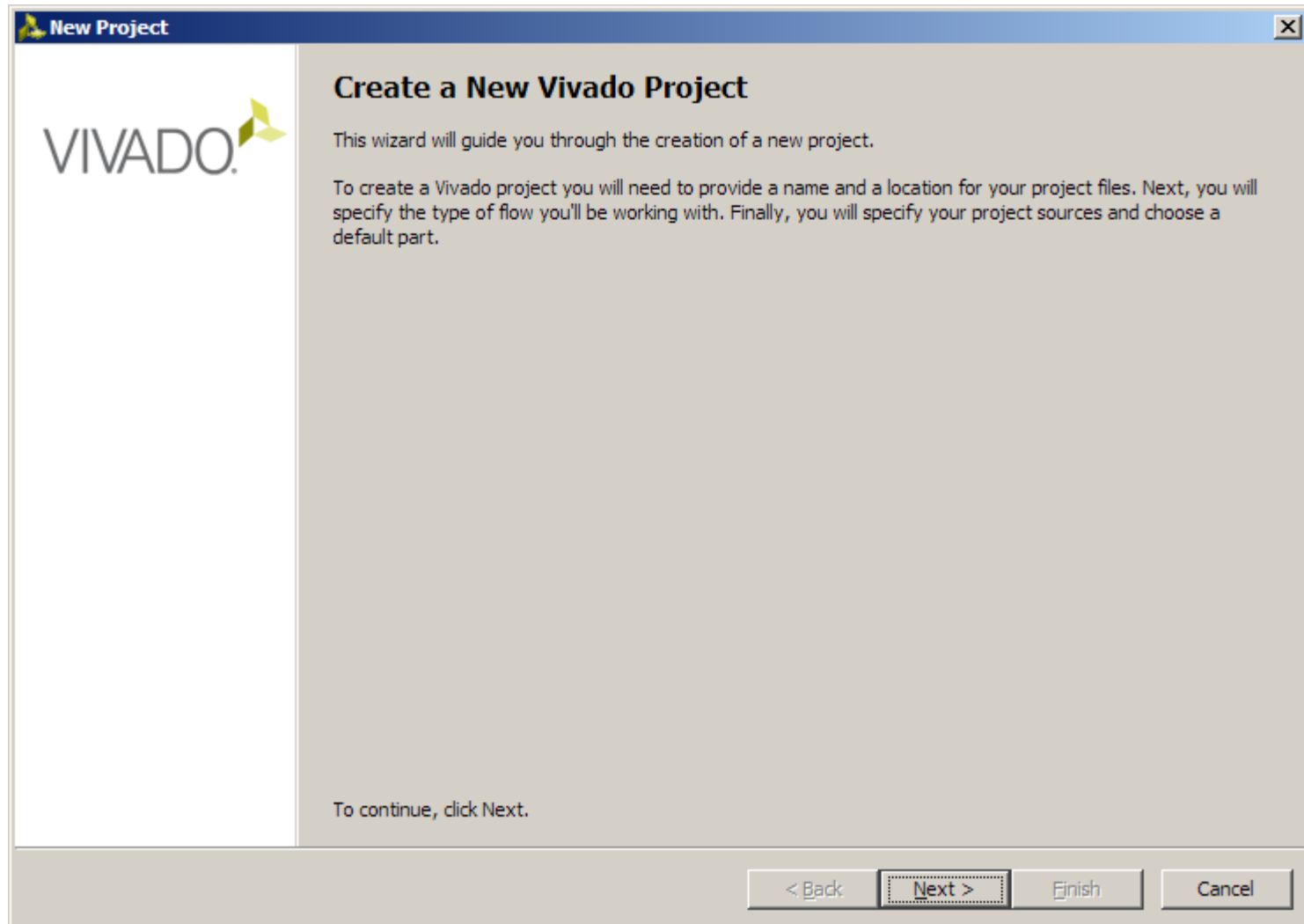
## ➤ Select Create New Project



**Note:** Presentation applies to the AC701

# Generate MIG Example Design

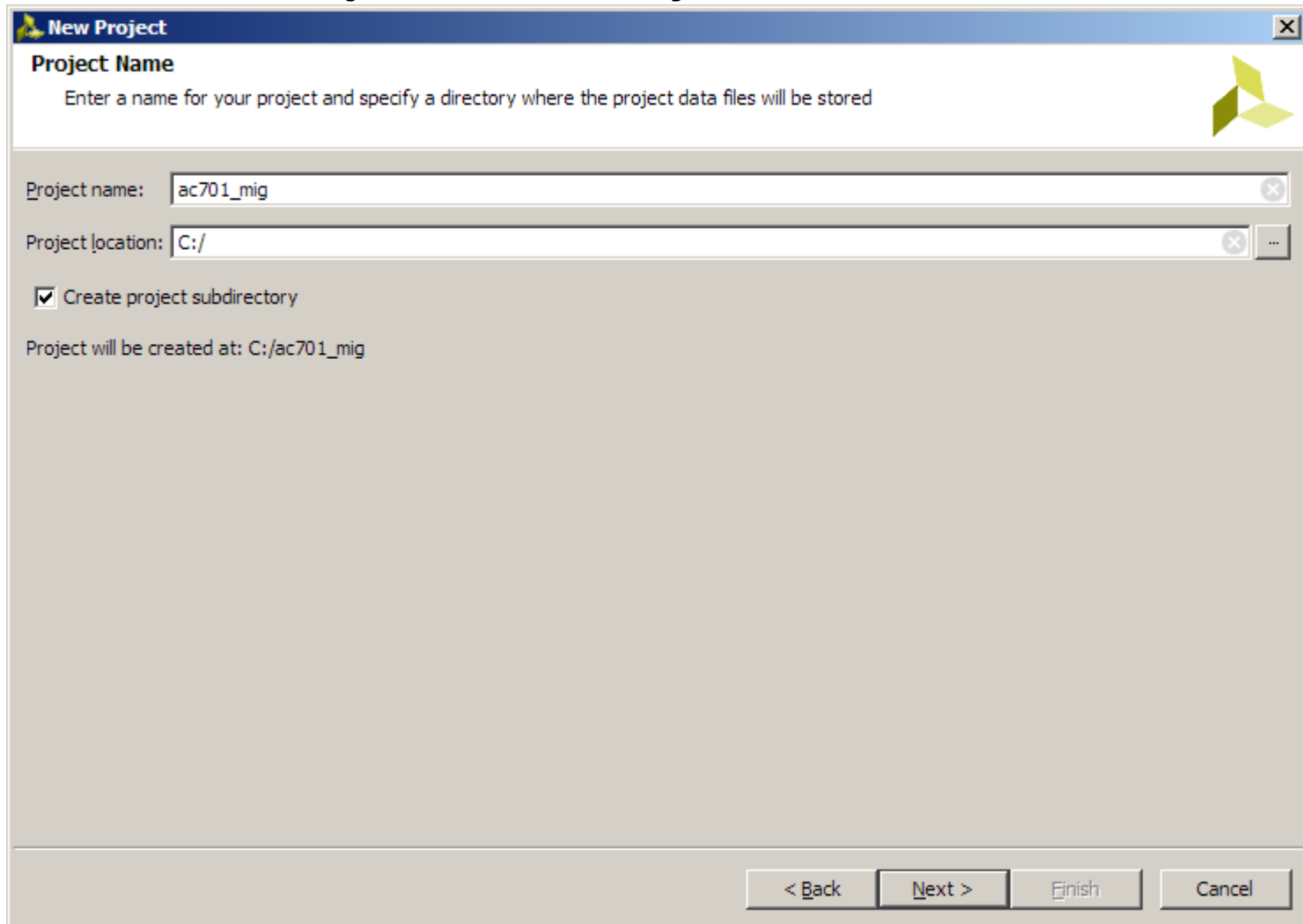
➤ Click Next



**Note:** Presentation applies to the AC701

# Generate MIG Example Design

- Set the Project name and location to ac701\_mig and C:\ul>- Check **Create Project Subdirectory**



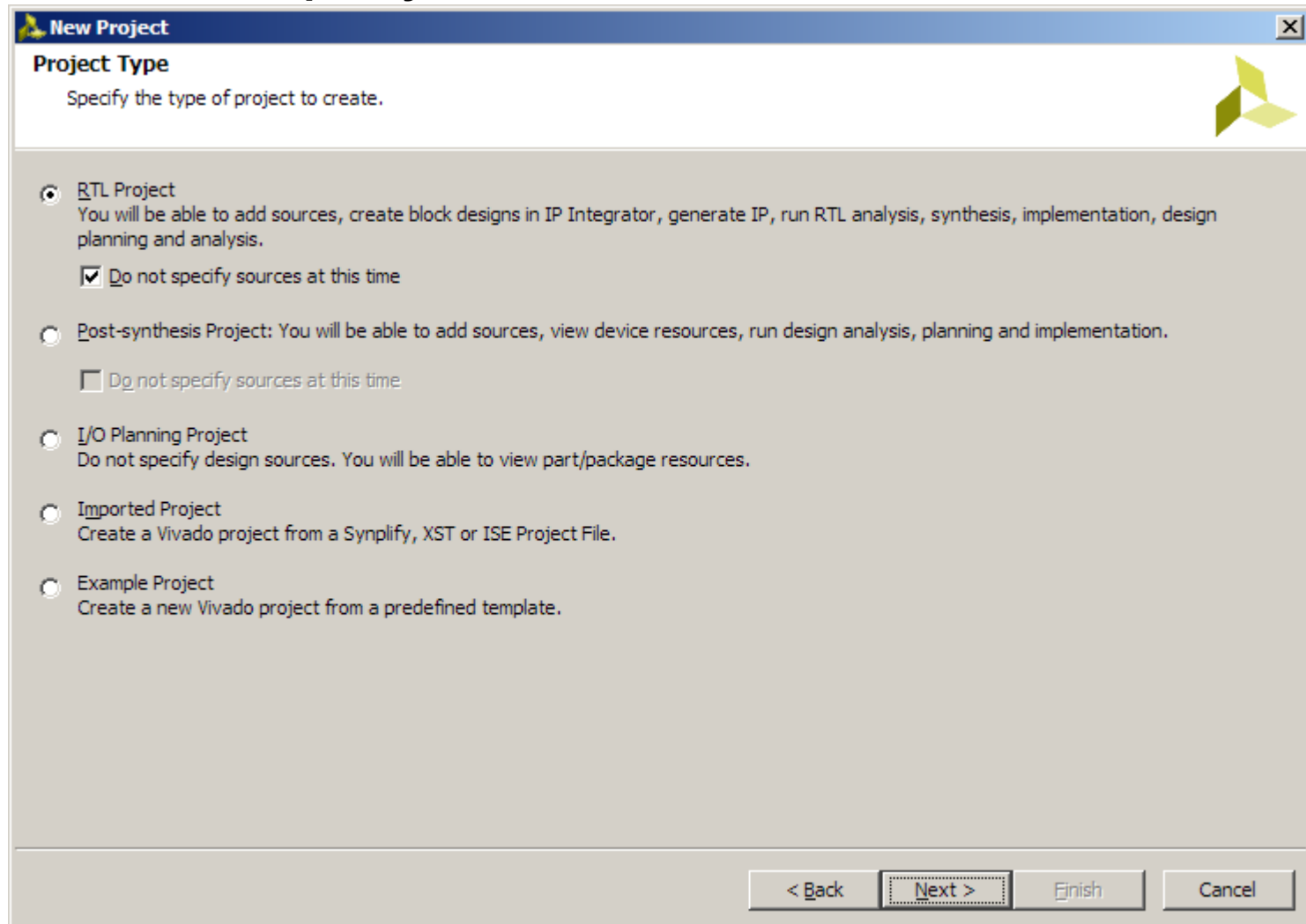
**Note:** Vivado generally requires forward slashes in paths



# Generate MIG Example Design

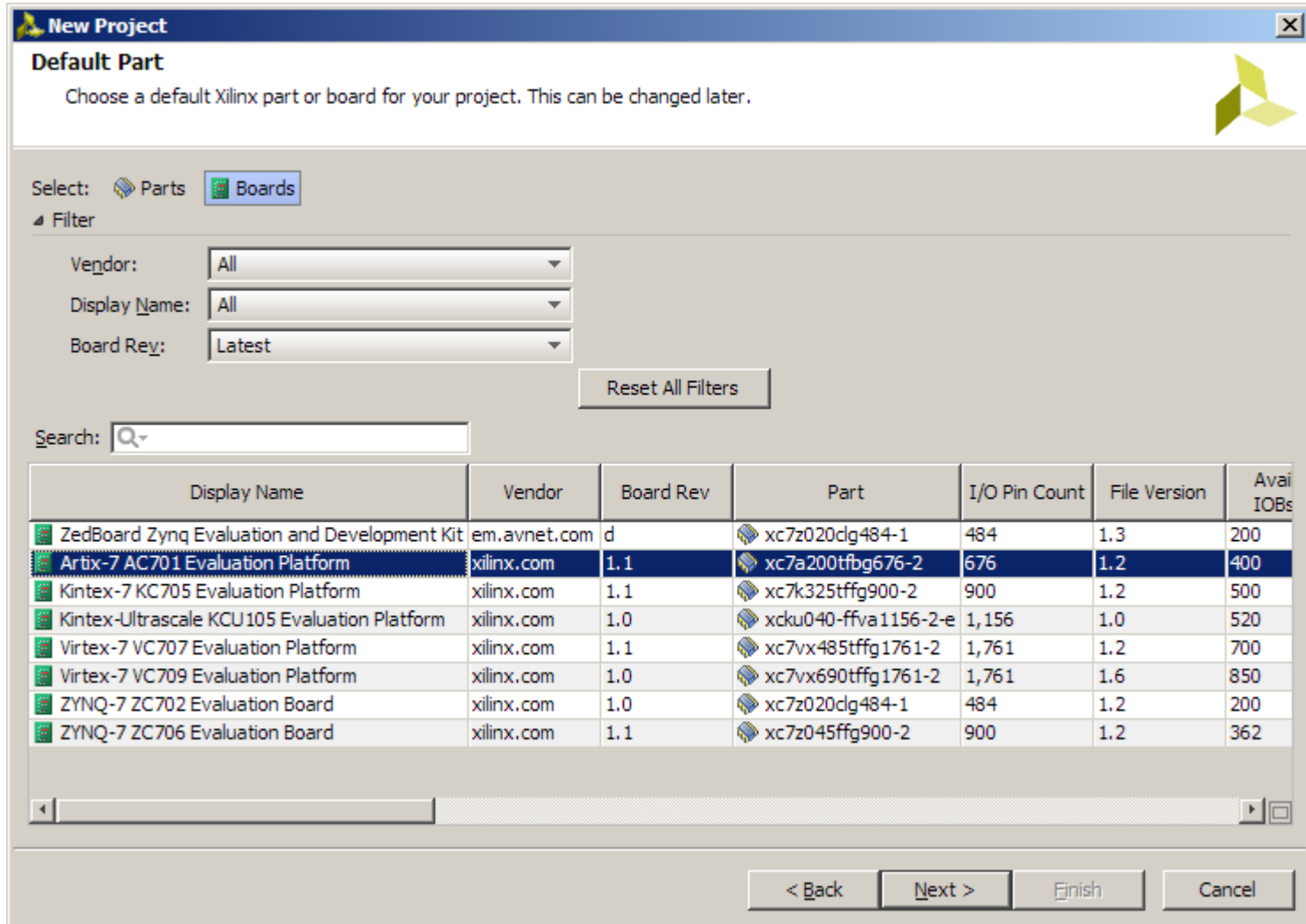
## ➤ Select RTL Project

- Select **Do not specify sources at this time**



# Generate MIG Example Design

## ➤ Select the AC701 Board



The screenshot shows the 'New Project' dialog box with the 'Default Part' section. The 'Boards' tab is selected, and the 'Artix-7 AC701 Evaluation Platform' is highlighted in the list. The filters are set to 'Vendor: All', 'Display Name: All', and 'Board Rev: Latest'. The search bar is empty. The table below shows the list of boards and their details.

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020d1g484-1	484	1.3	200
<b>Artix-7 AC701 Evaluation Platform</b>	<b>xilinx.com</b>	<b>1.1</b>	<b>xc7a200t1bg676-2</b>	<b>676</b>	<b>1.2</b>	<b>400</b>
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcku040-ffva1156-2-e	1,156	1.0	520
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.2	700
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020d1g484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.2	362

Note: Presentation applies to the AC701

# Generate MIG Example Design

➤ Click Finish



**Note:** Presentation applies to the AC701

# Generate MIG Example Design

➤ Click on IP Catalog

The screenshot displays the Vivado 2015.1 software interface for a project named 'ac701\_mig'. The 'Project Manager' window is open, showing a tree view of sources including 'Design Sources', 'Constraints', 'Simulation Sources', and 'sim\_1'. The 'IP Catalog' option is highlighted with a red box in the left-hand 'Project Manager' sidebar. The 'Project Summary' window is also open, showing the implementation status. The 'Design Runs' window at the bottom shows a table of design runs.

Name	Constraints	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs
synth_1	constrs_1										
impl_1	constrs_1										

Note: Presentation applies to the AC701



# Generate MIG Example Design

➤ Select MIG 7 Series, v2.3 under Memory Interface Generators

The screenshot shows the Vivado 2015.1 Project Manager interface. The 'IP Catalog' tab is active, displaying a list of IP blocks. The 'Memory Interface Generator (MIG 7 Series)' is selected, and its details are shown in the 'Details' pane below the table.

Name	Version	AXI4	Status	License
Embedded Processing				
FPGA Features and Design				
Math Functions				
Memories & Storage Elements				
ECC	2.0		Production	Included
FIFOs				
Memory Interface Generators				
<b>Memory Interface Generator (MIG 7 Series)</b>	<b>2.3</b>	<b>AXI4</b>	<b>Production</b>	<b>Included</b>
RAMs & ROMs				
Partial Reconfiguration				
Standard Bus Interfaces				
Video & Image Processing				

**Details**

Name: **Memory Interface Generator (MIG 7 Series)**  
Version: 2.3 (Rev. 1)  
Interfaces: AXI4  
Description: This Memory Interface Generator is a simple menu-driven tool to generate advanced memory interfaces. This tool

IP: Memory Interface Generator (MIG 7 Series)

Note: Presentation applies to the AC701

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# Generate MIG Example Design

- Right click on MIG 7 Series
- Select Customize IP

The screenshot shows the Vivado 2015.1 Project Manager interface. The main window displays the IP Catalog for the project 'ac701\_mig'. The 'Memory Interface Generator (MIG 7 Series)' is selected, and a context menu is open over it, with 'Customize IP...' highlighted. The IP Catalog table is as follows:

Name	Version	AXI4	Status	License
Embedded Processing				
FPGA Features and Design				
Math Functions				
Memories & Storage Elements				
ECC	2.0		Production	Included
FIFOs				
Memory Interface Generators				
Memory Interface Generator (MIG 7 Series)	2.3 (Rev. 1)	AXI4	Production	Included
RAMs & ROMs				
Partial Reconfiguration				
Standard Bus Interfaces				
Video & Image Processing				

The context menu options are: Properties... (Ctrl+E), **Customize IP...**, License Status, Compatible Families, Change Log, Product Webpage, Answer Records, IP Settings..., Add Repository..., Refresh All Repositories, and Export to Spreadsheet...

Note: Presentation applies to the AC701

# Generate MIG Example Design



- Leave this page as is
  - Click Next

# Generate MIG Example Design

- Leave this page as is
  - Click Next

MIG Output Options

**Create Design**

Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.

**Verify Pin Changes and Update Design**

Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.

Component Name

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example\_design", "user\_design" and "docs". The user\_design will contain the generated memory interface. The example\_design adds a simple example application connected to the generated memory interface.

**Component Name**

Multi-Controller

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDR II + SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information

**Number of Controllers**

AXI4 Interface

Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.

**AXI4 Interface**

< Back    Next >    Cancel



# Generate MIG Example Design

- Leave this page as is
  - Click Next

REFERENCE DESIGN

Pin Compatible FPGAs

Memory Selection

Controller Options

AXI Parameter

Memory Options

FPGA Options

Extended FPGA Options

IO Planning Options

Bank Selection

System Signals Selection

Summary

Simulation Options

PCB Information

Design Notes

Pin Compatible FPGAs

Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible\_ucf folder. **If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required.** MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.

A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.

Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.

Target FPGA

User Guide Version Info < Back Next > Cancel

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Note: Presentation applies to the AC701

# Generate MIG Example Design



## ➤ Select Memory Type

- DDR3 SDRAM
- Click Next

# Generate MIG Example Design

Options for Controller 0 - DDR3 SDRAM

**Clock Period:** Choose the clock period for the desired frequency. The allowed period range(2500 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information. 2500 ps 400.00 MHz

**PHY to Controller Clock Ratio:** Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices. 4:1

**Memory Type:** Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above. SODIMMs

**Memory Part:** Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II. MT8JTF12864HZ-1G6  
Create Custom Part

**Memory Voltage:** Select the Voltage of the Memory part selected. 1.5V

**Data Width:** Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above. 64

**ECC:** MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported. Disabled

**Data Mask:** Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.

**ORDERING:** Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received. Normal

**Memory Details:** 1GB, x8, row:14, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, single rank, 1.5V

< Back Next > Cancel

## ➤ Select

- Clock Period: **2500 ps**
- Type: **SODIMMs**
- Part: **MT8JTF12864HZ-1G6**
- Data Mask: **Checked**
- Click Next

# Generate MIG Example Design

**Memory Options for Controller 0 - DDR3 SDRAM**

**Input Clock Period:** Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

5000 ps (200 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

**Read Burst Type and Length**  
The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

**Output Driver Impedance Control**  
Programmable impedance for the output buffer.

RZQ/7

**Controller Chip Select Pin**  
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Enable

**RTT (nominal) - On Die Termination (ODT)**  
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 (40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configurations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

RZQ/6

Memory Address Mapping Selection

User Address

A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	A
ROW																BANK				COLUMN													

< Back   Next >   Cancel

## ➤ Select:

- Input Clock Period: **5000 ps**
- RTT: **RZQ/6**
- Click Next



# Generate MIG Example Design

The screenshot shows a configuration window for the MIG (Memory Interface Generator) design. It contains several sections with dropdown menus and checkboxes:

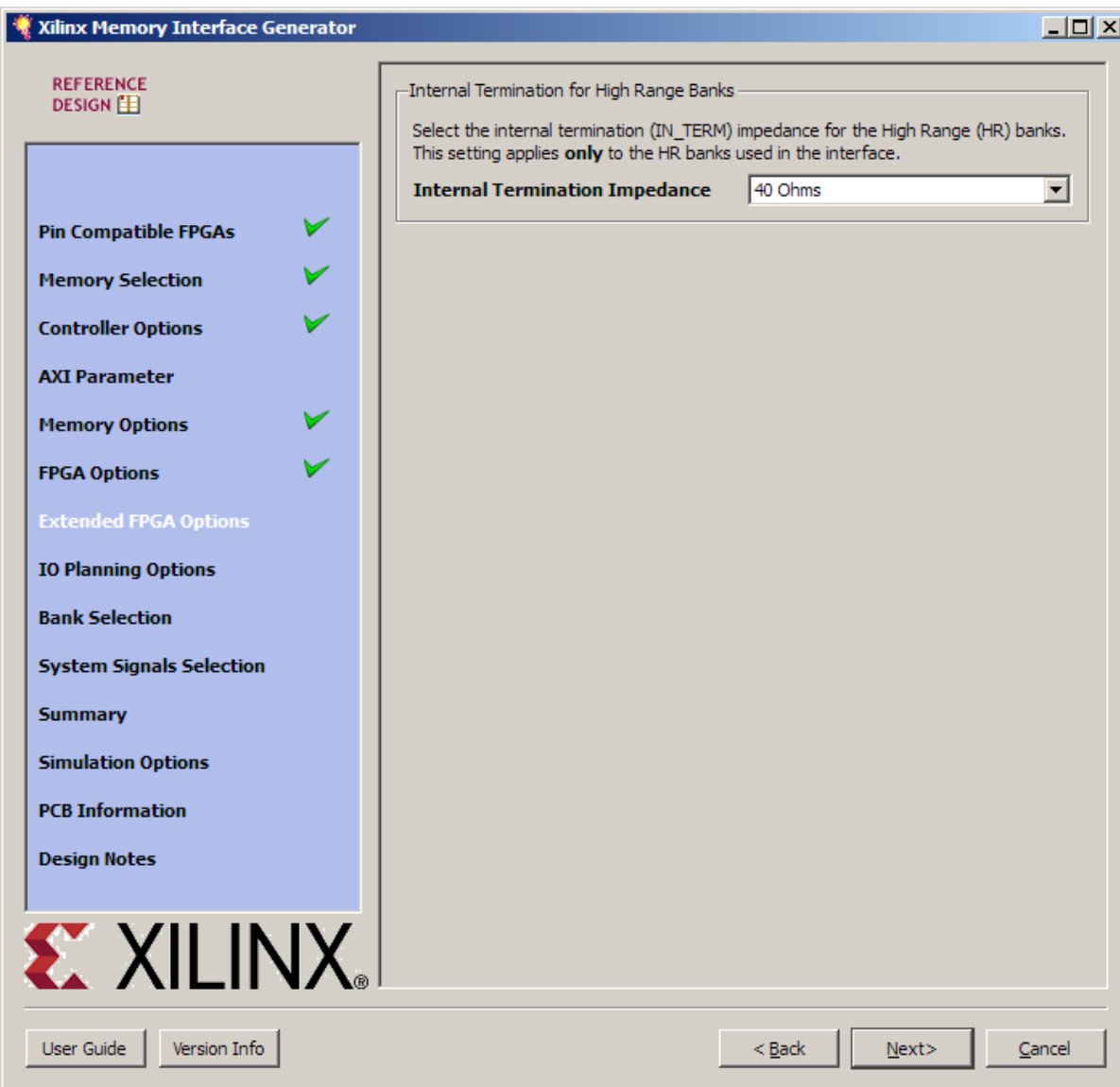
- System Clock:** Choose the desired input clock configuration. Design clock can be Differential or Single-Ended. **System Clock** is set to **Differential**.
- Reference Clock:** Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended. **Reference Clock** is set to **Use System Clock**.
- System Reset Polarity:** Choose the desired System Reset Polarity. **System Reset Polarity** is set to **ACTIVE HIGH**.
- Debug Signals Control:** This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals. **Debug Signals for Memory Controller** is set to **ON**. **Sample Data Depth** is set to **1024**.
- Internal Vref:** Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs. **Internal Vref** is **unchecked**.
- IO Power Reduction:** Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITES and periods of inactivity.

At the bottom of the window are three buttons: **< Back**, **Next >**, and **Cancel**.

## ➤ Select

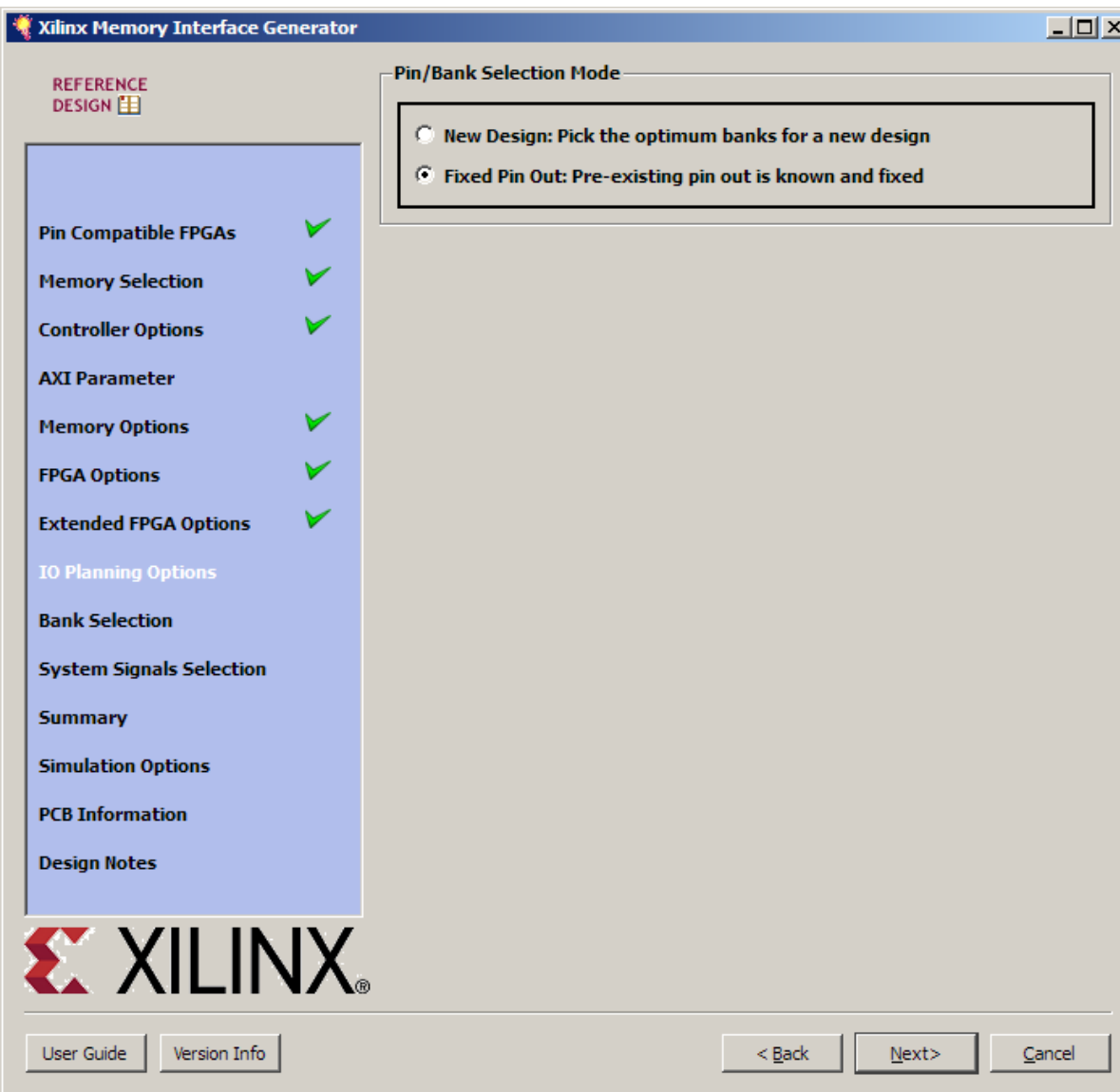
- Reference Clock: **Use System Clock**
- System Reset: **Active HIGH**
- Debug: **ON**
- Click Next

# Generate MIG Example Design



- Set Internal Termination Impedance to 40 Ohms
  - Click Next

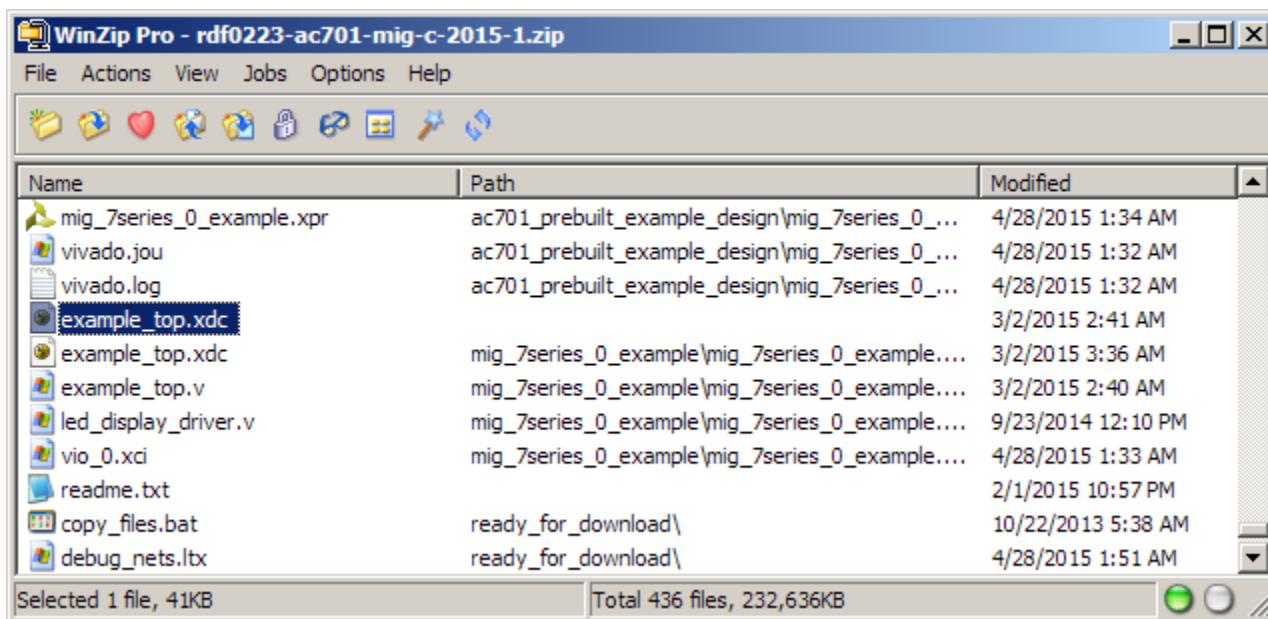
# Generate MIG Example Design



- **Select Fixed Pin Out**
  - Click Next

# Modifications to Example Design

- Open the AC701 MIG Design Files (2015.1 C) ZIP file
  - Available through <http://www.xilinx.com/ac701>
  - Extract the file, “**example\_top.xdc**” *only* to C:\ac701\_mig
  - Contains the XDC constraints needed for AC701 MIG design
  - This zip file will be needed later in the presentation



# Generate MIG Example Design

## ➤ Select Read XDC/UCF

- Open the file:  
example\_top.xdc

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	All Banks	Select Byte	Select Pin	
2	ddr3_dq[1]	All Banks	Select Byte	Select Pin	
3	ddr3_dq[2]	All Banks	Select Byte	Select Pin	
4	ddr3_dq[3]	All Banks	Select Byte	Select Pin	
5	ddr3_dq[4]	All Banks	Select Byte	Select Pin	
6	ddr3_dq[5]	All Banks	Select Byte	Select Pin	
7	ddr3_dq[6]	All Banks	Select Byte	Select Pin	
8	ddr3_dq[7]	All Banks	Select Byte	Select Pin	
9	ddr3_dq[8]	All Banks	Select Byte	Select Pin	
10	ddr3_dq[9]	All Banks	Select Byte	Select Pin	
11	ddr3_dq[10]	All Banks	Select Byte	Select Pin	
12	ddr3_dq[11]	All Banks	Select Byte	Select Pin	
13	ddr3_dq[12]	All Banks	Select Byte	Select Pin	
14	ddr3_dq[13]	All Banks	Select Byte	Select Pin	
15	ddr3_dq[14]	All Banks	Select Byte	Select Pin	
16	ddr3_dq[15]	All Banks	Select Byte	Select Pin	

INFO : Press Validate to proceed.

Validate **Read XDC/UCF** Save Pin

< Back Next > Cancel

Load your UCF

Look in: ac701\_mig\_design

- ac701\_mig\_design.data
- ac701\_mig\_design.runs
- ac701\_mig\_design.srscs
- example\_top.xdc**

My Recent Documents

Desktop

My Documents

My Computer

My Network Places

File name: example\_top.xdc

Files of type: Constraint Files (\*.xdc \*.ucf)

Note: Presentation applies to the AC701

# Generate MIG Example Design

Pin Selection For Controller 0 - DDR3 SDRAM

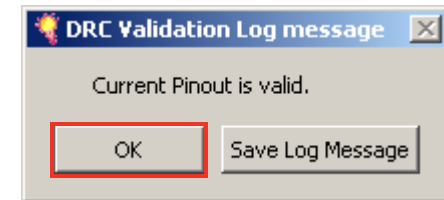
	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	33	T3	AB6	SSTL15
2	ddr3_dq[1]	33	T3	AA8	SSTL15
3	ddr3_dq[2]	33	T3	Y8	SSTL15
4	ddr3_dq[3]	33	T3	AB5	SSTL15
5	ddr3_dq[4]	33	T3	AA5	SSTL15
6	ddr3_dq[5]	33	T3	Y5	SSTL15
7	ddr3_dq[6]	33	T3	Y6	SSTL15
8	ddr3_dq[7]	33	T3	Y7	SSTL15
9	ddr3_dq[8]	33	T2	AF4	SSTL15
10	ddr3_dq[9]	33	T2	AF5	SSTL15
11	ddr3_dq[10]	33	T2	AF3	SSTL15
12	ddr3_dq[11]	33	T2	AE3	SSTL15
13	ddr3_dq[12]	33	T2	AD3	SSTL15
14	ddr3_dq[13]	33	T2	AC3	SSTL15
15	ddr3_dq[14]	33	T2	AB4	SSTL15
16	ddr3_dq[15]	33	T2	AA4	SSTL15

INFO : Press Validate to proceed.

Validate Read XDC/UCF Save PinOut

< Back Next > Cancel

- Once it finishes reading in the XDC, click **Validate**
  - Click OK



# Generate MIG Example Design

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	33	T3	AB6	SSTL15
2	ddr3_dq[1]	33	T3	AA8	SSTL15
3	ddr3_dq[2]	33	T3	Y8	SSTL15
4	ddr3_dq[3]	33	T3	AB5	SSTL15
5	ddr3_dq[4]	33	T3	AA5	SSTL15
6	ddr3_dq[5]	33	T3	Y5	SSTL15
7	ddr3_dq[6]	33	T3	Y6	SSTL15
8	ddr3_dq[7]	33	T3	Y7	SSTL15
9	ddr3_dq[8]	33	T2	AF4	SSTL15
10	ddr3_dq[9]	33	T2	AF5	SSTL15
11	ddr3_dq[10]	33	T2	AF3	SSTL15
12	ddr3_dq[11]	33	T2	AE3	SSTL15
13	ddr3_dq[12]	33	T2	AD3	SSTL15
14	ddr3_dq[13]	33	T2	AC3	SSTL15
15	ddr3_dq[14]	33	T2	AB4	SSTL15
16	ddr3_dq[15]	33	T2	AA4	SSTL15

INFO : Validation successful. Press Next to proceed.

Validate Read XDC/UCF Save PinOut

< Back **Next>** Cancel

- The Next button is enabled once the pinout is validated.
  - Click Next



# Generate MIG Example Design

- Set `sys_clk_p/n` to `R3/P3(CC_P/N)`
  - Click Next

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see [UG586 Bank and Pin rules](#).

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Clock Pin Selection

The `sys_clk` is used as the system clock for the memory interface. This signal should be connected to a low jitter external clock source via a differential (P/N) pair for best performance. This signal should be in the address/control bank, but may be placed in an adjacent bank if there are not enough pins available such as when fitting a 16 bit interface in a single bank.

Signal Name	Bank Number	Pin Number	
1	sys_clk_p/n	34	R3/P3(CC_P/N)

Reference Clock Pin Selection

The `clk_ref` input is used as the reference clock for the IODELAY. Refer the "7 Series FPGA SelectIO Resources User Guide" for more information. This input can be generated internally or can be connected to an external clock source on a clock capable differential (P/N) pair. This selection will be faded when Reference Clock type chosen is **Use System Clock**.

Signal Name	Bank Number	Pin Number	
1	clk_ref_p/n	Select Bank	Select Pin

Status Signals

These signals may be connected internally to other logic or brought out to a pin.

**All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).**

< Back   Next >   Cancel

# Generate MIG Example Design

- Leave this page as is
  - Click Next

**Xilinx Memory Interface Generator**

REFERENCE DESIGN

**Pin Compatible FPGAs** ✓  
**Memory Selection** ✓  
**Controller Options** ✓  
**AXI Parameter**  
**Memory Options** ✓  
**FPGA Options** ✓  
**Extended FPGA Options** ✓  
**IO Planning Options** ✓  
**Pin Selection** ✓  
**System Signals Selection** ✓  
**Summary**  
**Simulation Options**  
**PCB Information**  
**Design Notes**

Vivado Project Options:  
Target Device : xc7a200t-fbg676  
Speed Grade : -2  
HDL : verilog  
Synthesis Tool : VIVADO

If any of the above options are incorrect, please click on "Cancel", change the CORE Generator Project Options, and restart MIG.

MIG Output Options:  
Module Name : mig\_7series\_0  
No of Controllers : 1  
Selected Compatible Device(s) : --

FPGA Options:  
System Clock Type : Differential  
Reference Clock Type : Use System Clock  
Debug Port : ON  
Internal Vref : disabled  
IO Power Reduction : ON  
XADC instantiation in MIG : Enabled

Extended FPGA Options:  
DCI for DQ, DQS/DQS#, DM : enabled  
Internal Termination (HR Banks) : 40 Ohms

Controller 0

Print

User Guide Version Info < Back Next > Cancel

Note: Presentation applies to the AC701

# Generate MIG Example Design

The screenshot shows the Xilinx Memory Interface Generator (MIG) software interface. On the left, a navigation pane lists various configuration options, all of which are marked with a green checkmark, indicating they have been completed. The main window displays the "Micron Technology, Inc. Simulation Model License Agreement". The text of the agreement is as follows:

Micron Technology, Inc. Simulation Model License Agreement

PLEASE READ THIS SIMULATION MODEL LICENSE AGREEMENT ("AGREEMENT") FROM MICRON TECHNOLOGY, INC. ("MTI") CAREFULLY BEFORE INSTALLING OR USING THIS SIMULATION MODEL (THE "MODEL"). BY INSTALLING OR USING THE MODEL, YOU ARE ACCEPTING AND AGREEING TO THE TERMS AND CONDITIONS OF THIS AGREEMENT. IF YOU DO NOT AGREE WITH THE TERMS AND CONDITIONS OF THIS AGREEMENT, THEN DO NOT INSTALL OR USE THE MODEL.

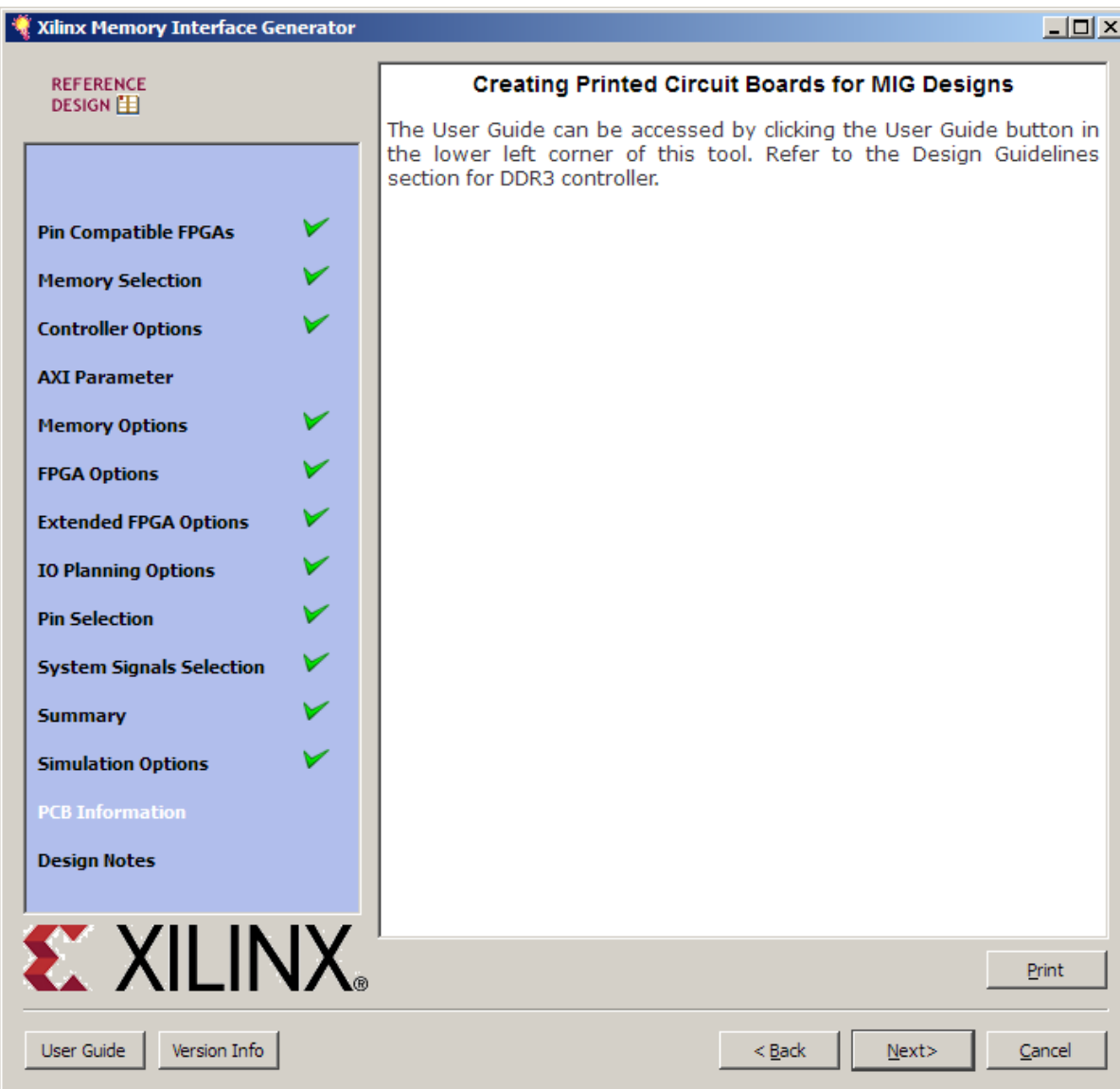
SOFTWARE LICENSE: You acknowledge and agree that it is your sole responsibility to obtain the appropriate license or permission from the owner(s) of the software platform(s) that are necessary for you to operate the Model. MTI is under no obligation whatsoever to offer, provide or secure such license or permission for you.

MODEL LICENSE: MTI hereby grants to you the right to install, use and modify the Model solely for testing the Model and designing your product(s) in connection with the Model. You shall not use the Model or any modifications for any other purpose, and shall not copy, rent, or lease the Model or the modifications to any third party. MTI may make changes to the Model at any time without notice to you. MTI is under no obligation whatsoever to update, maintain, or provide new

At the bottom of the window, there are two radio buttons for "Accept" and "Decline". Below the radio buttons, there is a small text box that reads: "Check Accept or Decline to proceed. By clicking Accept, memory model will be output in the simulation directory. By clicking Decline, a memory model must be acquired and configured appropriately." There are also buttons for "Print", "< Back", "Next >", and "Cancel".

- **Accept Simulation license, if desired**
  - Otherwise, Decline license
  - Click Next

# Generate MIG Example Design



- Leave this page as is
  - Click Next

# Generate MIG Example Design

➤ Click Generate

**REFERENCE DESIGN**

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- AXI Parameter
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options ✓
- IO Planning Options ✓
- Pin Selection ✓
- System Signals Selection ✓
- Summary ✓
- Simulation Options ✓
- PCB Information ✓
- Design Notes

## DDR3 SDRAM Design for Artix-7 FPGAs

### Design Notes

1. This design is tested with Vivado 2015.1 version
2. This design is simulated with Questa SIM 10.3d version, VCS I-2014.03-SP1 version, and IES 14.10.011 version
3. Components, RDIMMs, UDIMMs and SODIMMs are supported
4. If fly by delays are simulated, they must be limited to 1.2ns
5. Consult the Version Info for known limitations

### Key Enhancements for MIG 2.3 - 2014.4 release

1. Updated Maximum supported design frequencies as per the 7 Series DC and AC Switching Characteristics data sheets
2. DDR3 OCLK delay calibration enhancements

### Key Enhancements for MIG 2.2 - 2014.3 release

1. Updated Maximum supported design frequencies as per the 7 Series DC and AC Switching Characteristics data sheets

Print

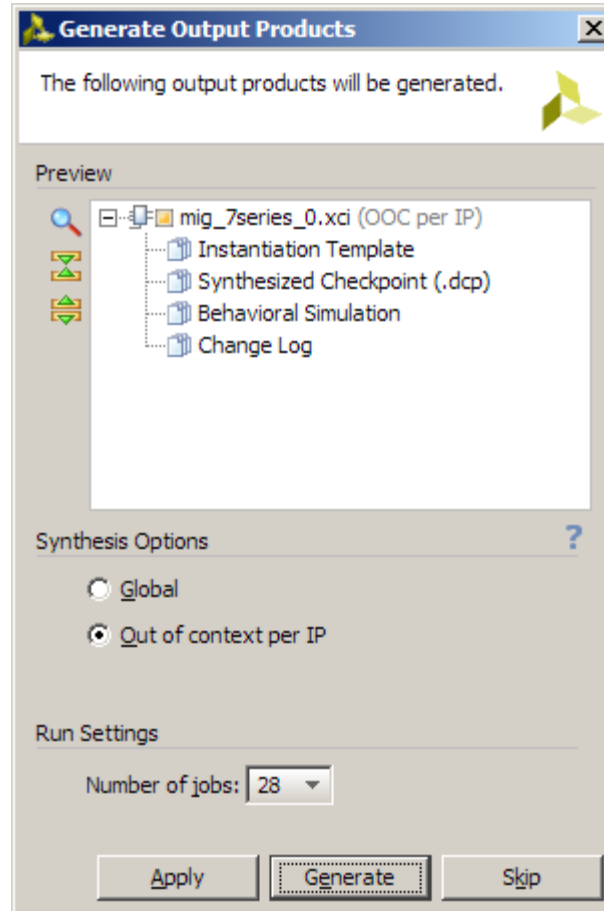
User Guide Version Info < Back Generate Cancel

Note: Presentation applies to the AC701

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# Generate MIG Example Design

➤ Click Generate



# Generate MIG Example Design

## ➤ MIG design appears in Design Sources

– Wait until checkmark appears on mig\_7series\_0\_synth\_1

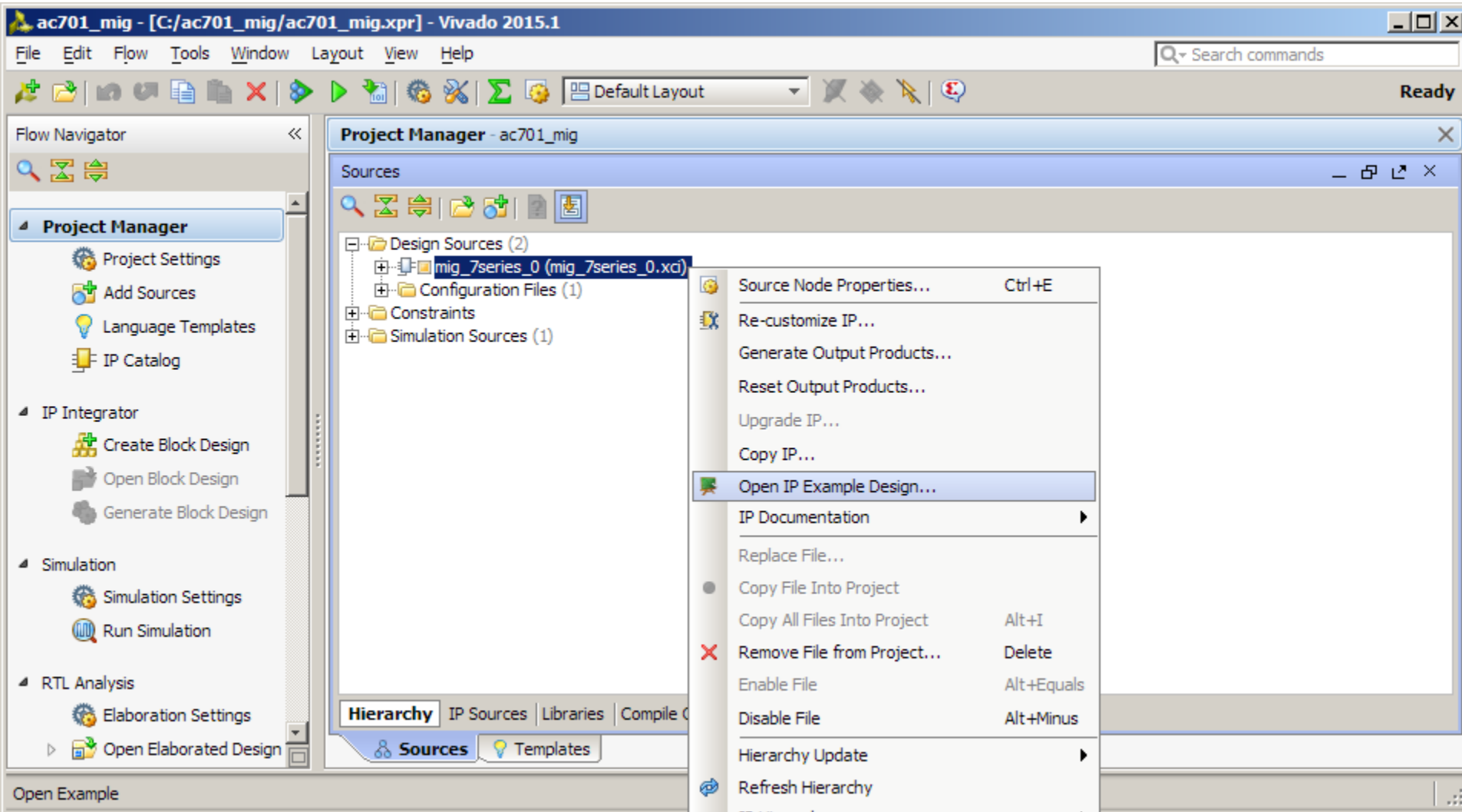
The screenshot displays the Vivado 2015.1 IDE interface for a project named 'ac701\_mig'. The 'Project Manager' window shows the 'Design Sources' tree with 'mig\_7series\_0 (mig\_7series\_0.xci)' listed. Below it, the 'Synthesis Run Properties' window shows a green checkmark next to 'mig\_7series\_0\_synth\_1', indicating a successful synthesis run. The 'Design Runs' window at the bottom shows a table of synthesis runs, with 'mig\_7series\_0\_synth\_1' highlighted in blue. The 'Project Summary' window on the right shows the project's configuration, including the part 'xc7a200' and the strategy 'Vivado Implementation'. The status bar at the bottom indicates 'Synthesis Run: mig\_7series\_0\_synth\_1'.

Name	Constraints	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FF
impl_1 (active)	constrs_1										
Out-of-Context Module Runs											
✓ mig_7series_0_synth_1	mig_7series...							9.455	12727	3.232	81

Note: Presentation applies to the AC701

# Compile Example Design

➤ Right click on mig\_7series\_0 and select Open IP Example Design...

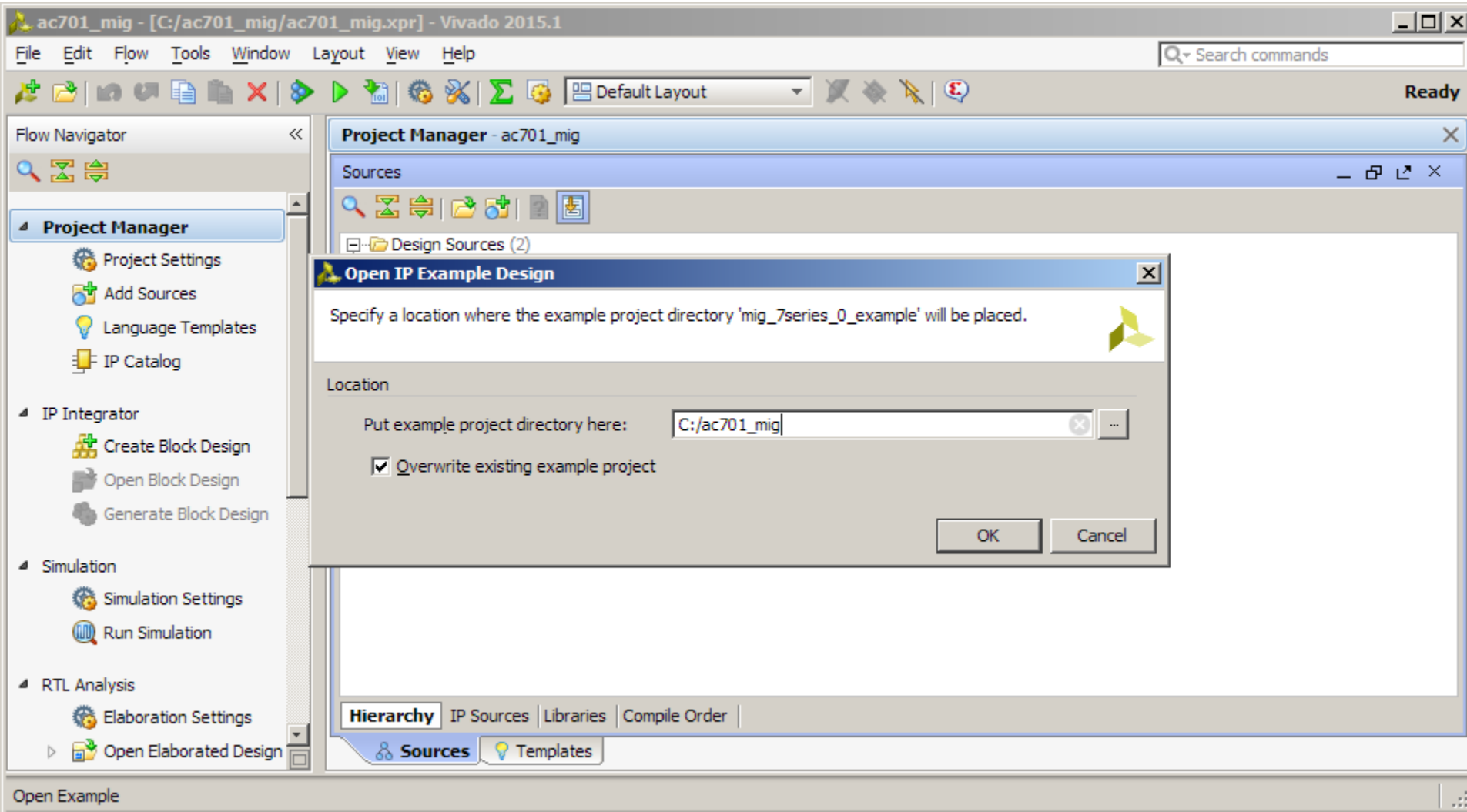


Note: Presentation applies to the AC701



# Compile Example Design

➤ Set the location to C:/ac701\_mig and click OK

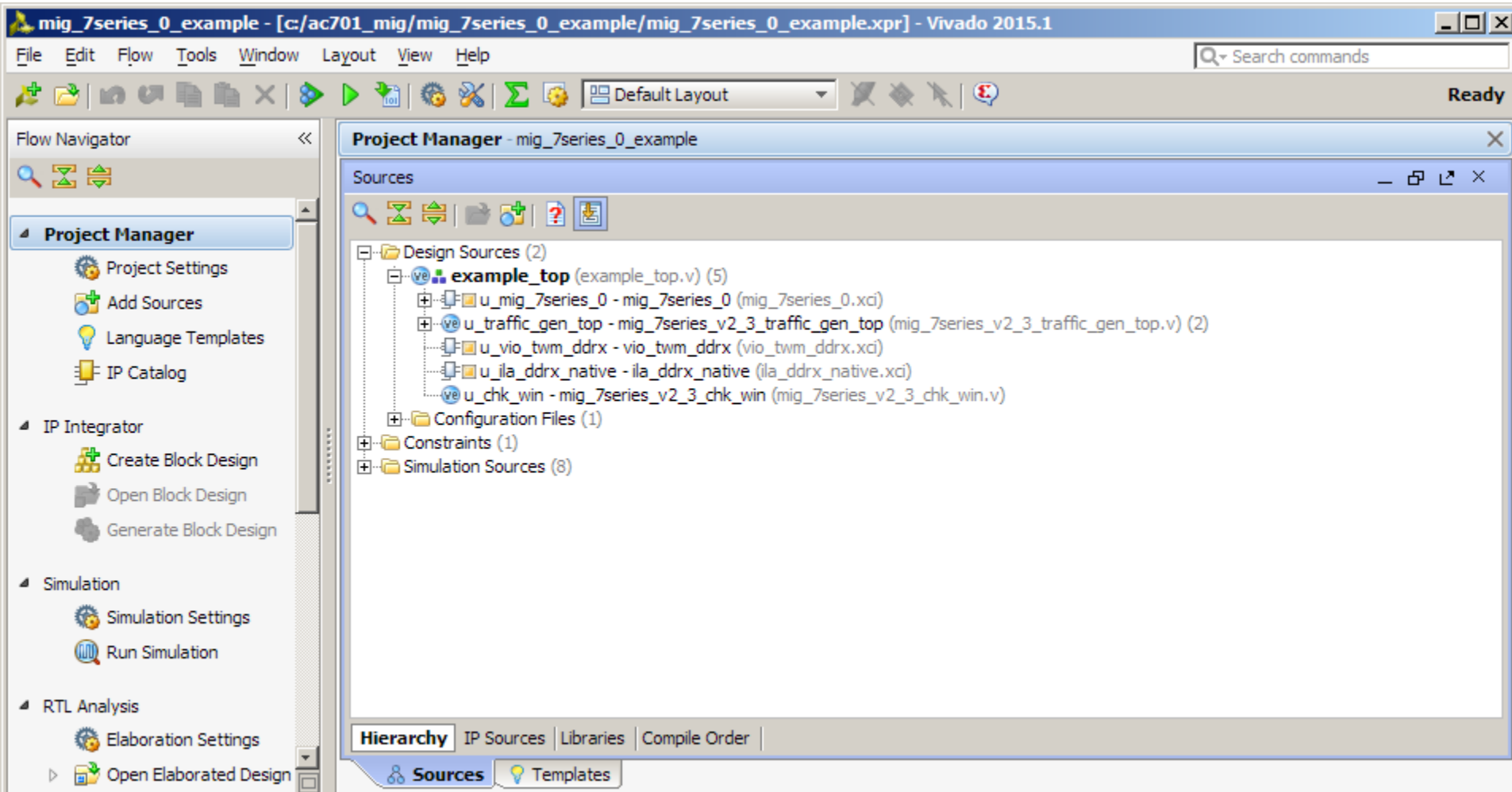


Note: Presentation applies to the AC701

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# Compile Example Design

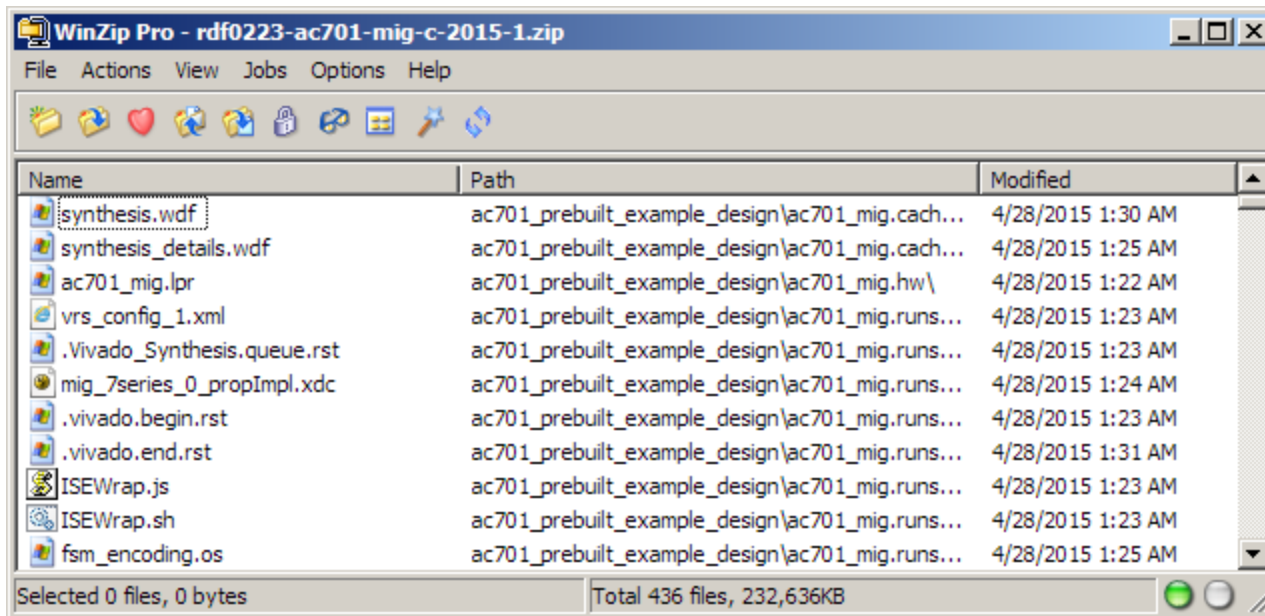
➤ A new project is created



**Note:** The original project window can be closed

# Modifications to Example Design

- Unzip the AC701 MIG Design Files (2015.1 C) ZIP file to your C:\ac701\_mig directory
  - Contains several changes needed to support Artix-7 devices with MIG
  - Do this **after** creating the Example Design; changes only affect the Example Design

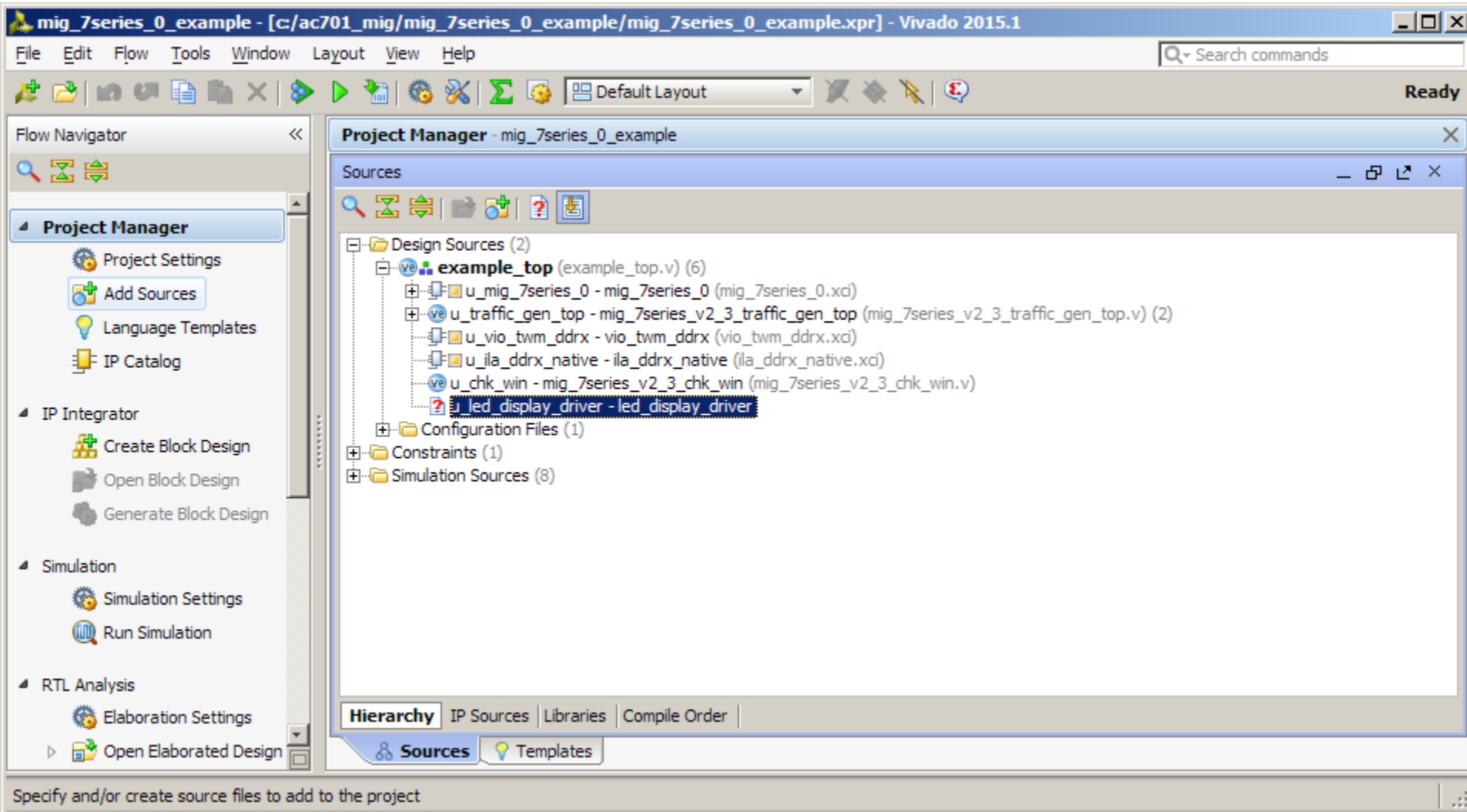


# Modifications to Example Design

- **Modifications to the example design**
  - Added RTL and XDC modifications to drive LEDs

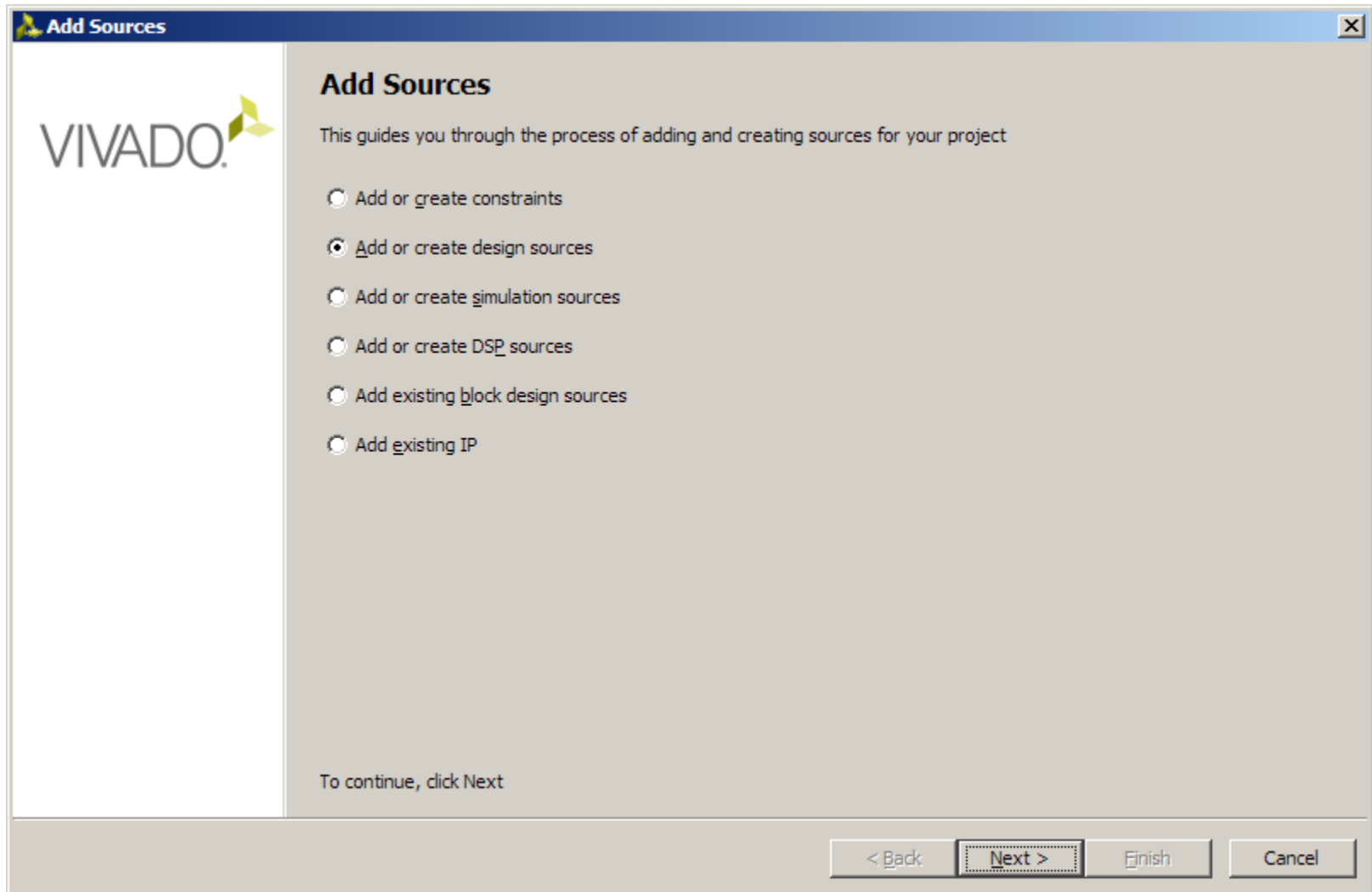
# Modifications to Example Design

- The LED Display driver RTL file needs to be added manually
- Click on Add Sources



# Modifications to Example Design

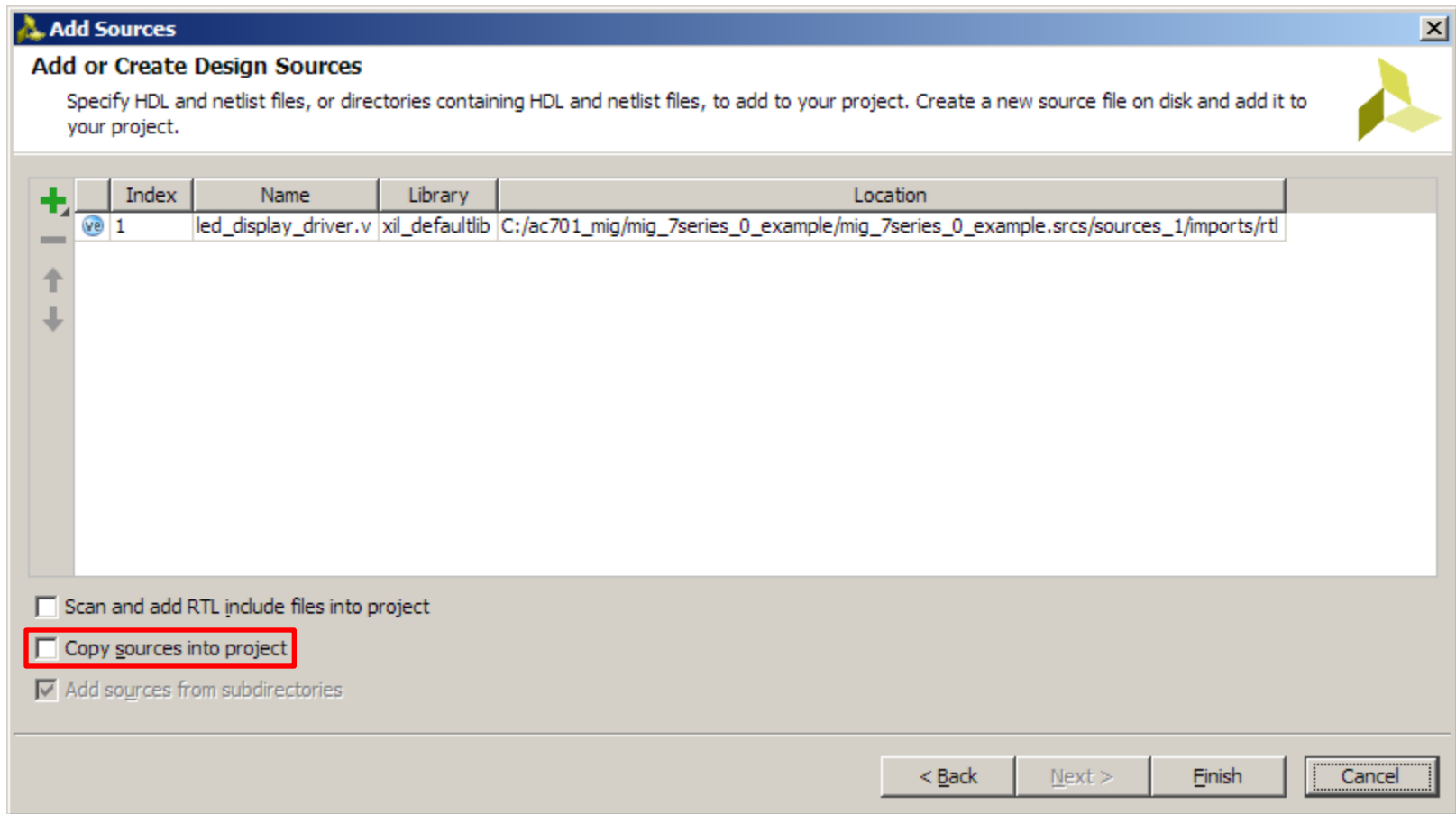
➤ Select Add or Create Design Sources and click Next



Note: Presentation applies to the AC701

# Modifications to Example Design

- Add led\_display\_driver.v from the example project
- Make sure Copy sources into project is deselected
- Click Finish



# Compile Example Design

➤ Click on Add Sources

The screenshot shows the Vivado 2015.1 Project Manager window for a project named "mig\_7series\_0\_example". The "Sources" tab is active, displaying a tree view of the project's source files. The tree is organized into four main categories: Design Sources (2), Configuration Files (1), Constraints (1), and Simulation Sources (8). The Design Sources category is expanded, showing a hierarchy starting with "example\_top (example\_top.v) (6)", which contains several sub-components: "u\_mig\_7series\_0 - mig\_7series\_0 (mig\_7series\_0.xci)", "u\_traffic\_gen\_top - mig\_7series\_v2\_3\_traffic\_gen\_top (mig\_7series\_v2\_3\_traffic\_gen\_top.v) (2)", "u\_vio\_twm\_ddrx - vio\_twm\_ddrx (vio\_twm\_ddrx.xci)", "u\_ila\_ddrx\_native - ila\_ddrx\_native (ila\_ddrx\_native.xci)", "u\_chk\_win - mig\_7series\_v2\_3\_chk\_win (mig\_7series\_v2\_3\_chk\_win.v)", "u\_led\_display\_driver - led\_display\_driver (led\_display\_driver.v) (1)", and "VIO\_inst - vio\_0". The Configuration Files category contains "vio\_0". The Constraints category contains "vio\_0". The Simulation Sources category contains "vio\_0". The Project Manager window also shows the Flow Navigator on the left, with the "Add Sources" button highlighted. The status bar at the bottom of the Project Manager window indicates "Specify and/or create source files to add to the project".

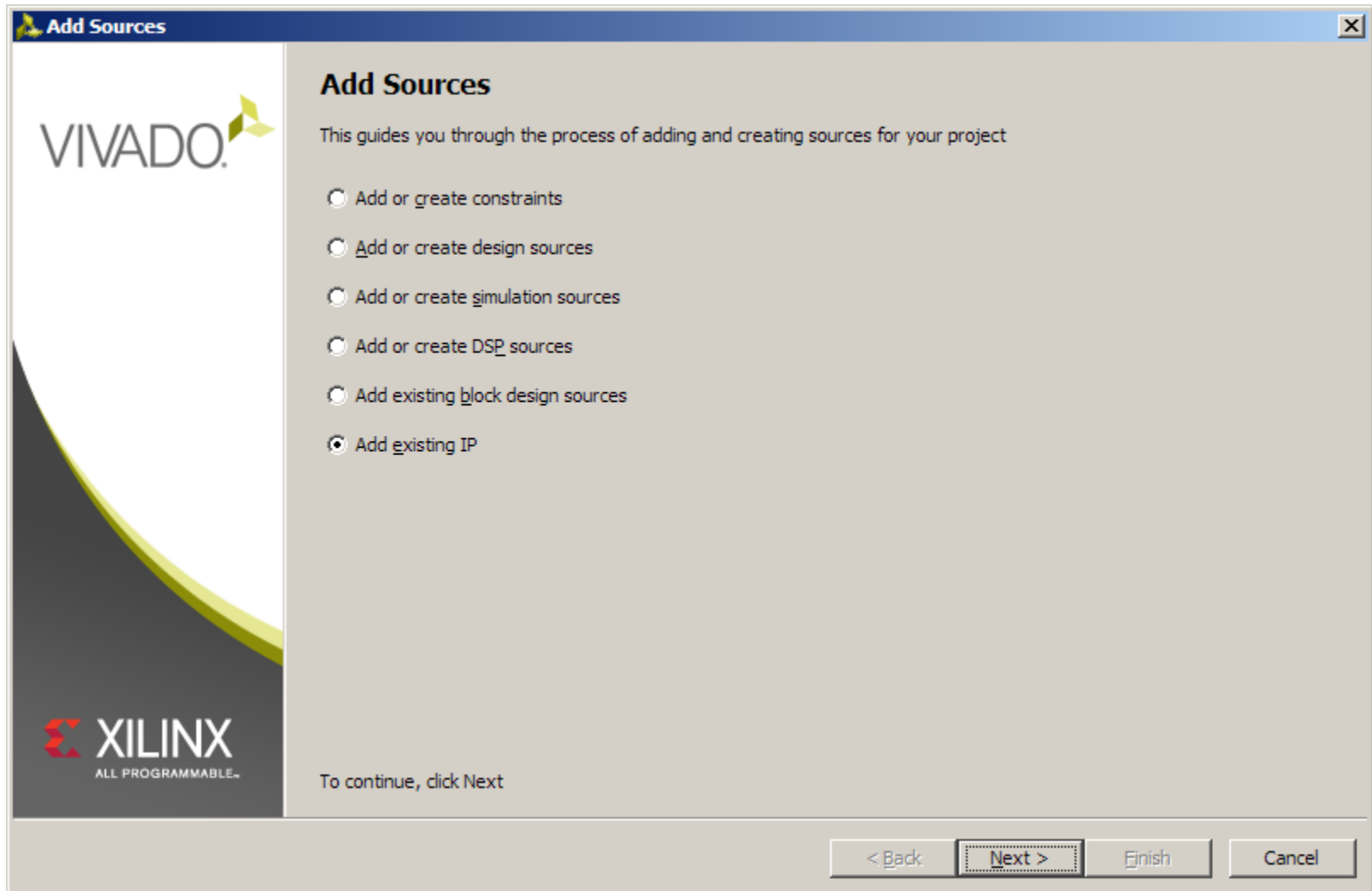
Note: Presentation applies to the AC701

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# Modifications to Example Design

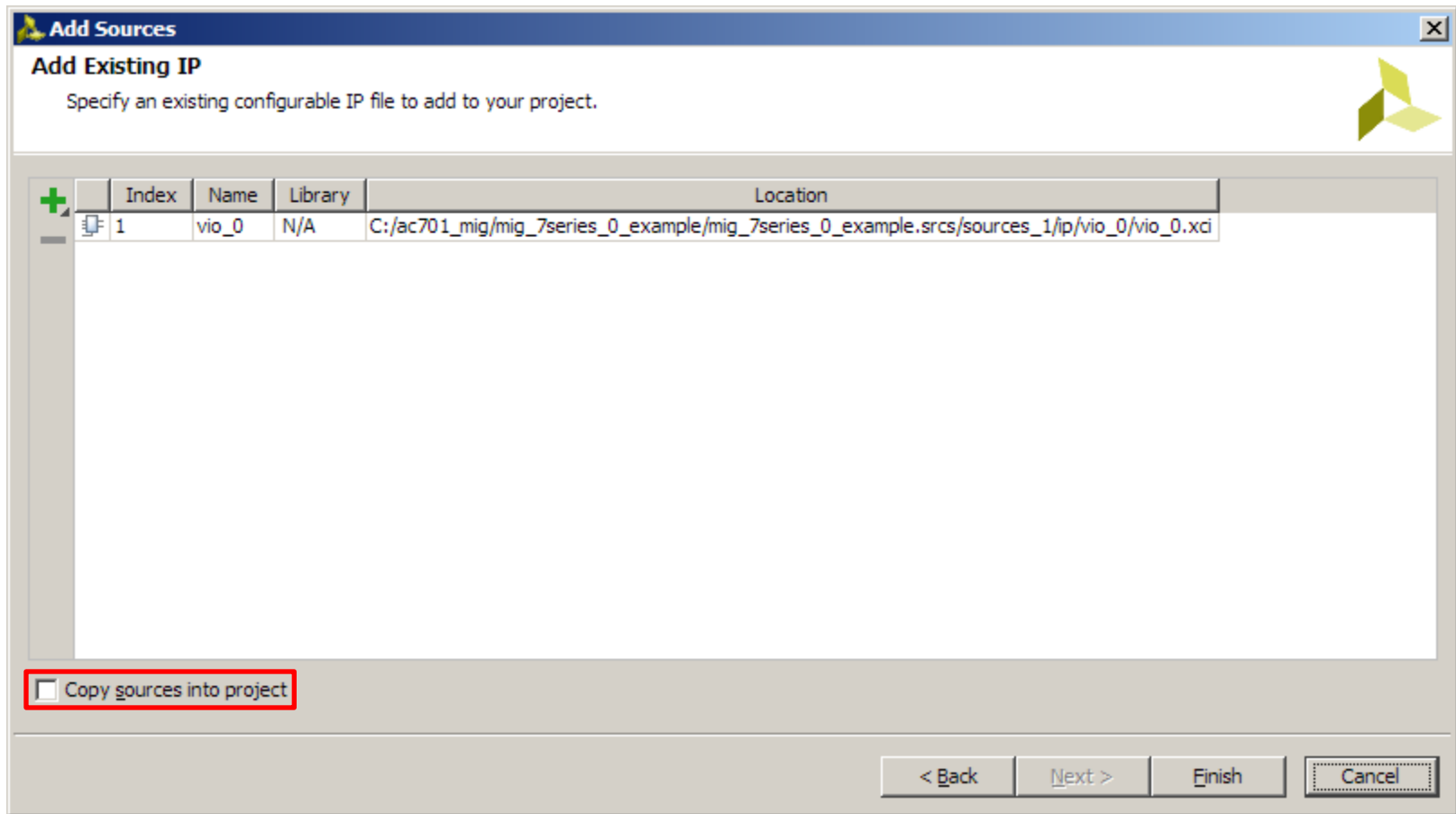
➤ Select Add Existing IP and click Next



Note: Presentation applies to the AC701

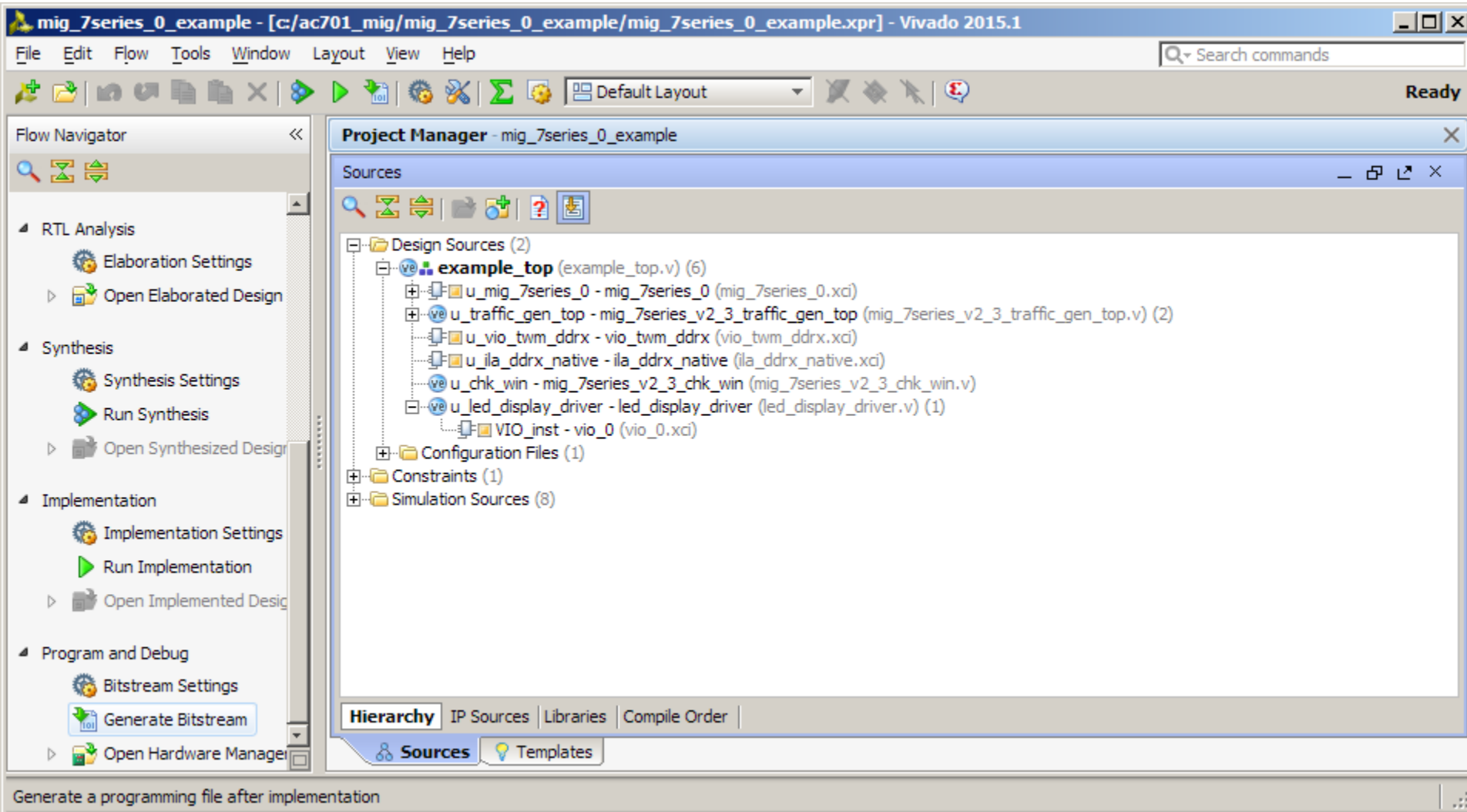
# Modifications to Example Design

- Add vio\_0.xci from the example project
- Make sure Copy sources into project is deselected
- Click Finish



# Compile Example Design

➤ Click on Generate Bitstream

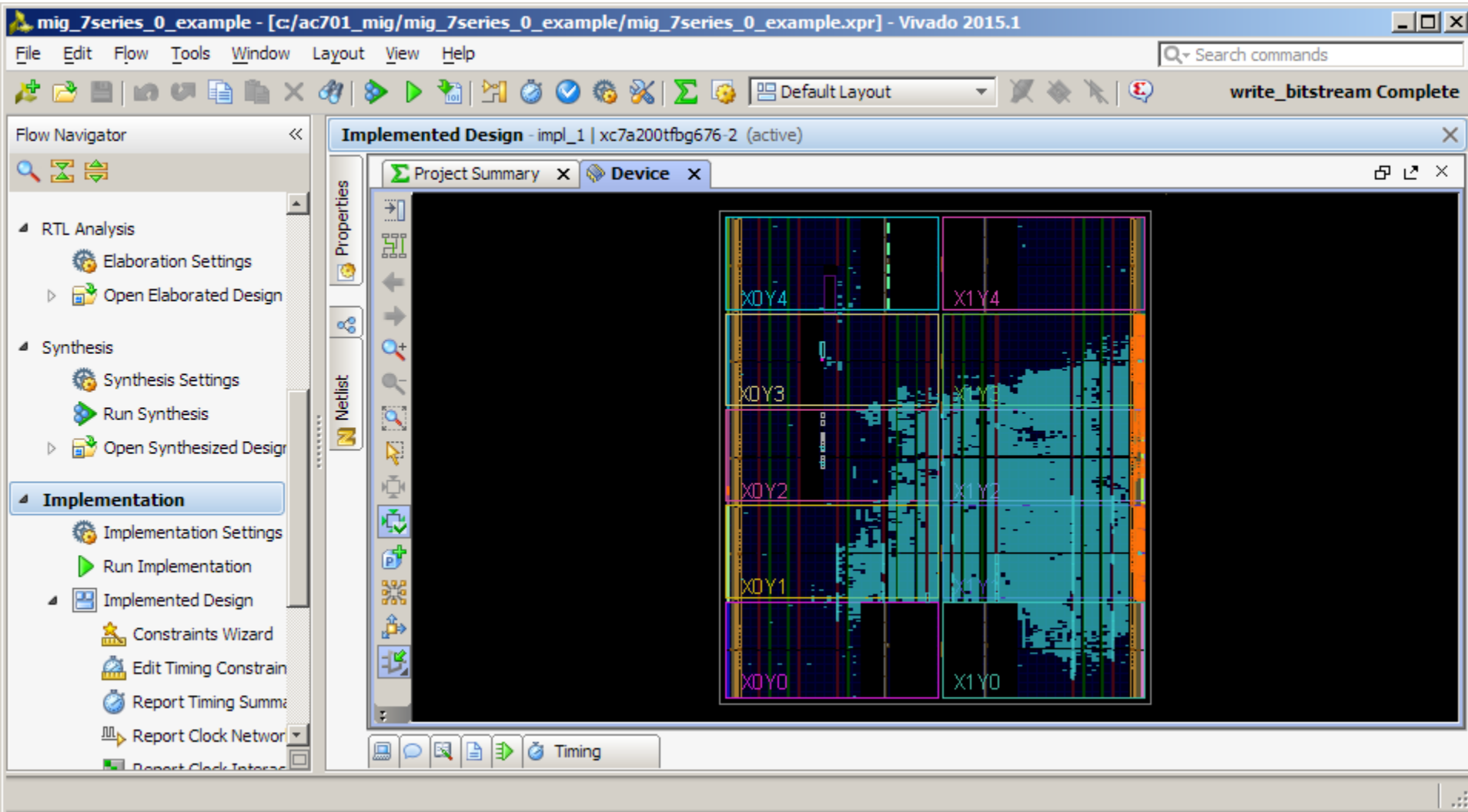


The screenshot displays the Vivado 2015.1 Project Manager interface for a project named 'mig\_7series\_0\_example'. The window title is 'mig\_7series\_0\_example - [c:/ac701\_mig/mig\_7series\_0\_example/mig\_7series\_0\_example.xpr] - Vivado 2015.1'. The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The toolbar shows various icons for file operations and project management. The 'Flow Navigator' on the left lists the design flow stages: RTL Analysis, Synthesis, Implementation, and Program and Debug. Under 'Program and Debug', the 'Generate Bitstream' button is highlighted with a blue border. The 'Project Manager' window on the right shows a tree view of 'Sources' for the project, including Design Sources (2), Configuration Files (1), Constraints (1), and Simulation Sources (8). The 'Sources' pane is currently selected, and the 'Hierarchy' tab is active at the bottom of the Project Manager window.

Note: Presentation applies to the AC701

# Compile Example Design

➤ Open and view the Implemented Design

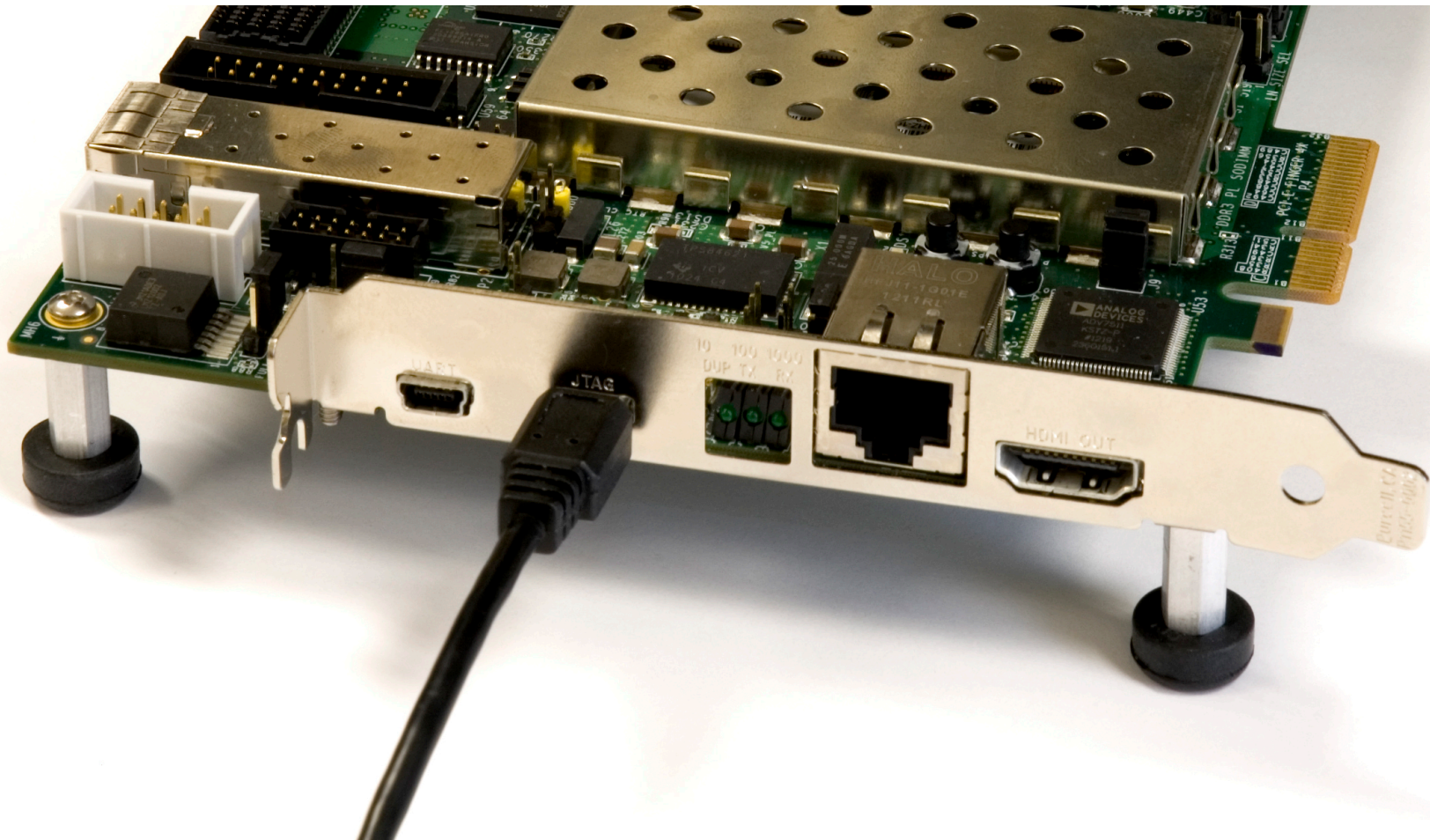


Note: Presentation applies to the AC701

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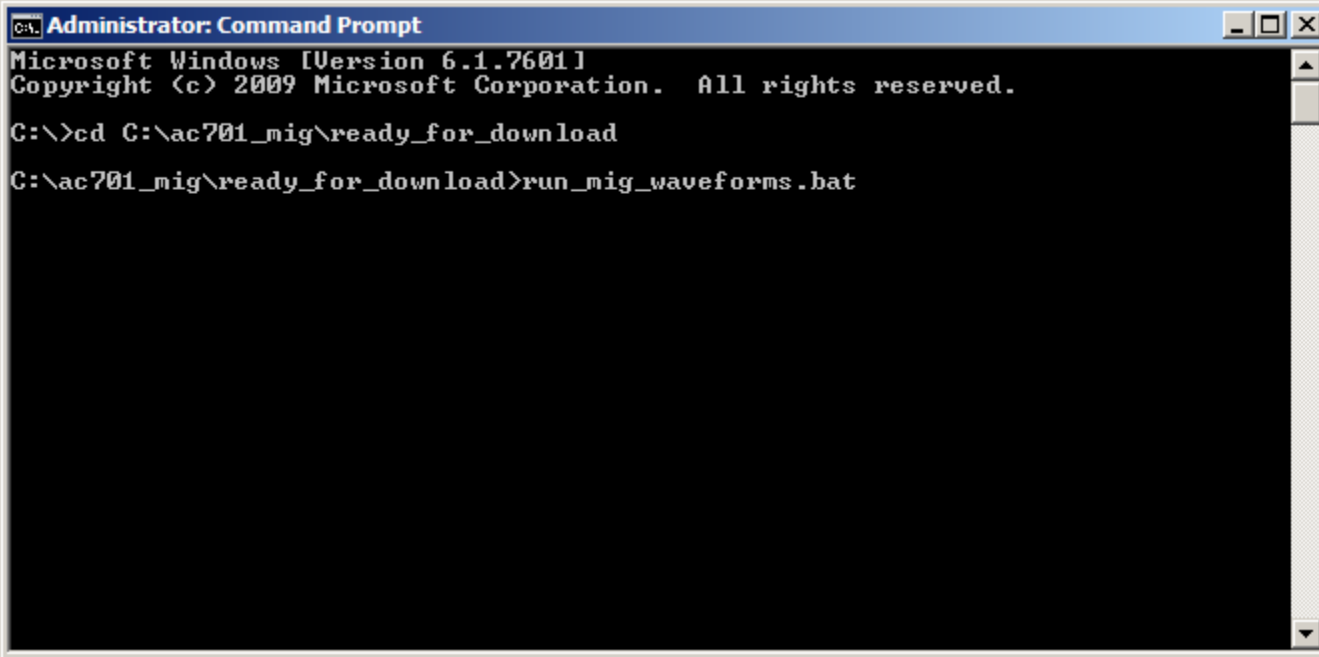
# AC701 Setup

- Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board
  - Connect this cable to your PC
  - Power on the AC701 board



# Run MIG Example Design

- From a Command Prompt, type:  
    cd C:\ac701\_mig\ready\_for\_download  
    run\_mig\_waveforms.bat



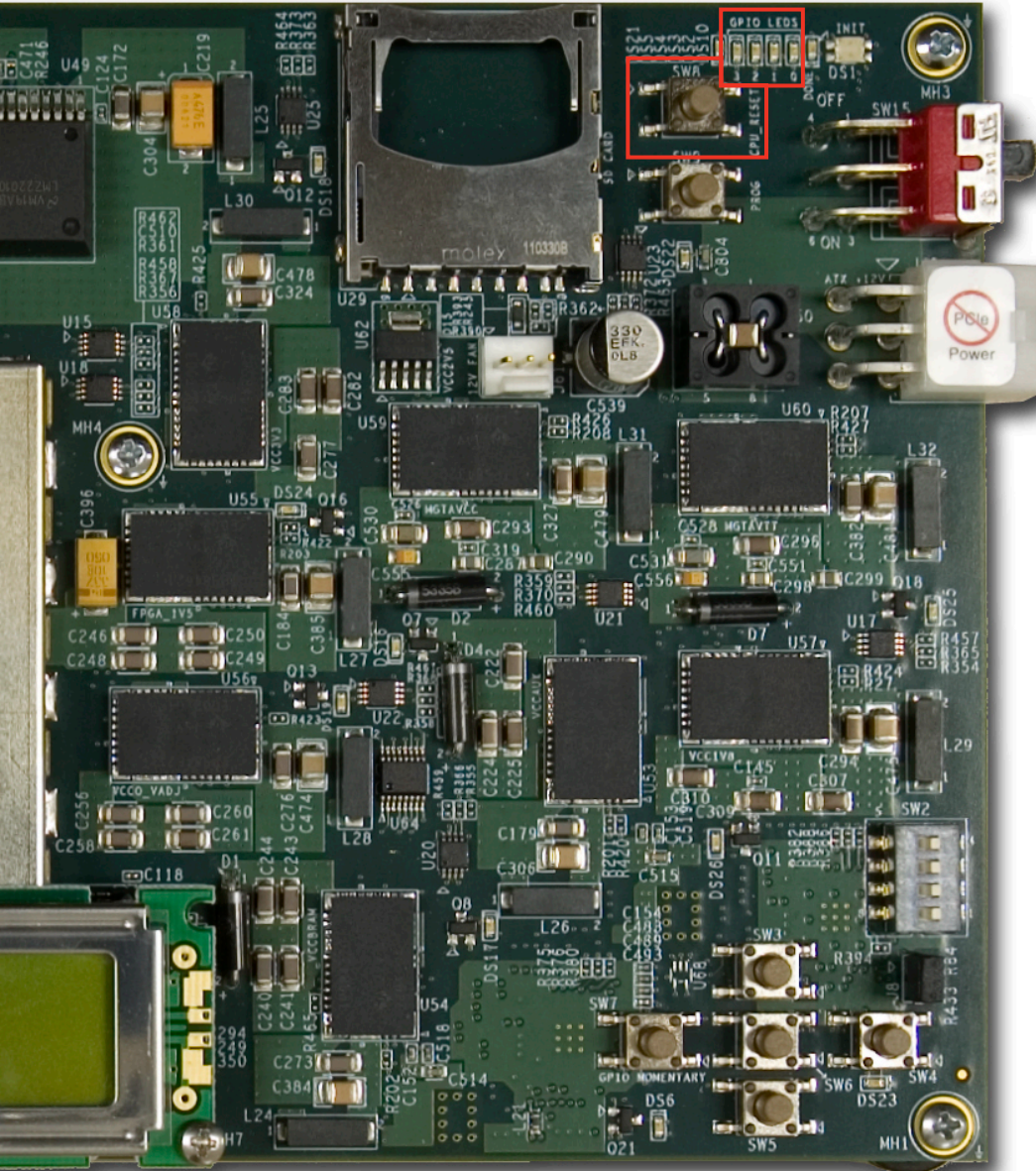
```
Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\>cd C:\ac701_mig\ready_for_download
C:\ac701_mig\ready_for_download>run_mig_waveforms.bat
```





# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - CPU\_RESET, SW8, is the reset



# Run MIG Example Design

➤ Click and drag to the left to expand the waveform



The screenshot shows the Vivado 2015.1 interface with the Hardware Manager window open. The waveform for hw\_ila\_1 is displayed, showing a signal at time 1,024. The waveform is expanded to show data at time 1,024. The table below shows the values for the signals in the waveform.

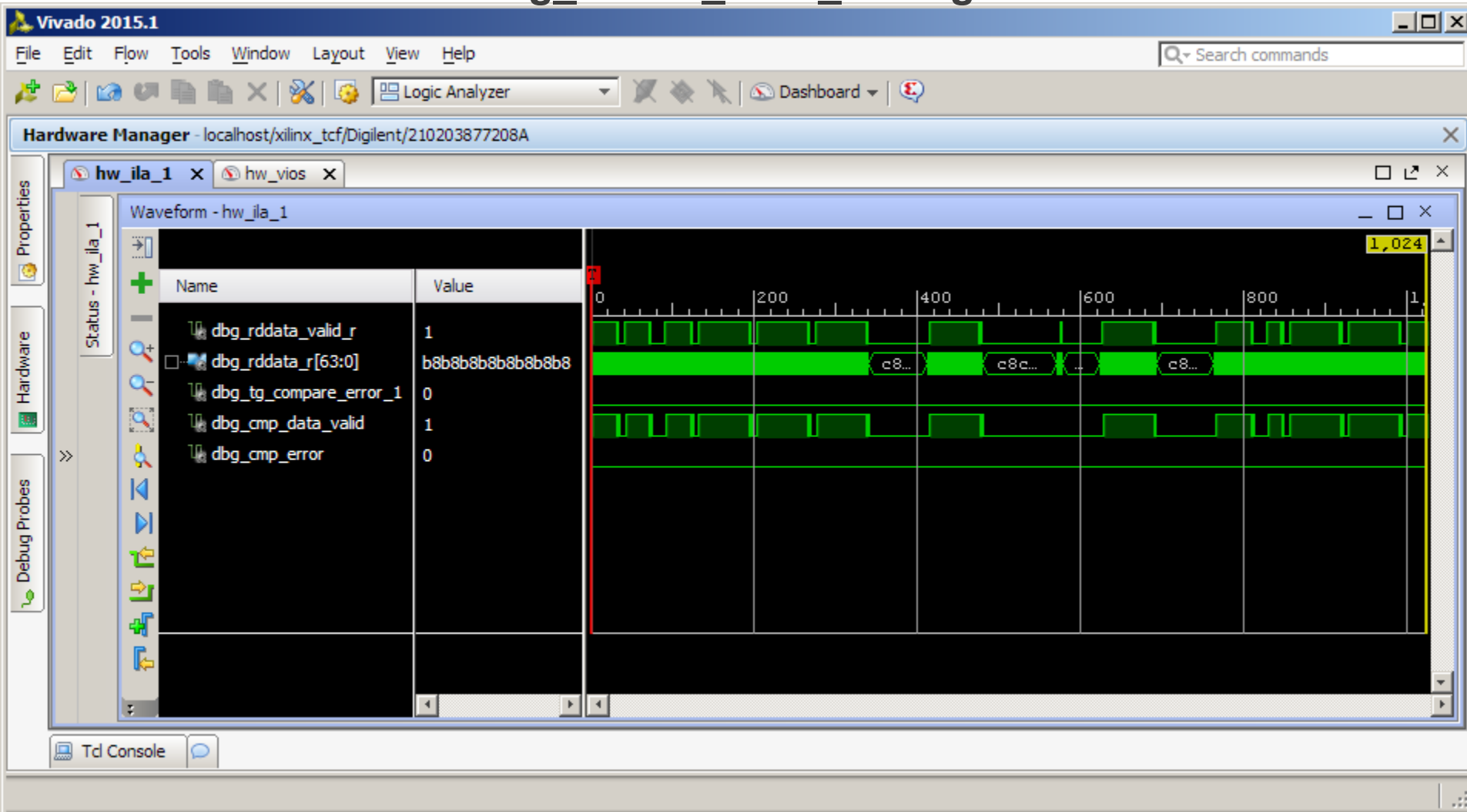
Name	Value
dbg_rddata_valid_r	1
dbg_rddata_r[63:0]	b8b8b8b8b8b8b8b8
dbg_tg_compare_error_1	0
dbg_cmp_data_valid	1
dbg_cmp_error	0

Note: Presentation applies to the AC701

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# Run MIG Example Design

- View waveforms
- Data is valid when dbg\_rddata\_valid\_r is high



# Run MIG Example Design

➤ Click and drag to the right to zoom in

The screenshot shows the Vivado 2015.1 Logic Analyzer interface. The main window displays a waveform for 'hw\_ila\_1'. The waveform is zoomed in, showing a range from 402 to 421. The signals are:

Name	Value
dbg_rddata_valid_r	1
dbg_rddata_r[63:0]	b8b8b8b8b8b8b8b8
dbg_tg_compare_error_1	0
dbg_cmp_data_valid	1
dbg_cmp_error	0

The waveform shows a sequence of data bytes (b8b8b8b8b8b8b8b8) being read from memory. The zoomed-in range is indicated by a red vertical line and a tooltip showing 'Zoom X Range 402 to 421'. The time axis is marked from 0 to 1,024.

Note: Presentation applies to the AC701

# Run MIG Example Design

➤ View waveform details

The screenshot shows the Vivado 2015.1 interface with the Hardware Manager window open. The selected hardware is hw\_ila\_1. The waveform viewer displays the following signals and their values:

Name	Value
dbg_rddata_valid_r	1
dbg_rddata_r[63:0]	b8b8b8b8b8b8b8b8
dbg_tg_compare_error_1	0
dbg_cmp_data_valid	1
dbg_cmp_error	0

The waveform viewer also shows a detailed view of the dbg\_rddata\_r[63:0] signal at time steps 414, 415, and 416. The signal values are:

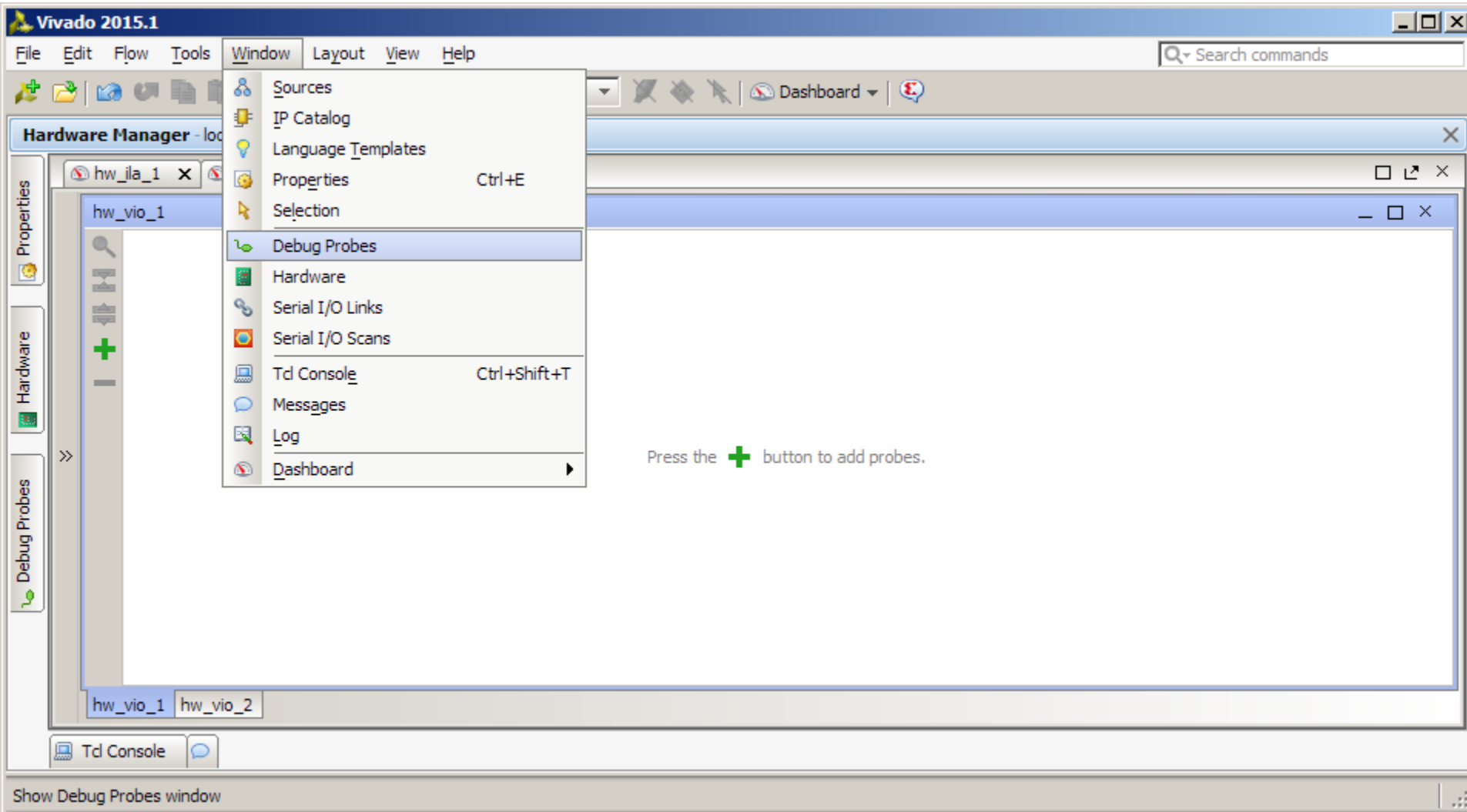
Time Step	Value
414	0000000000000000
415	0808080808080808
416	1010101010101010

Note: Presentation applies to the AC701

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# Adjust Data Pattern using VIO Console

➤ Select the hw\_vios tab and open the Debug Probes



Note: Presentation applies to the AC701

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# Adjust Data Pattern using VIO Console

- Select the `vio_data_mode_value` and `vio_modify_enable` probes
- Drag these probes to the `hw_vios` tab

The screenshot shows the Vivado 2015.1 interface. The **Hardware Manager** window is open, displaying the **Debug Probes** window on the left and the **hw\_vios** tab on the right.

In the **Debug Probes** window, the following probes are listed:

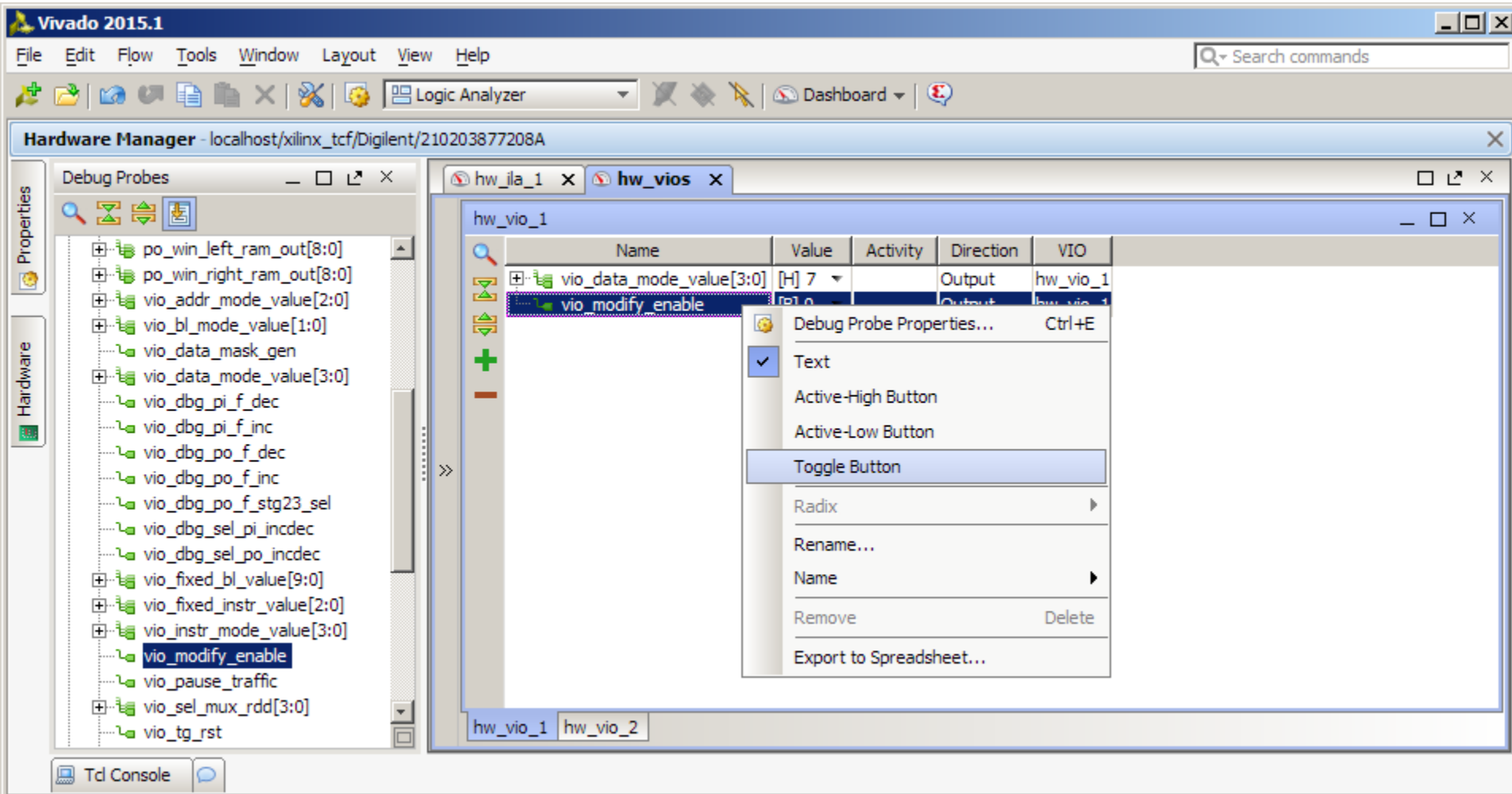
- `po_win_left_ram_out[8:0]`
- `po_win_right_ram_out[8:0]`
- `vio_addr_mode_value[2:0]`
- `vio_bl_mode_value[1:0]`
- `vio_data mask gen`
- `vio_data_mode_value[3:0]` (highlighted with a red box)
- `vio_dbg_pi_f_dec`
- `vio_dbg_pi_f_inc`
- `vio_dbg_po_f_dec`
- `vio_dbg_po_f_inc`
- `vio_dbg_po_f_stg23_sel`
- `vio_dbg_sel_pi_incdec`
- `vio_dbg_sel_po_incdec`
- `vio_fixed_bl_value[9:0]`
- `vio_fixed_instr_value[2:0]`
- `vio_instr_mode_value[3:0]`
- `vio_modify_enable` (highlighted with a red box)
- `vio_pause_traffic`
- `vio_sel_mux_rdd[3:0]`
- `vio_tg_rst`

In the **hw\_vios** tab, the **hw\_vio\_1** window is open, showing a table of VIO signals:

Name	Value	Activity	Direction	VIO
<code>vio_data_mode_value[3:0]</code>	[H] 7		Output	hw_vio_1
<code>vio_modify_enable</code>	[B] 0		Output	hw_vio_1

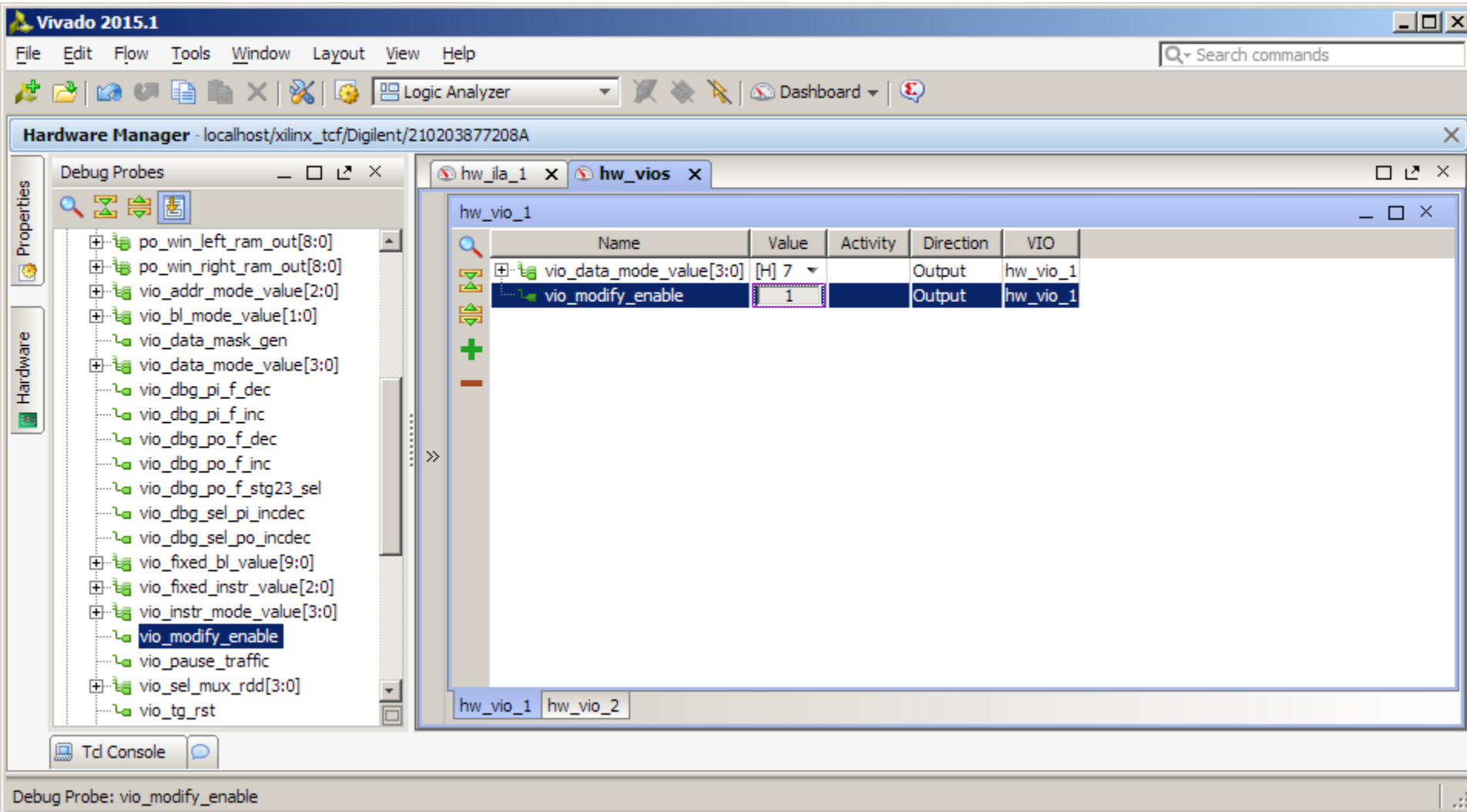
# Adjust Data Pattern using VIO Console

➤ Right click on `vio_modify_enable` and set to Toggle Button



# Adjust Data Pattern using VIO Console

➤ Toggle the `vio_modify_enable` button to “1”



The screenshot shows the Vivado 2015.1 interface. The Hardware Manager window displays the hardware tree on the left and the VIO console on the right. The VIO console for `hw_vio_1` shows the following table:

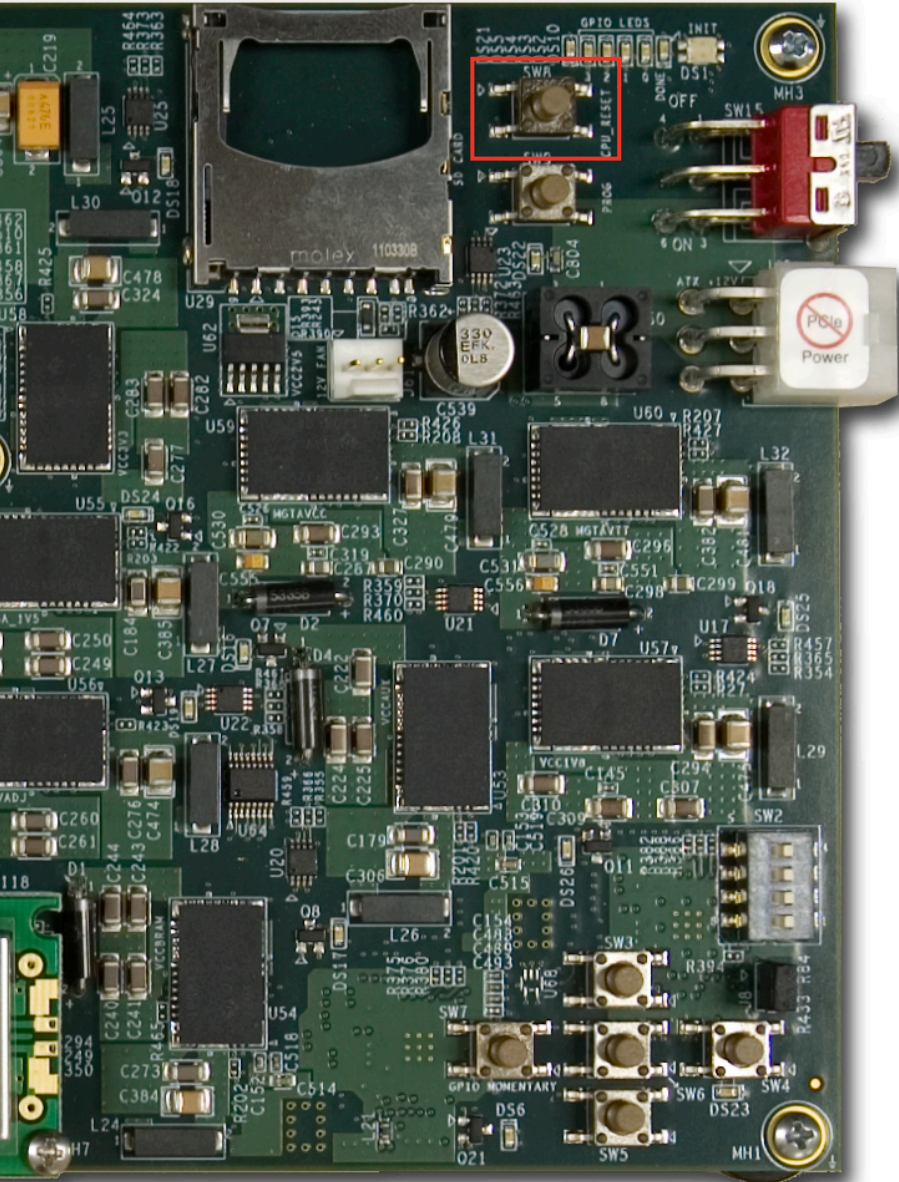
Name	Value	Activity	Direction	VIO
<code>vio_data_mode_value[3:0]</code>	[H] 7		Output	<code>hw_vio_1</code>
<code>vio_modify_enable</code>	1		Output	<code>hw_vio_1</code>

The `vio_modify_enable` signal is highlighted in blue, and its value is set to 1. The Hardware tree on the left shows the `vio_modify_enable` signal selected.

Note: Presentation applies to the AC701



# Run MIG Example Design



- Press and release the CPU RESET switch, SW8, after each change to `vio_modify_enable` or `vio_data_mode_value`

# Adjust Data Pattern using VIO Console

- Select the hw\_ila\_1 tab
- Under Status, click Run Trigger Immediately

The screenshot shows the Vivado 2015.1 interface. The Hardware Manager window is open, displaying the hw\_ila\_1 tab. The Status window for hw\_ila\_1 shows the Core status as Idle and the Capture status as Idle. The Run Trigger Immediately button is highlighted with a red box. The Waveform window for hw\_ila\_1 shows a table of debug data.

Name	Value
dbg_rddata_valid_r	1
dbg_rddata_r[63:0]	b8b8b8b8b8b8b8b8
dbg_tg_c..._error_1	0
dbg_cmp_data_valid	1
dbg_cmp_error	0

The waveform window shows a table of debug data with columns for time (414, 415, 416) and values. The values are highlighted in green.

Time	Value
414	0000000000000000
415	0808080808080808
416	1010...

At the bottom of the window, there is a button labeled 'Run trigger immediate for this ILA core'.

# Adjust Data Pattern using VIO Console

## ➤ View PRBS data

The screenshot shows the Vivado 2015.1 interface. The Hardware Manager window is open, displaying a waveform for hw\_ila\_1. The waveform is titled "Waveform - hw\_ila\_1" and shows several signals. The signal dbg\_rddata\_r[63:0] is highlighted, showing PRBS data values at time steps 414, 415, 416, and 417. The values are: 6bd7ae5..., 356ad5ab56ad5ab5, 2244881123468d1a, and 43860c193264c891. The signal dbg\_rddata\_valid\_r is 0, dbg\_tg\_compare\_error\_1 is 1, dbg\_cmp\_data\_valid is 0, and dbg\_cmp\_error is 0.

Name	Value	414	415	416	417
dbg_rddata_valid_r	0				
dbg_rddata_r[63:0]	3a75ead4a953a64c	6bd7ae5...	356ad5ab56ad5ab5	2244881123468d1a	43860c193264c891
dbg_tg_compare_error_1	1				
dbg_cmp_data_valid	0				
dbg_cmp_error	0				



# References

# References

## ➤ Artix-7 Memory

- 7 Series FPGAs Memory Interface Solutions User Guide – UG586
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/mig\\_7series/v2\\_3/ug586\\_7Series\\_MIS.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v2_3/ug586_7Series_MIS.pdf)
- MIG 7 Series – Release Notes
  - <http://www.xilinx.com/support/answers/54025.htm>

## ➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf)

# Documentation

# Documentation

## ➤ Artix-7

- Artix-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm>
- Design Advisory Master Answer Record for Artix-7 FPGAs
  - <http://www.xilinx.com/support/answers/51456.htm>

## ➤ AC701 Documentation

- Artix-7 FPGA AC701 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html>
- AC701 Getting Started Guide – UG967
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ac701/2014\\_3/ug967-ac701-eval-kit-getting-started.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ac701/2014_3/ug967-ac701-eval-kit-getting-started.pdf)
- AC701 User Guide – UG952
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ac701/ug952-ac701-a7-eval-bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ac701/ug952-ac701-a7-eval-bd.pdf)