
# AC701 MIG Design Creation

**April 2015**

XTP225

# Revision History

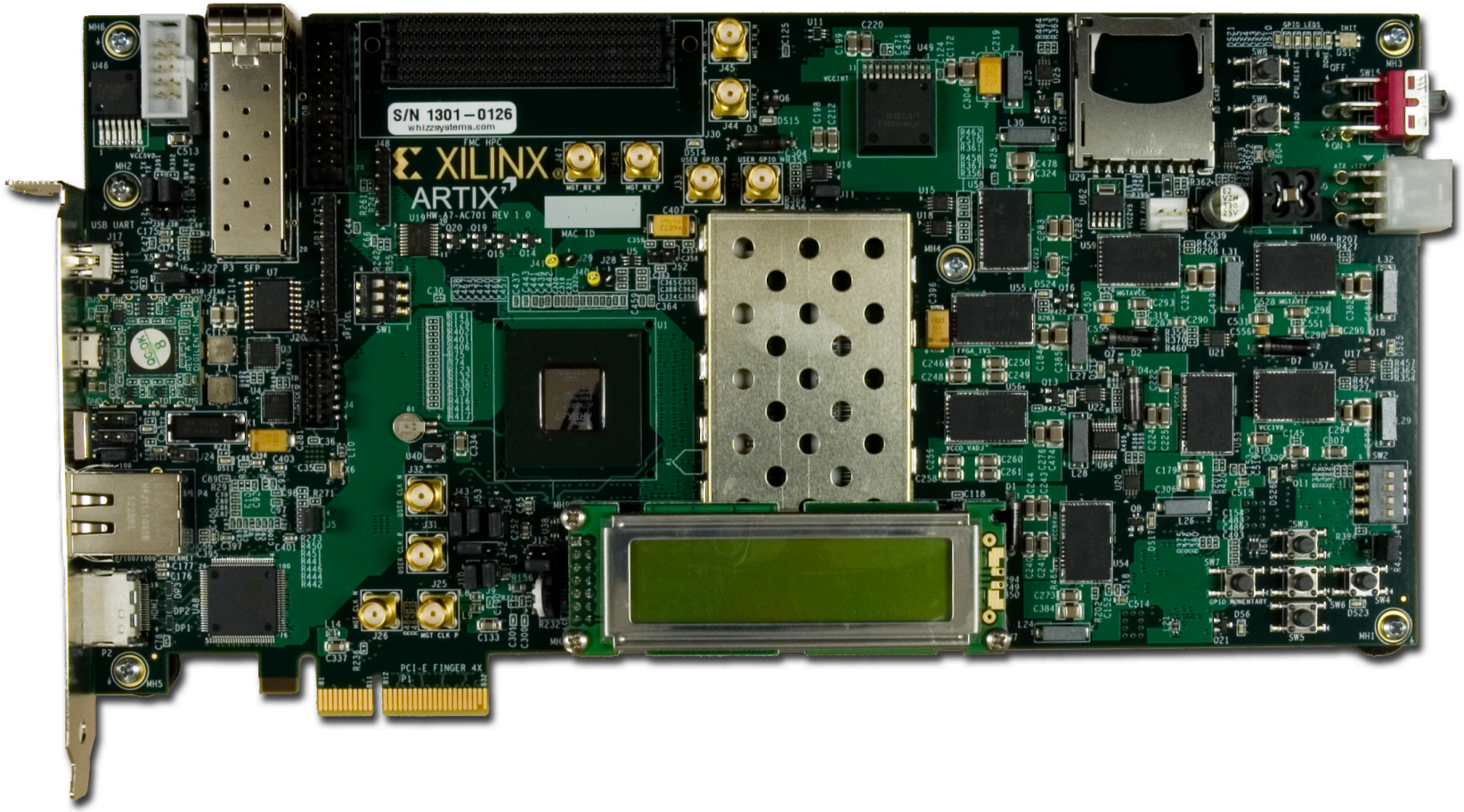
| Date | Version | Description |
|---|---|---|
| 04/30/14 | 11.0 | Regenerated for 2015.1. |
| 11/24/14 | 10.0 | Regenerated for 2014.4. |
| 10/08/14 | 9.0 | Regenerated for 2014.3. |
| 06/09/14 | 8.0 | Regenerated for 2014.2. |
| 04/16/14 | 7.0 | Regenerated for 2014.1. |
| 12/18/13 | 6.0 | Regenerated for 2013.4. |
| 10/23/13 | 5.0 | Regenerated for 2013.3. |
| 06/19/13 | 4.0 | Regenerated for 2013.2. AR55531 fixed. |
| 04/03/13 | 3.0 | Regenerated for 2013.1. AR53420 fixed. Added AR55531. |
| 02/04/13 | 2.1 | As per AR54044, added 2012.4 device pack. Added AR53420 and AR54223. |
| 12/18/12 | 2.0 | Regenerated for 2012.4 |
| 10/23/12 | 1.0 | Initial Version. |

# Overview

- Xilinx AC701 Board
- Software Requirements
- Generate MIG Example Design
- Modifications to Example Design
- Compile Example Design
- AC701 Setup
- Run MIG Example Design
  - Adjust Data Pattern using VIO Console
- References

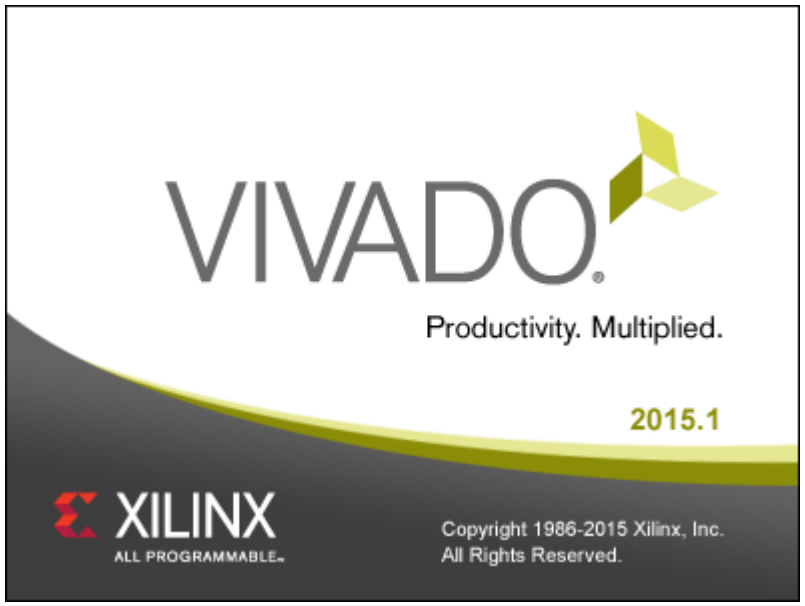
**Note:** This presentation applies to the AC701

# Xilinx AC701 Board



# Vivado Software Requirements

- Xilinx Vivado Design Suite 2015.1, Design Edition



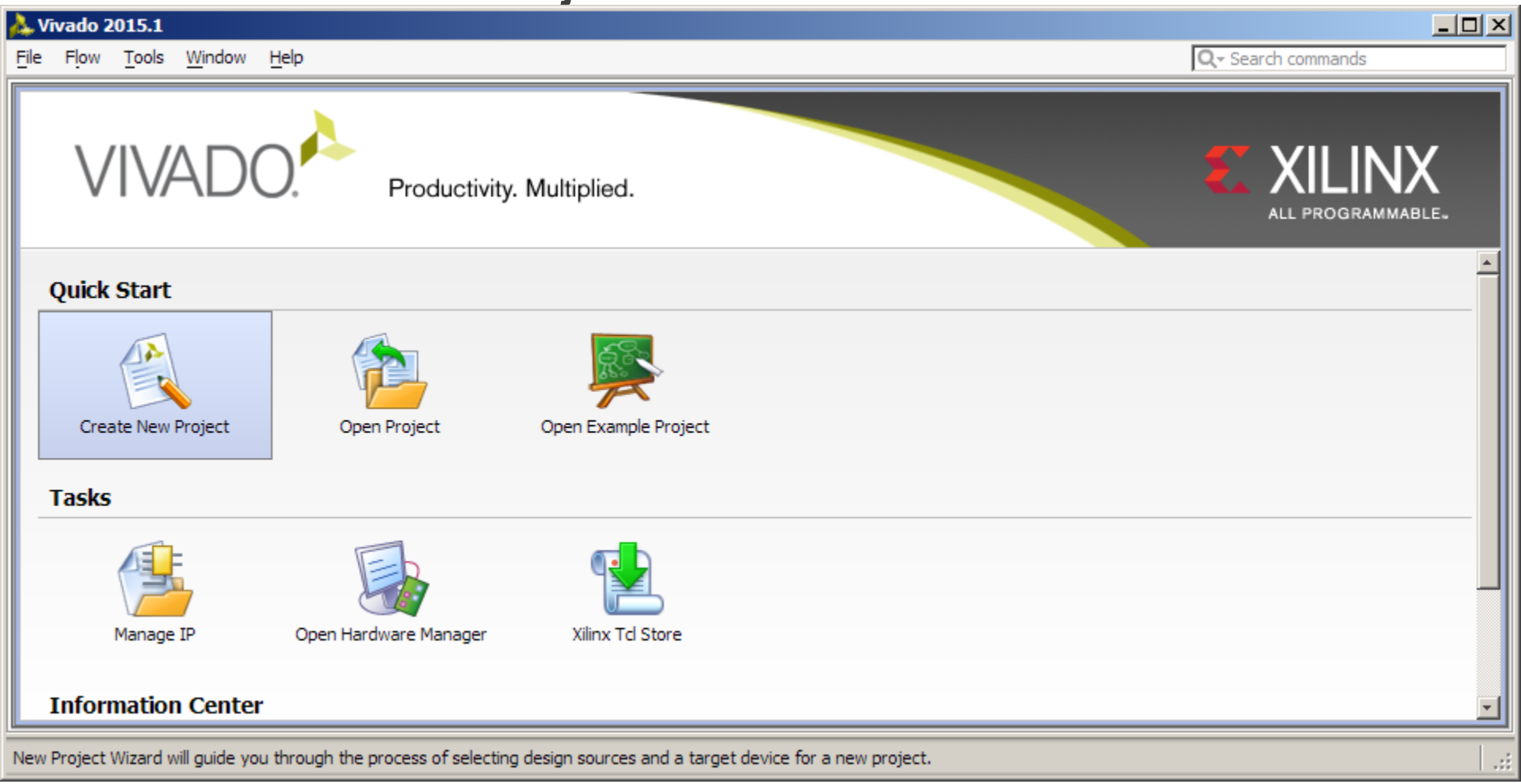

**Note:** Presentation applies to the AC701

# Generate MIG Example Design

- Open Vivado

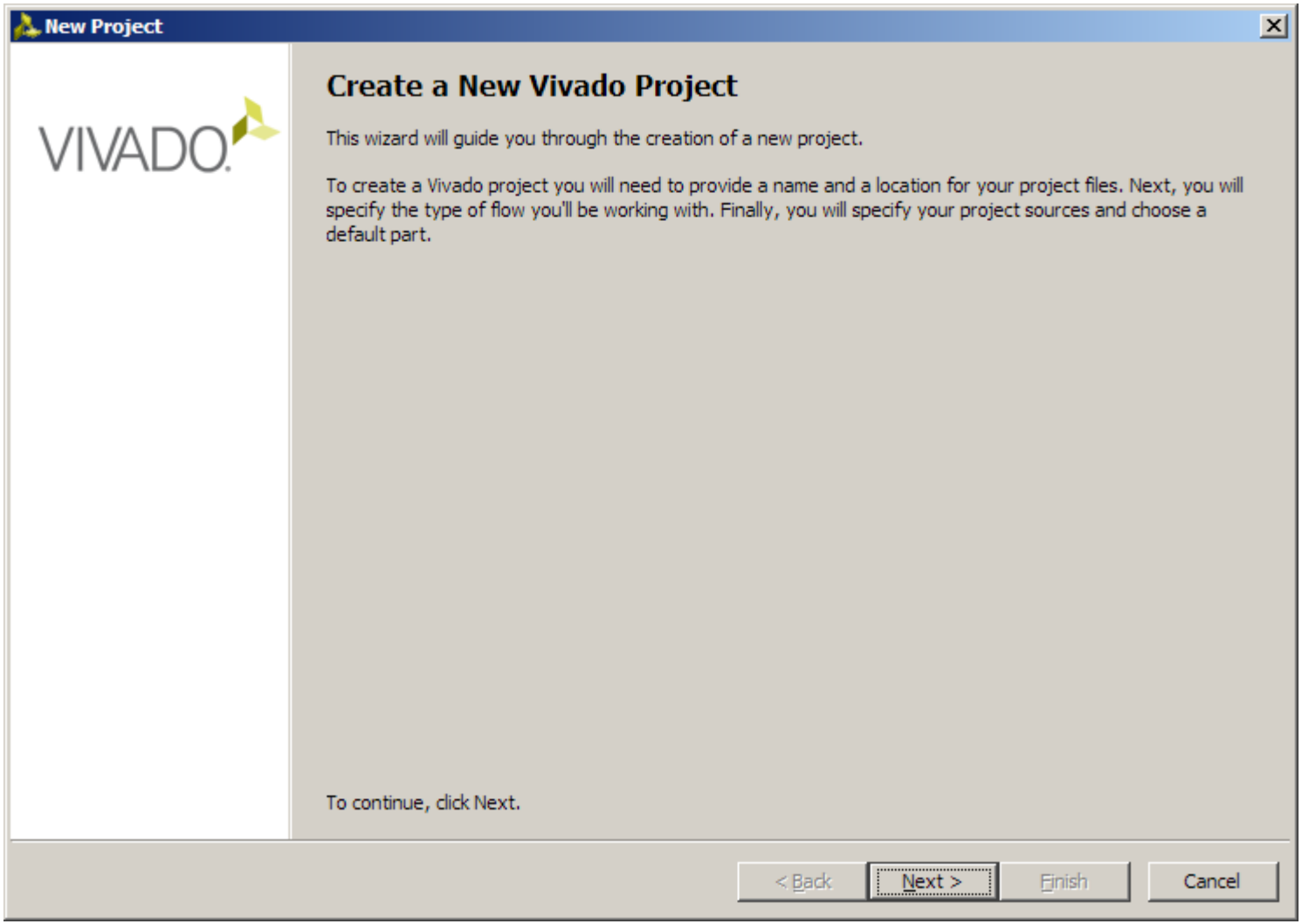
  **Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado**

- Select Create New Project



# Generate MIG Example Design

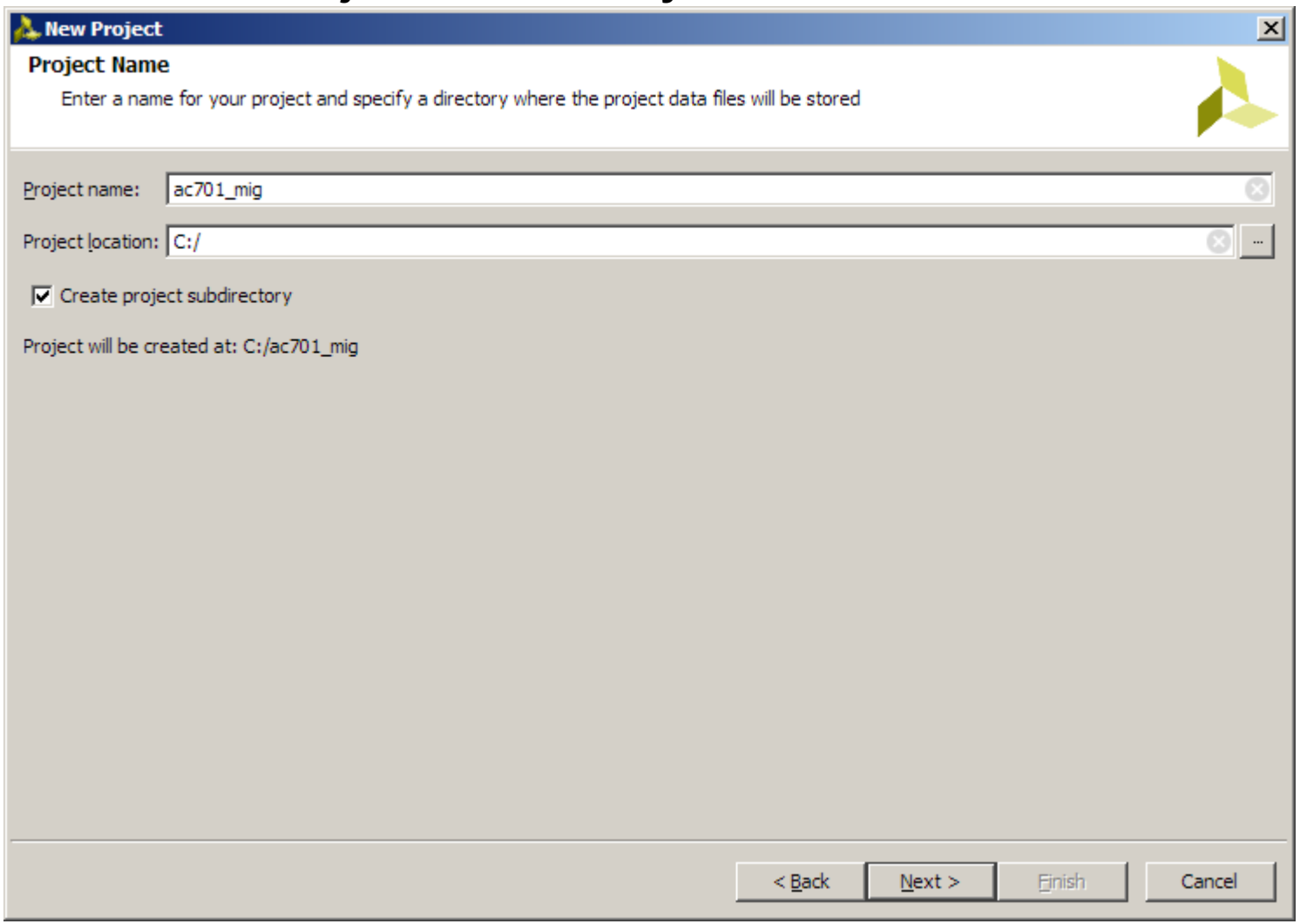
- Click Next




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

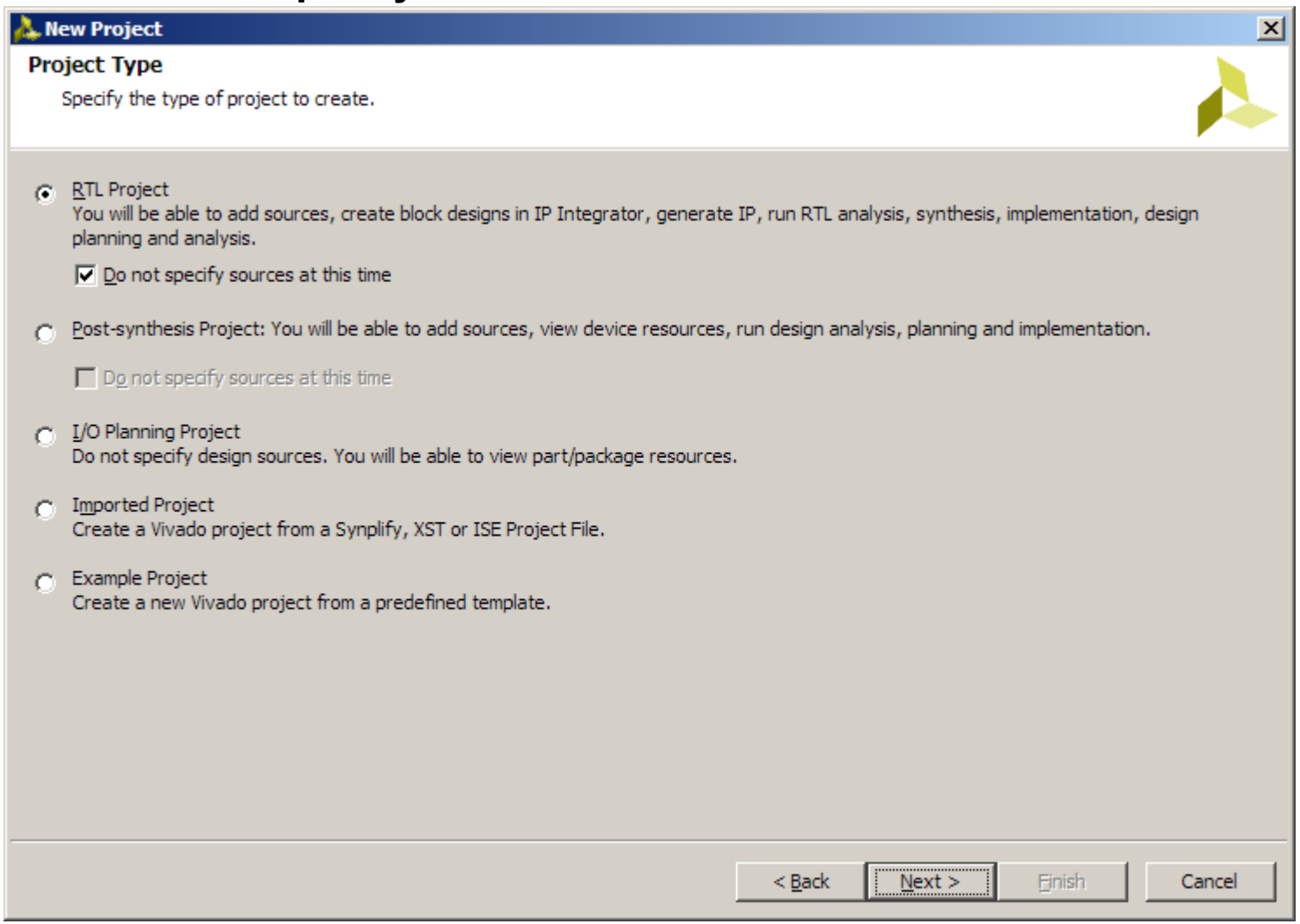
- **Set the Project name and location to ac701_mig and C:**
  - Check **Create Project Subdirectory**




**Note:** Vivado generally requires forward slashes in paths

# Generate MIG Example Design

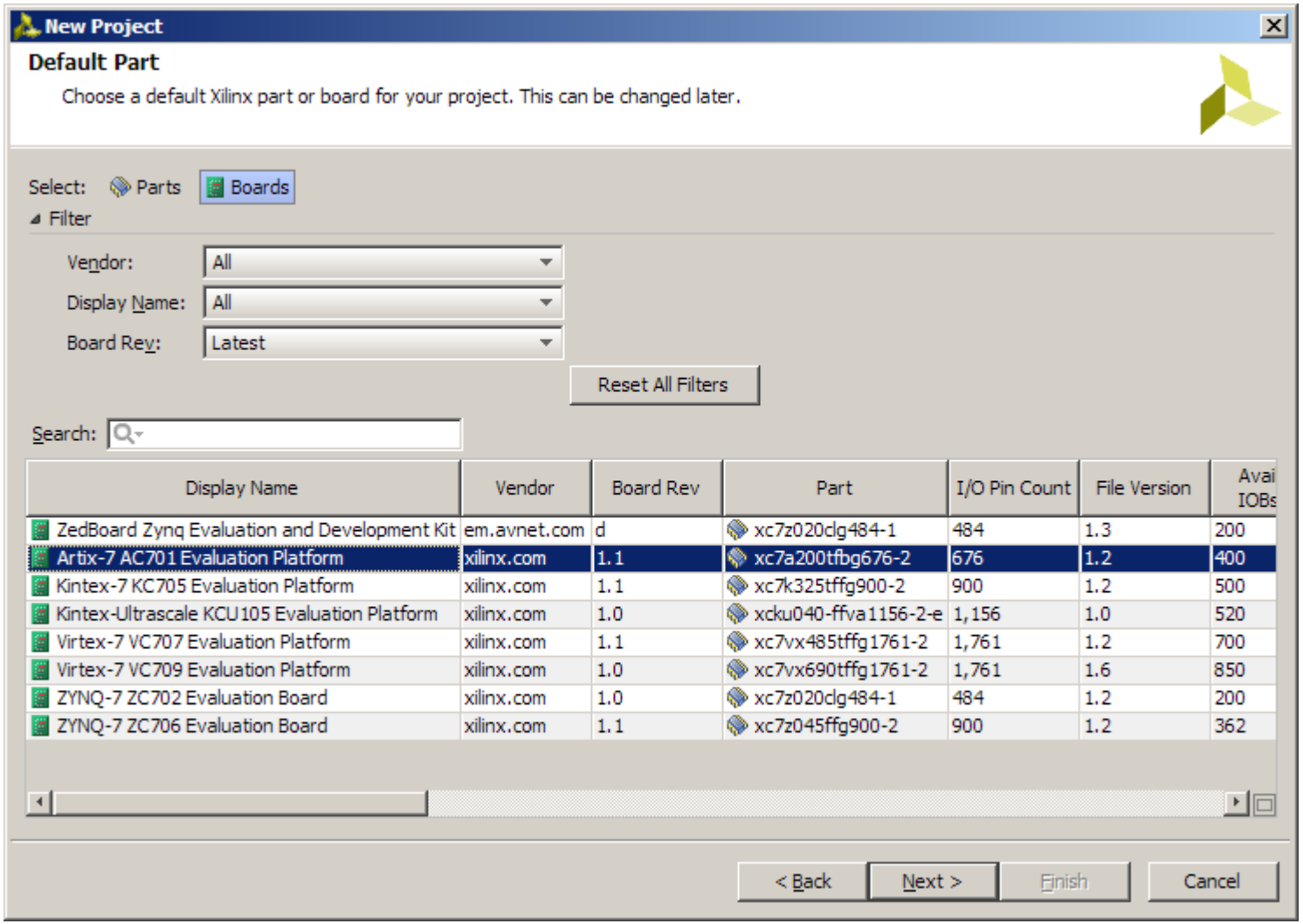
- **Select RTL Project**
  - Select **Do not specify sources at this time**




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

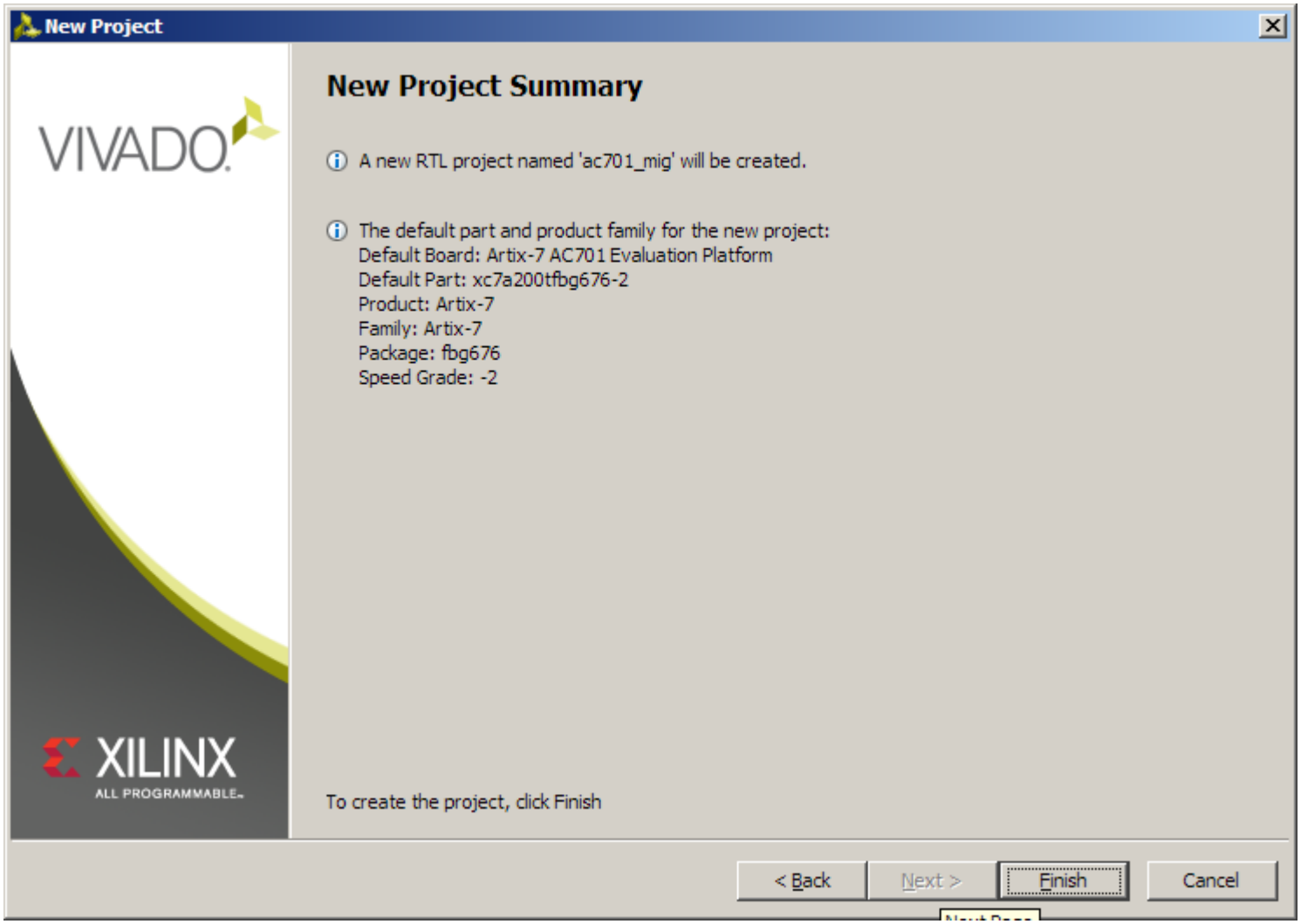
## Select the AC701 Board




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

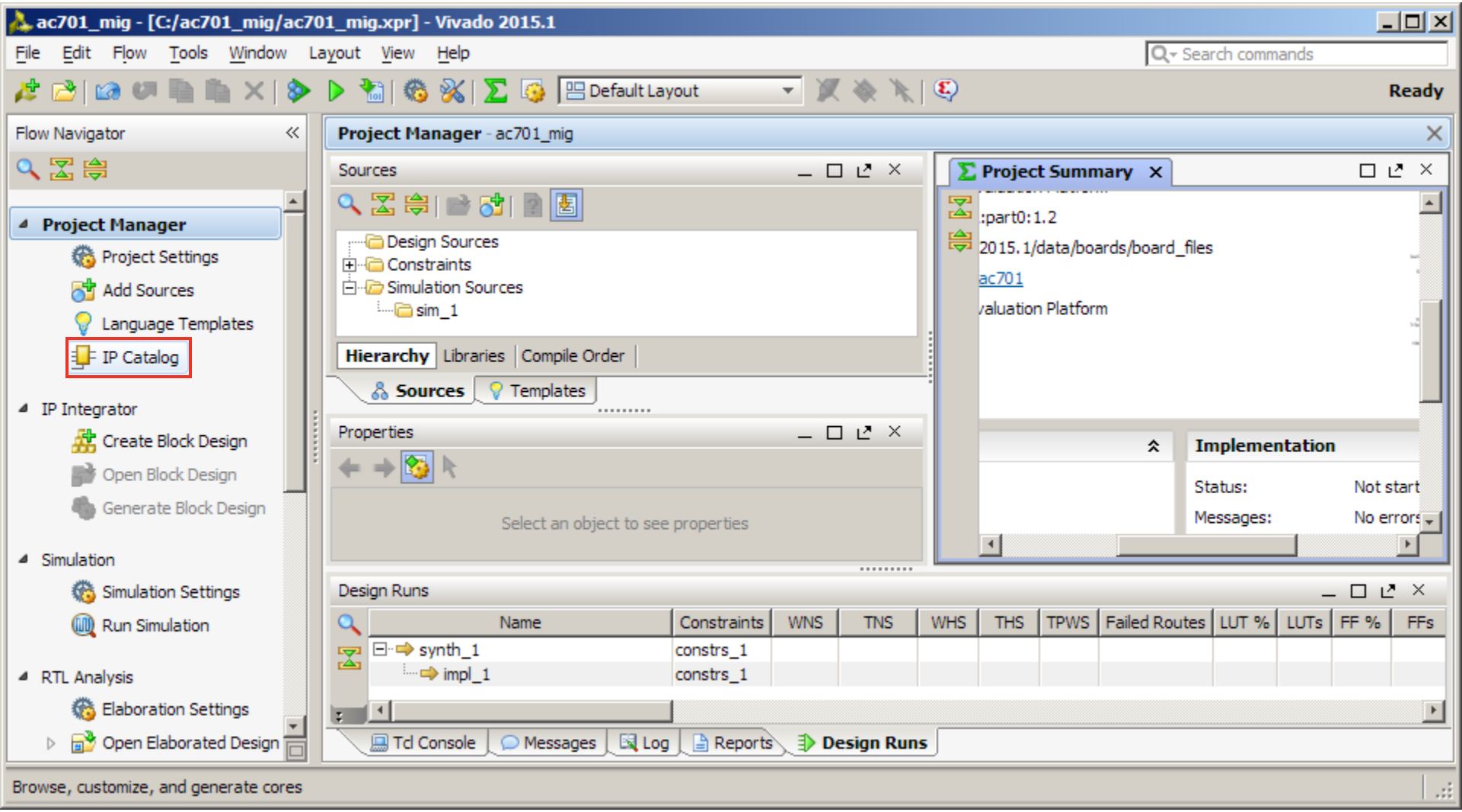
- Click Finish




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

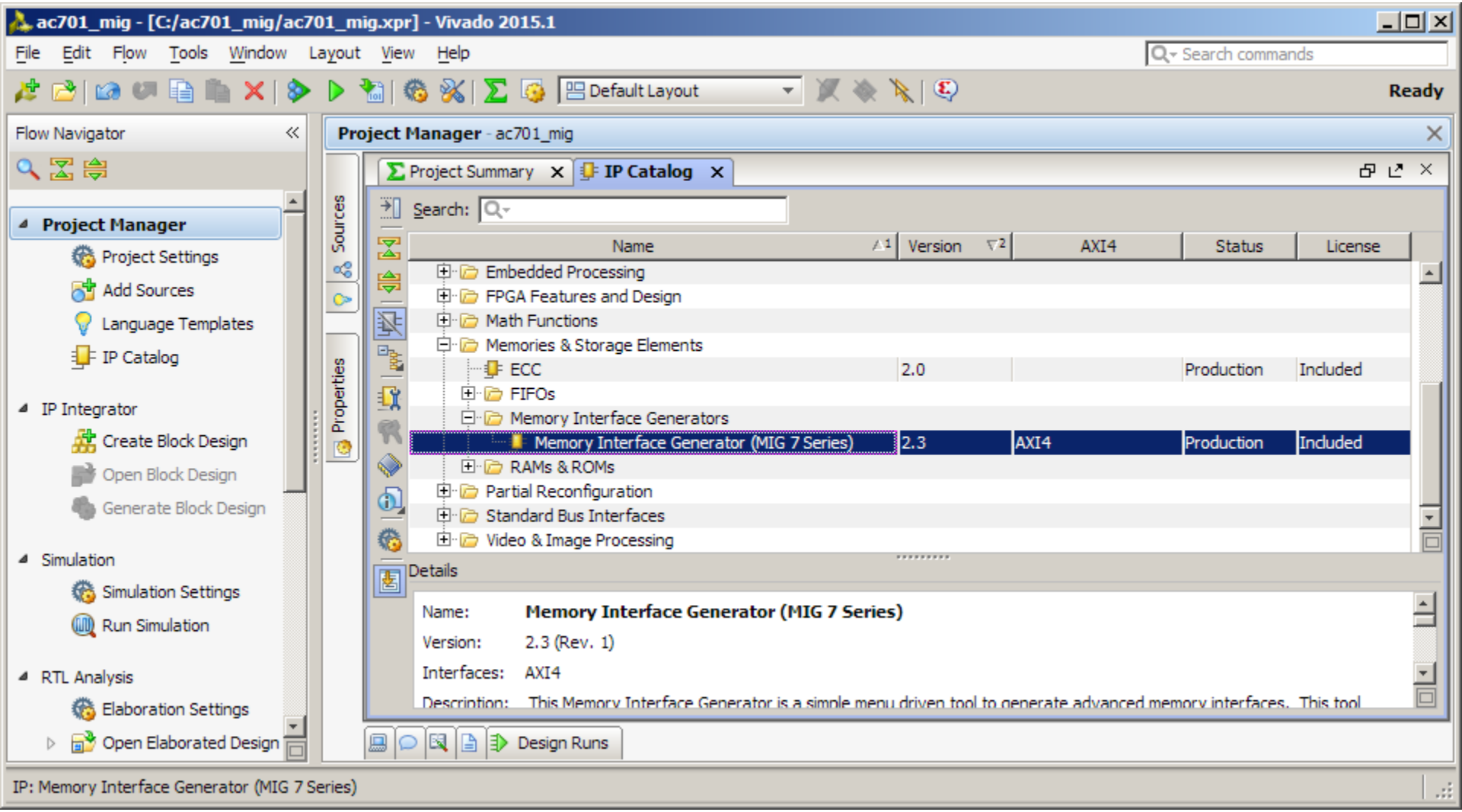
- Click on IP Catalog




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

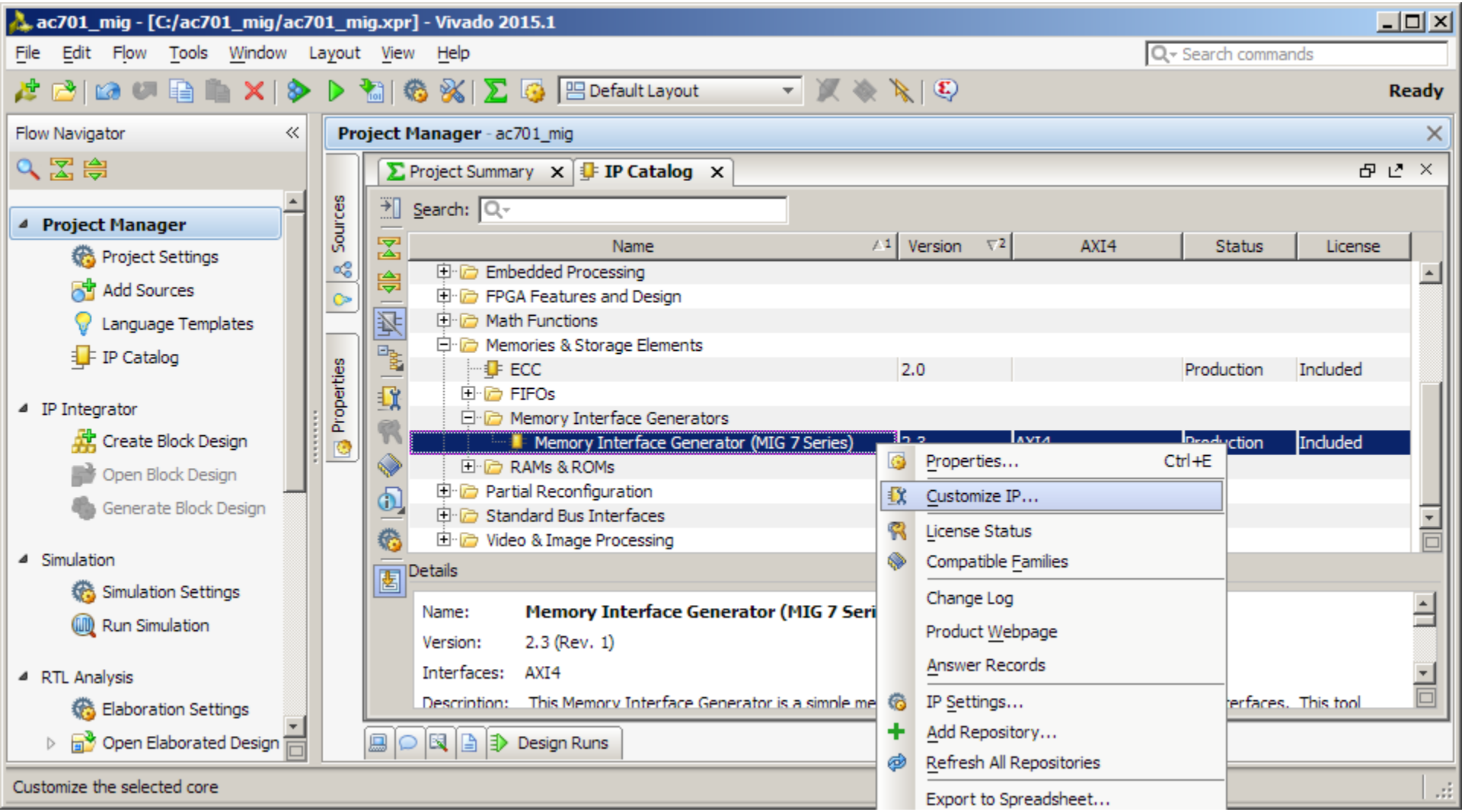
- Select MIG 7 Series, v2.3 under Memory Interface Generators




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

- Right click on MIG 7 Series
- Select Customize IP



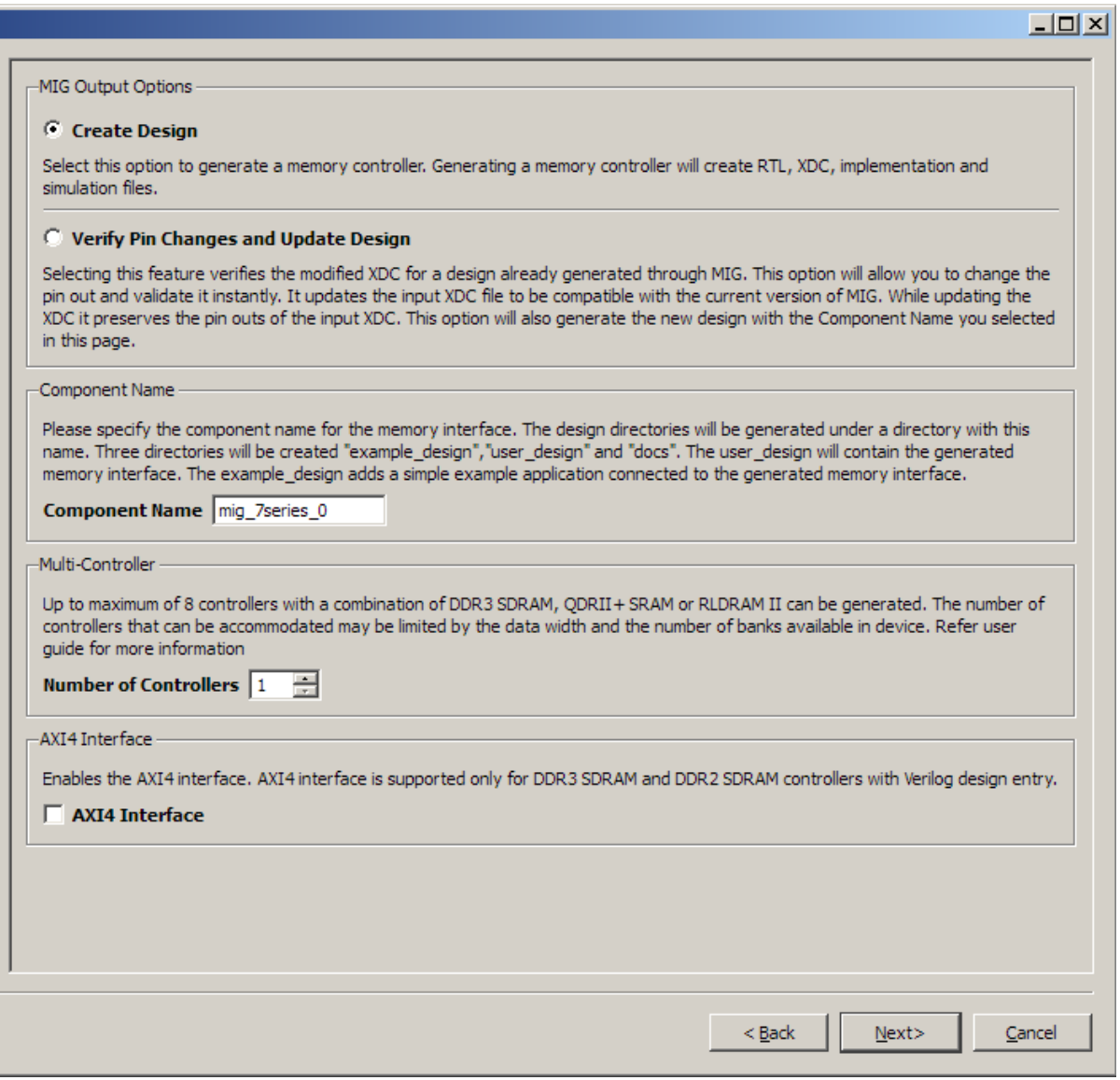

**Note:** Presentation applies to the AC701

# Generate MIG Example Design


- Leave this page as is
  - Click Next

**Note:** Presentation applies to the AC701

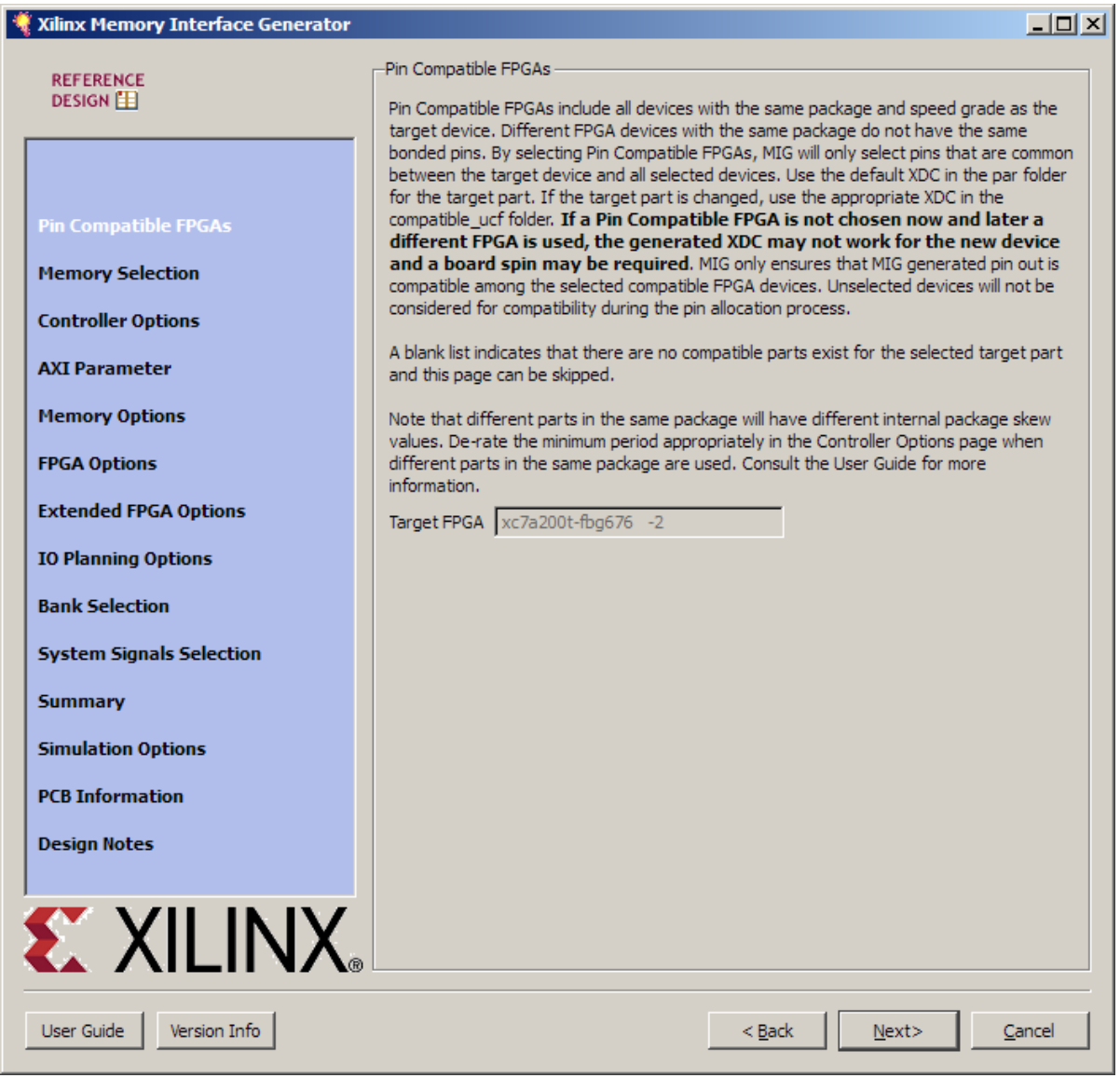
# Generate MIG Example Design




- **Leave this page as is**
  - Click Next

**Note:** Presentation applies to the AC701

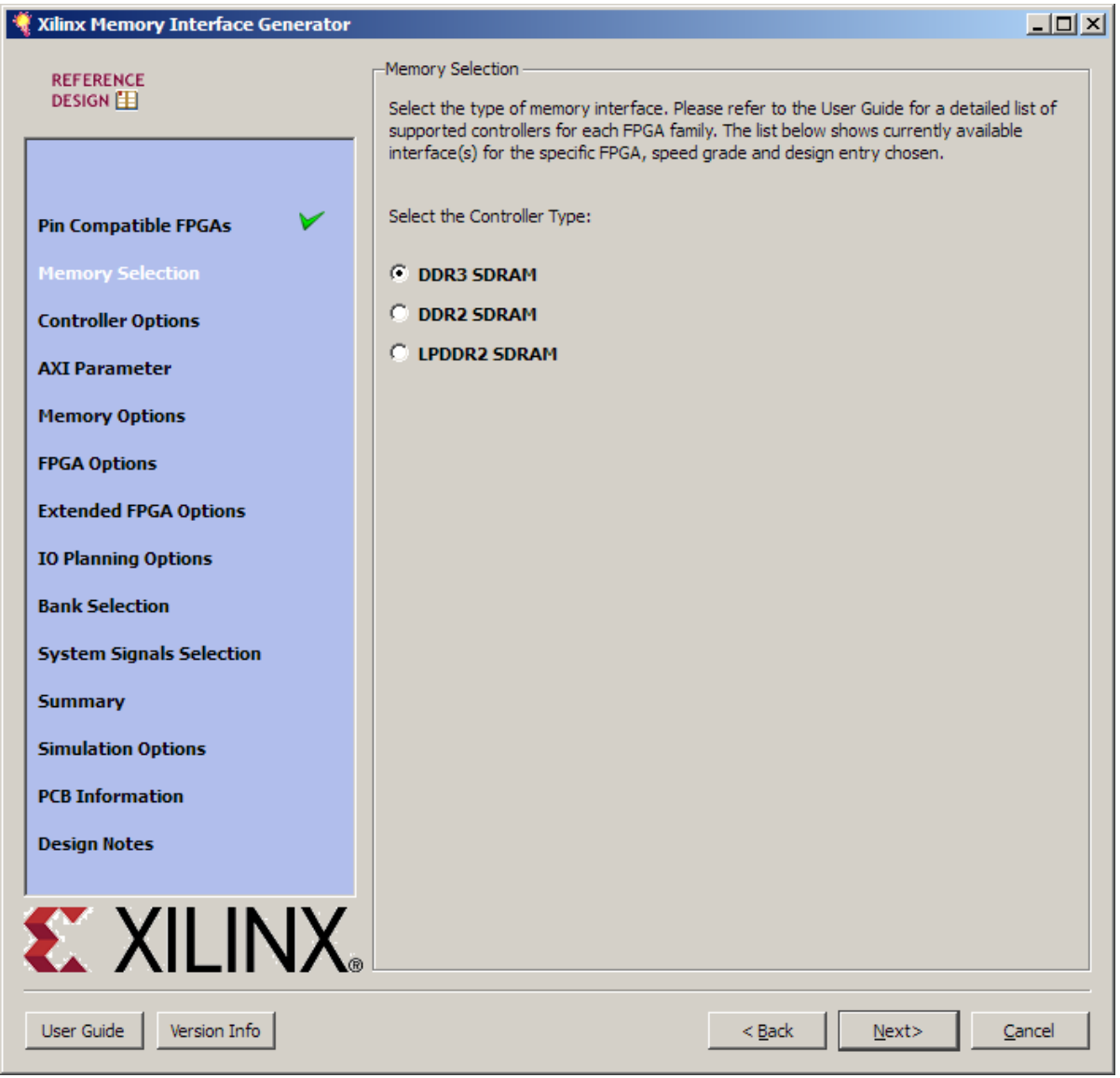
# Generate MIG Example Design




- Leave this page as is
  - Click Next

**Note:** Presentation applies to the AC701

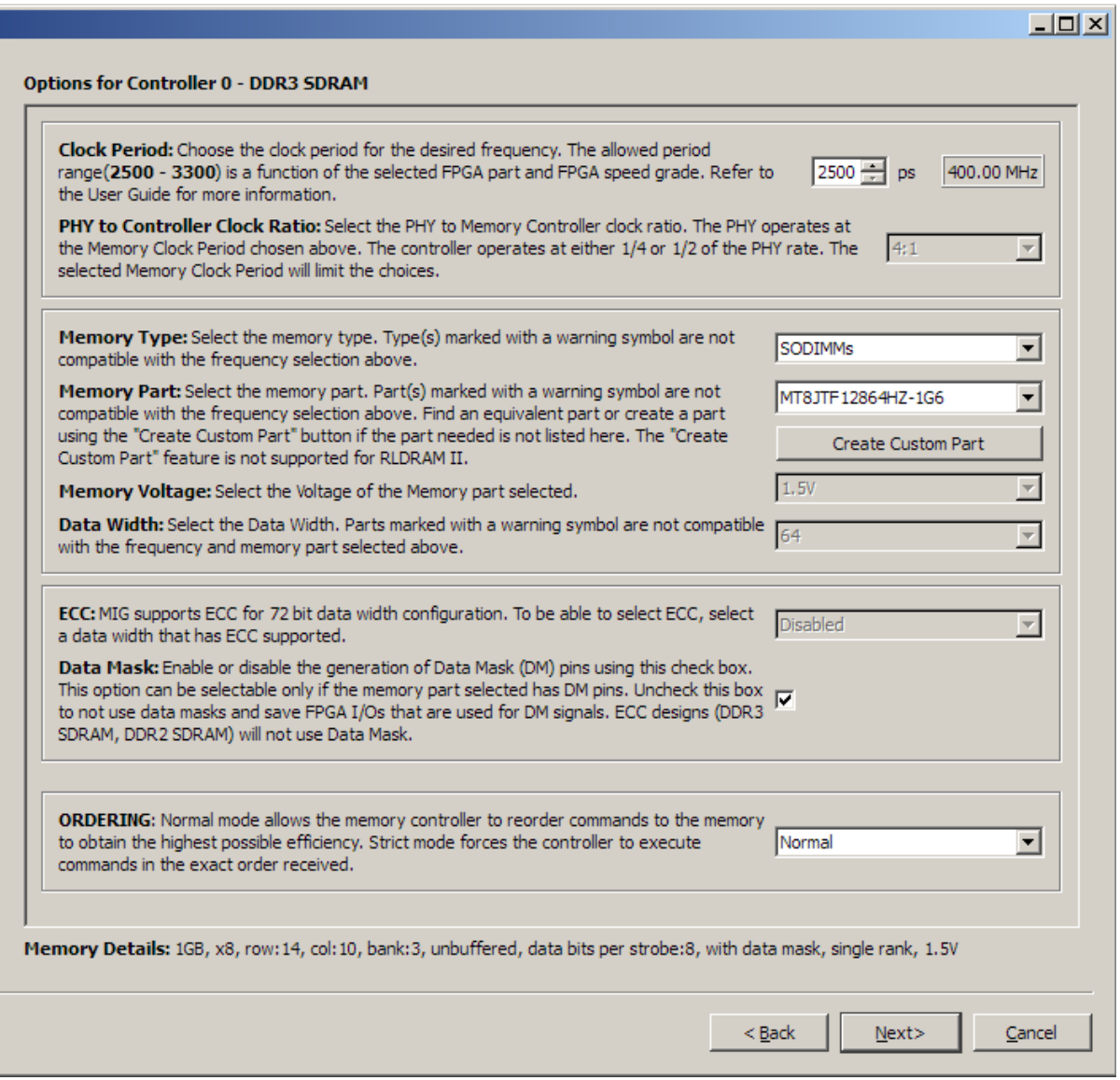
# Generate MIG Example Design




- **Select Memory Type**
  - DDR3 SDRAM
  - Click Next

**Note:** Presentation applies to the AC701

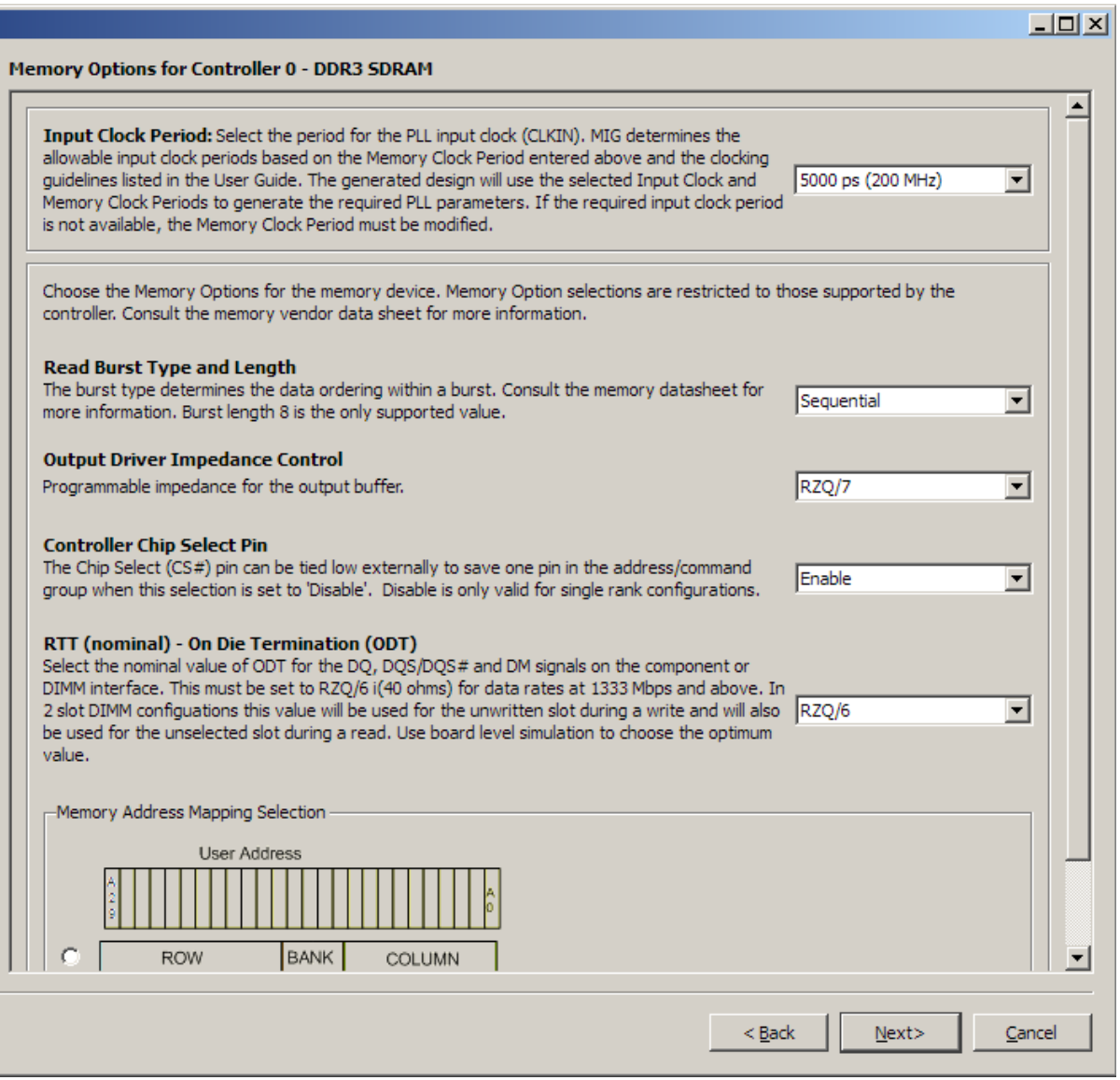
# Generate MIG Example Design




- **Select**
  - Clock Period: **2500 ps**
  - Type: **SODIMMs**
  - Part: **MT8JTF12864HZ-1G6**
  - Data Mask: **Checked**
  - Click Next

**Note:** Presentation applies to the AC701

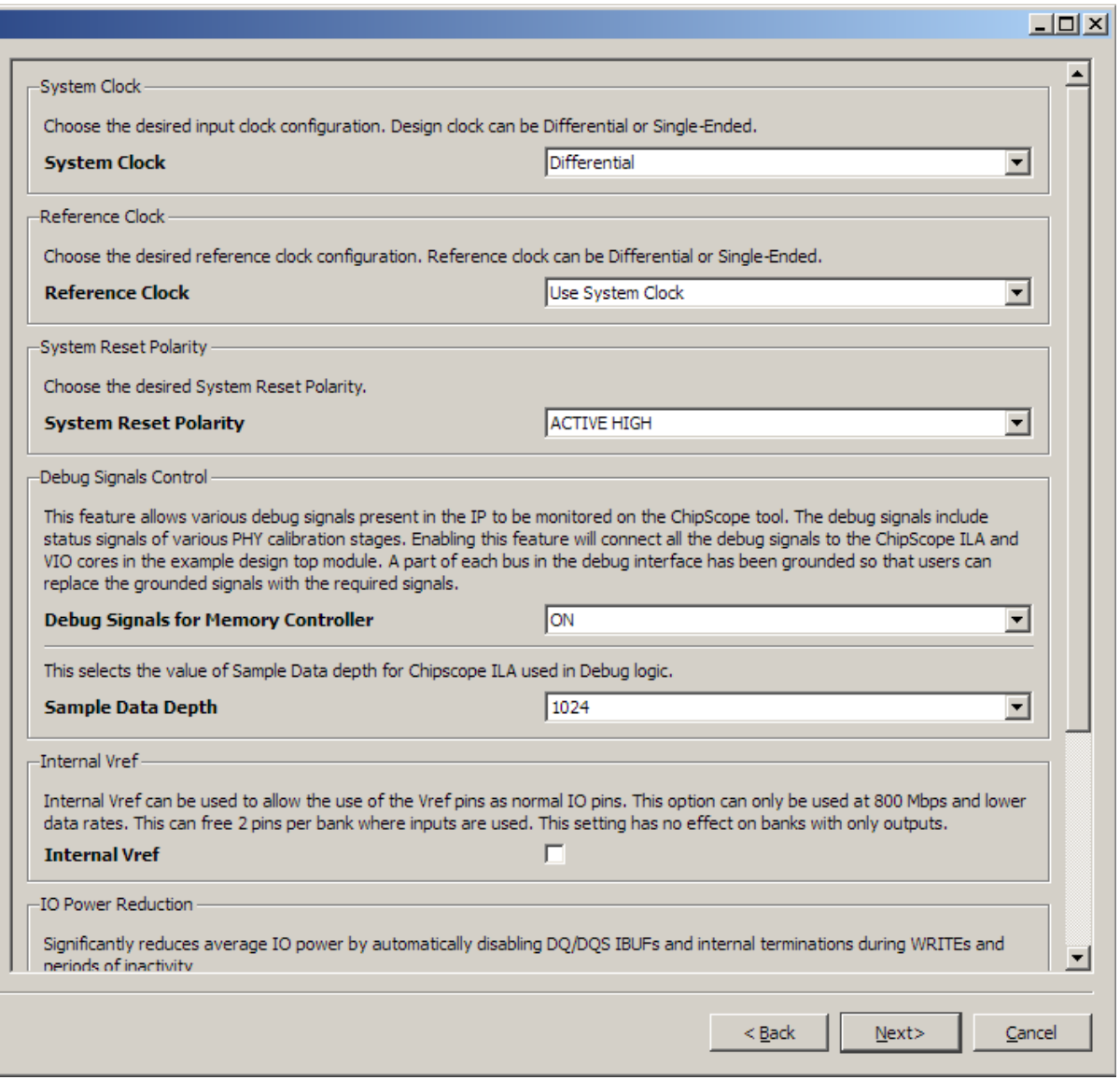
# Generate MIG Example Design




- **Select:**
  - Input Clock Period: **5000 ps**
  - RTT: **RZQ/6**
  - Click Next

**Note:** Presentation applies to the AC701

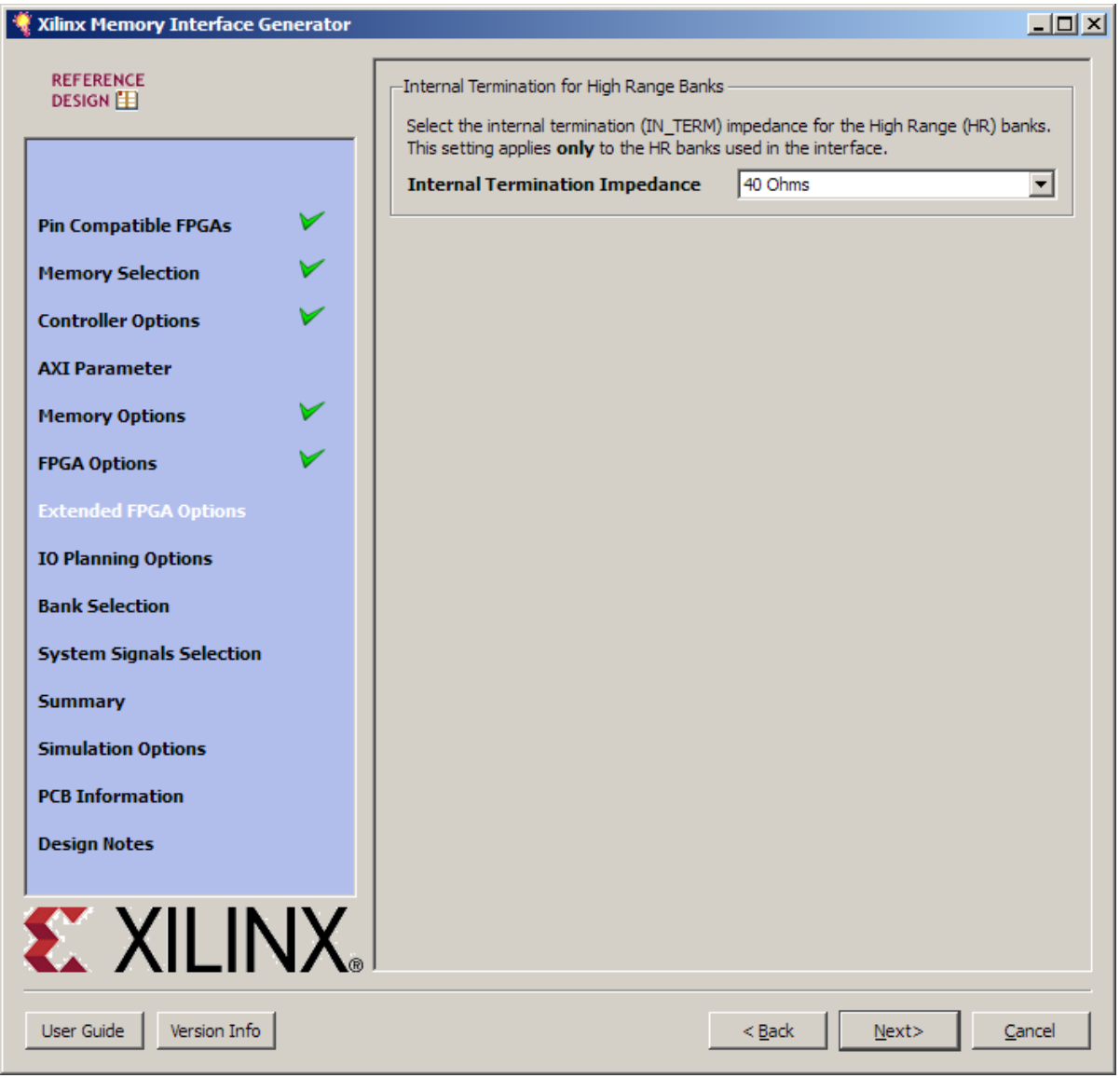
# Generate MIG Example Design




- **Select**
  - Reference Clock: **Use System Clock**
  - System Reset: **Active HIGH**
  - Debug: **ON**
  - Click Next

**Note:** Presentation applies to the AC701

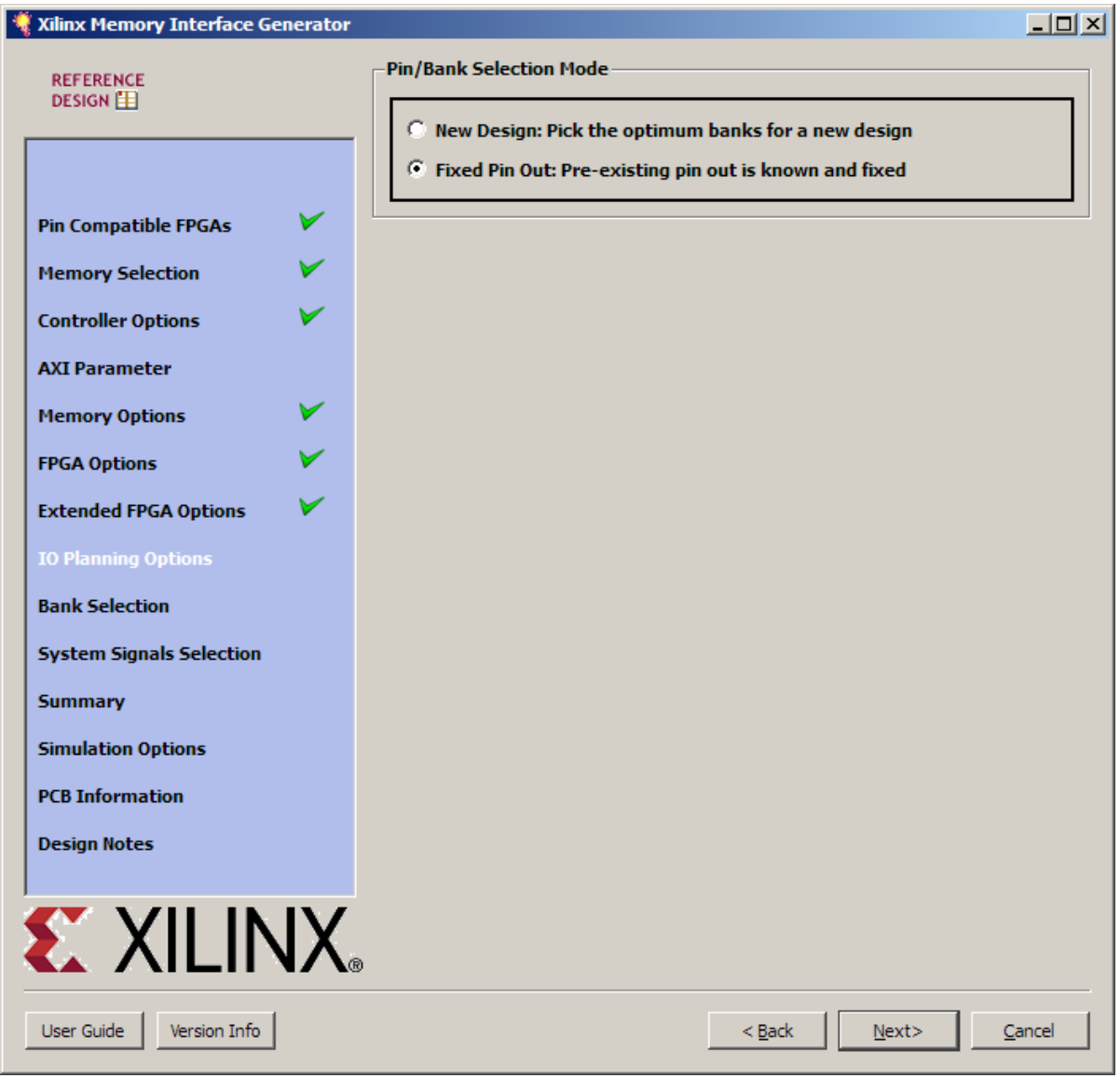
# Generate MIG Example Design




- **Set Internal Termination Impedance to 40 Ohms**
  - Click Next

**Note:** Presentation applies to the AC701

# Generate MIG Example Design

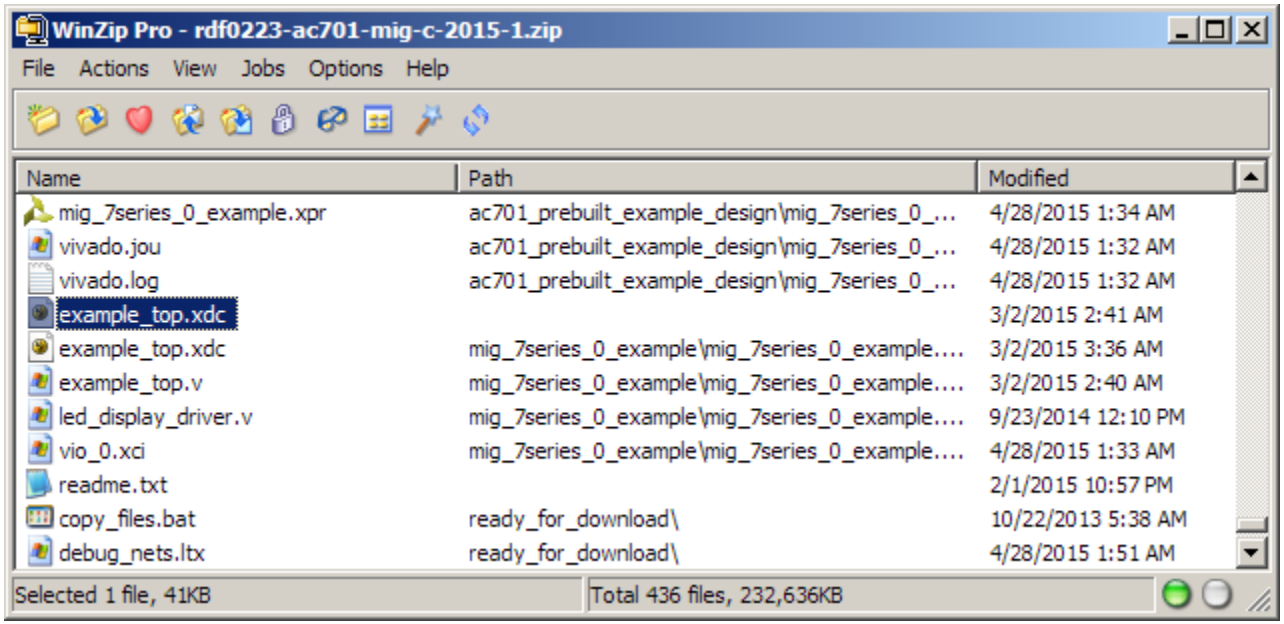



- **Select Fixed Pin Out**
  - Click Next

**Note:** Presentation applies to the AC701

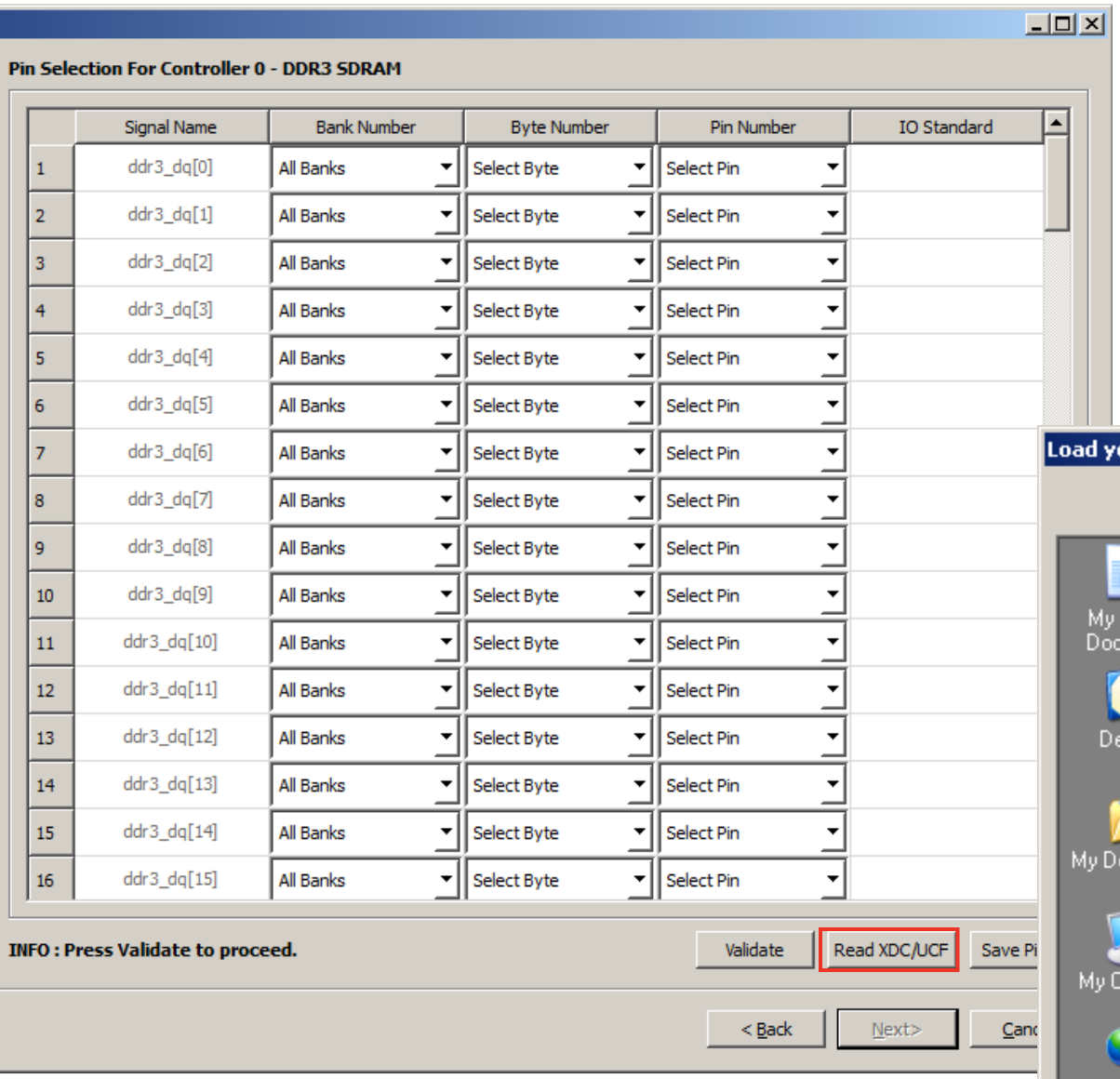
# Modifications to Example Design

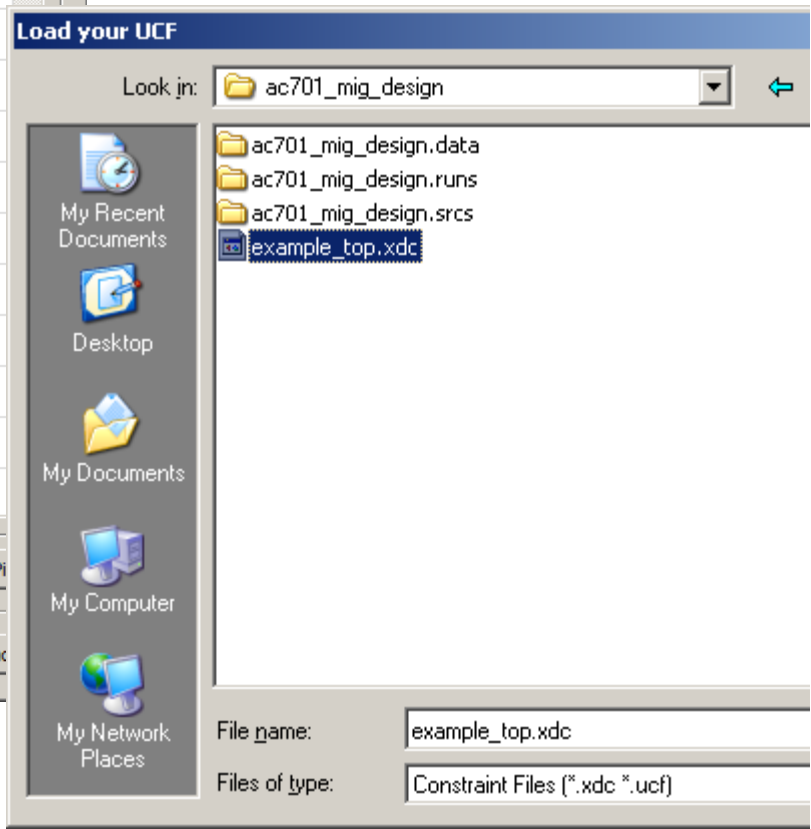
- **Open the AC701 MIG Design Files (2015.1 C) ZIP file**
  - Available through http://www.xilinx.com/ac701
  - Extract the file, "**example_top.xdc**" *only* to C:\ac701_mig
  - Contains the XDC constraints needed for AC701 MIG design
  - This zip file will be needed later in the presentation




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

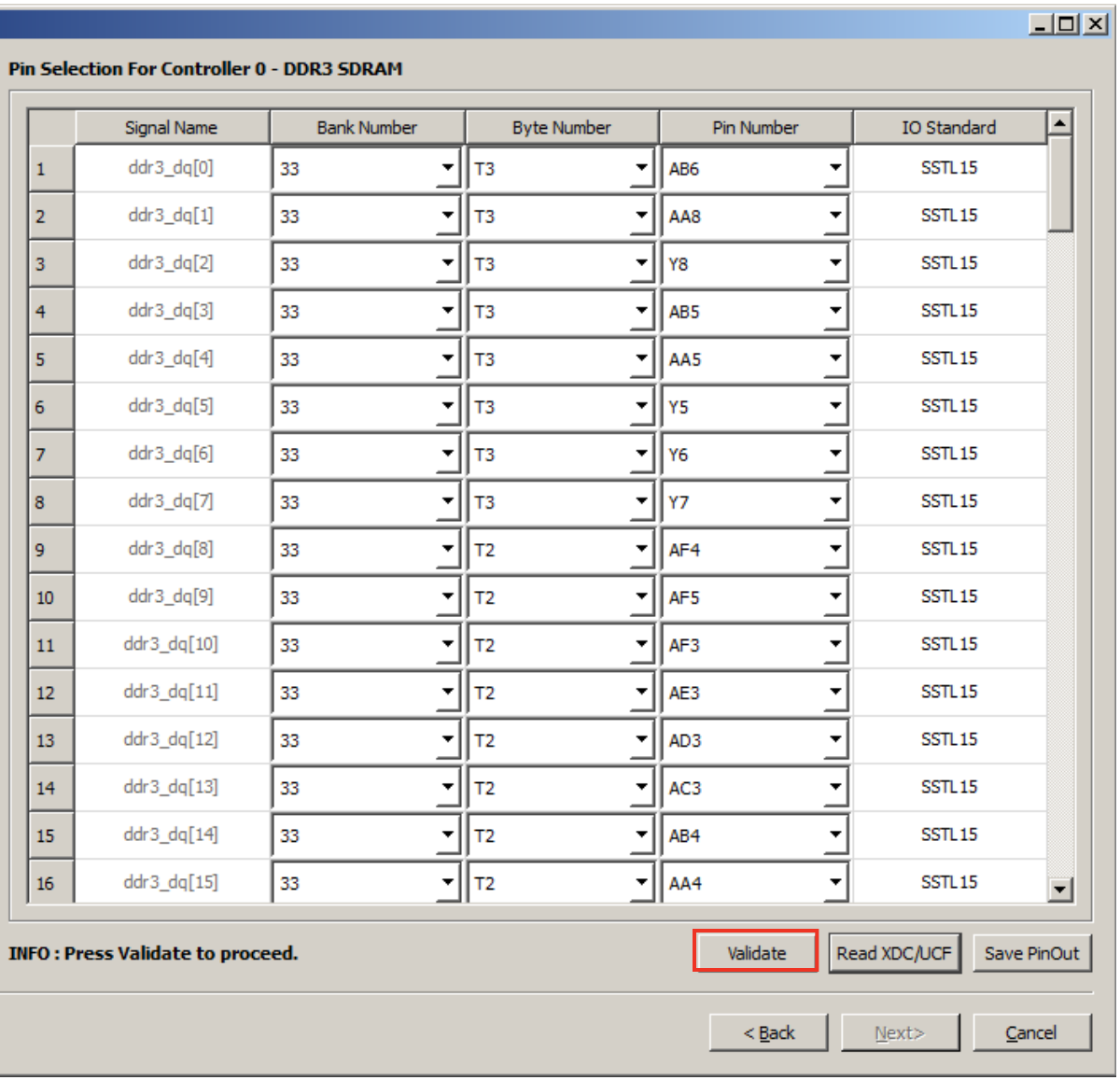


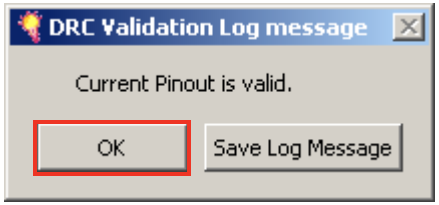

- **Select Read XDC/UCF**
  - Open the file: example_top.xdc

**Note:** Presentation applies to the AC701

# Generate MIG Example Design

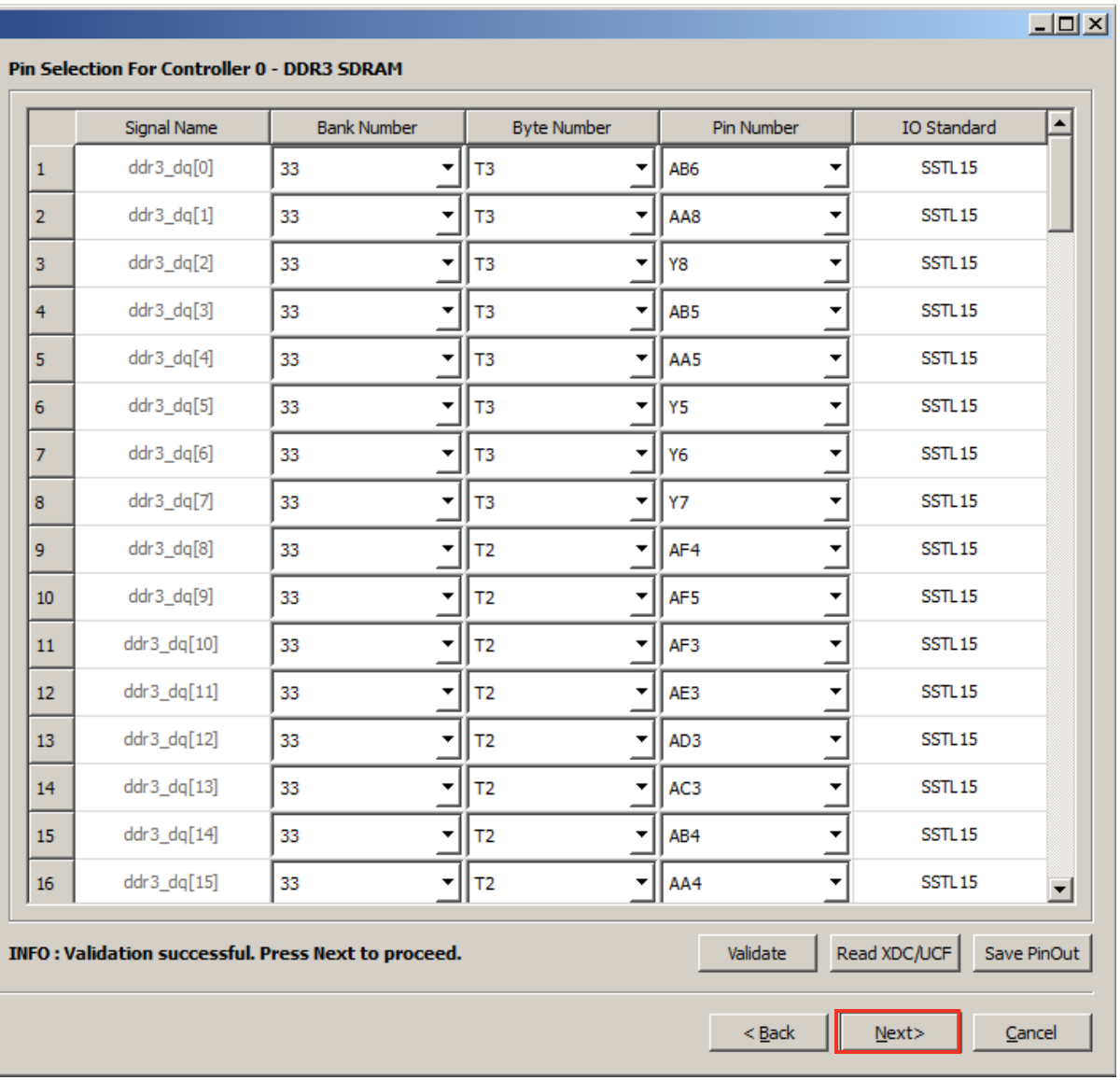



- Once it finishes reading in the XDC, click Validate
  - Click OK




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

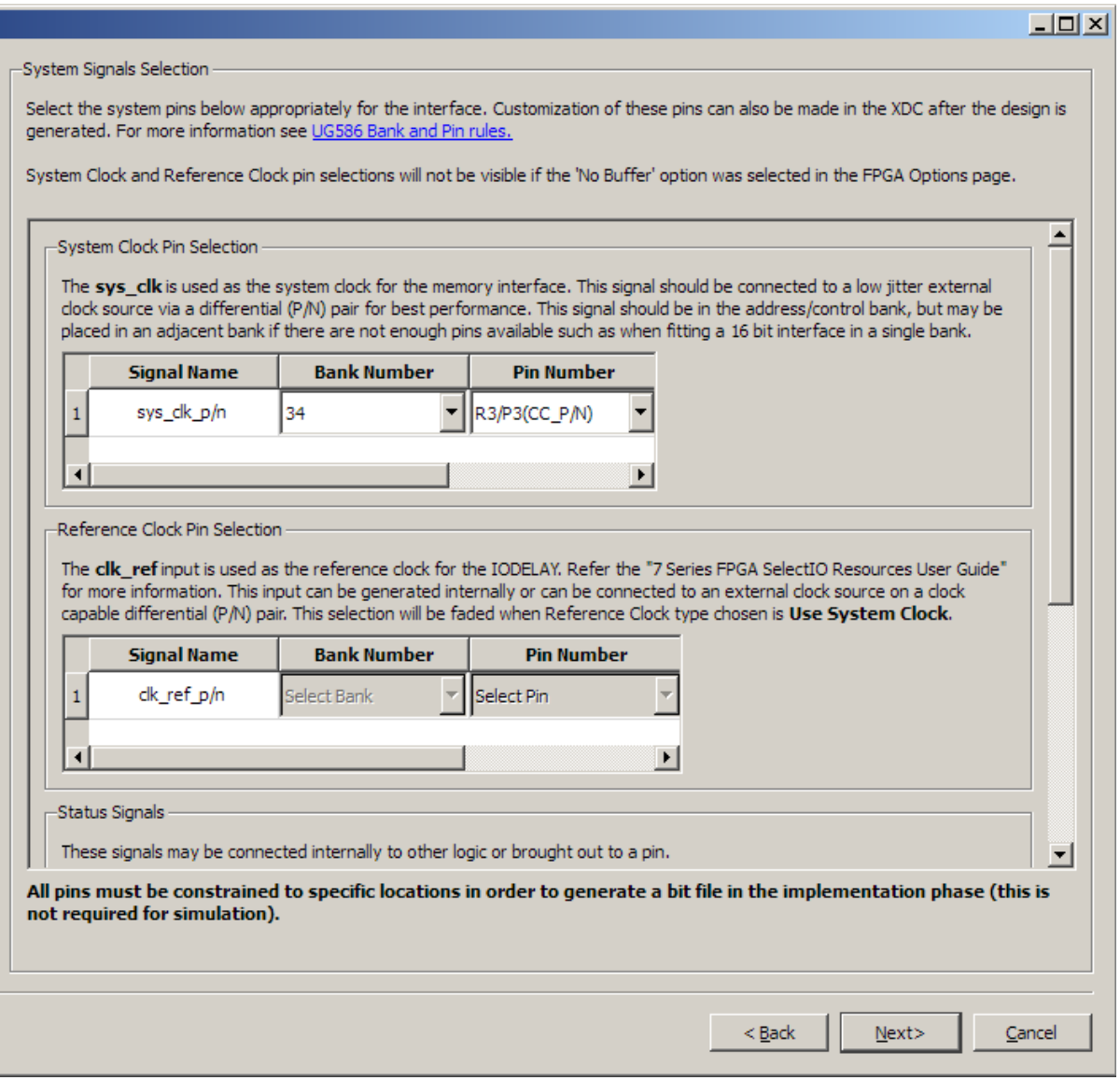



| | Signal Name | Bank Number | Byte Number | Pin Number | IO Standard |
|---|---|---|---|---|---|
| 1 | ddr3_dq[0] | 33 | T3 | AB6 | SSTL15 |
| 2 | ddr3_dq[1] | 33 | T3 | AA8 | SSTL15 |
| 3 | ddr3_dq[2] | 33 | T3 | Y8 | SSTL15 |
| 4 | ddr3_dq[3] | 33 | T3 | AB5 | SSTL15 |
| 5 | ddr3_dq[4] | 33 | T3 | AA5 | SSTL15 |
| 6 | ddr3_dq[5] | 33 | T3 | Y5 | SSTL15 |
| 7 | ddr3_dq[6] | 33 | T3 | Y6 | SSTL15 |
| 8 | ddr3_dq[7] | 33 | T3 | Y7 | SSTL15 |
| 9 | ddr3_dq[8] | 33 | T2 | AF4 | SSTL15 |
| 10 | ddr3_dq[9] | 33 | T2 | AF5 | SSTL15 |
| 11 | ddr3_dq[10] | 33 | T2 | AF3 | SSTL15 |
| 12 | ddr3_dq[11] | 33 | T2 | AE3 | SSTL15 |
| 13 | ddr3_dq[12] | 33 | T2 | AD3 | SSTL15 |
| 14 | ddr3_dq[13] | 33 | T2 | AC3 | SSTL15 |
| 15 | ddr3_dq[14] | 33 | T2 | AB4 | SSTL15 |
| 16 | ddr3_dq[15] | 33 | T2 | AA4 | SSTL15 |

- **The Next button is enabled once the pinout is validated.**
  - Click Next

**Note:** Presentation applies to the AC701

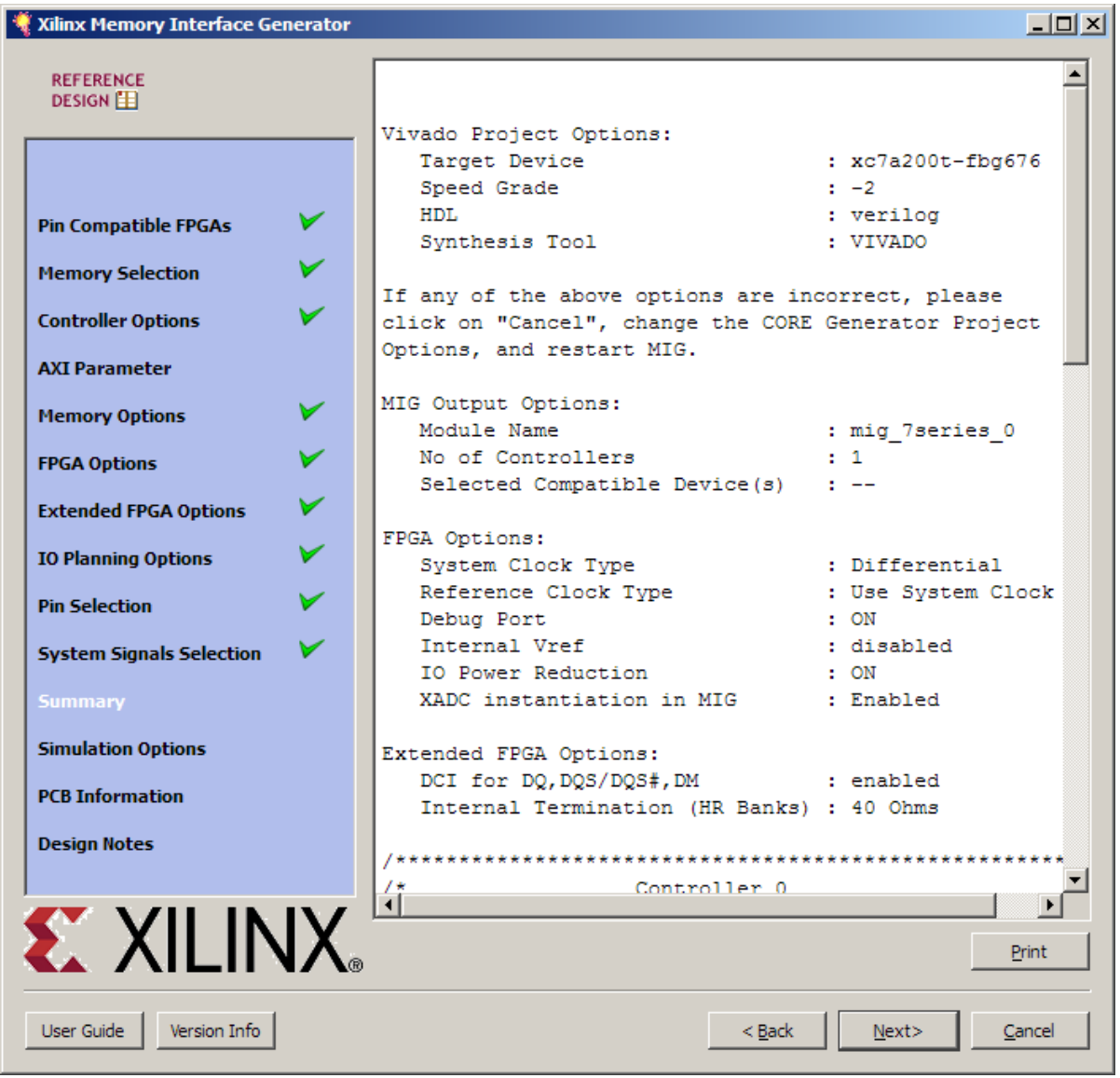
# Generate MIG Example Design




- Set sys_clk_p/n to R3/P3(CC_P/N)
  - Click Next

**Note:** Presentation applies to the AC701

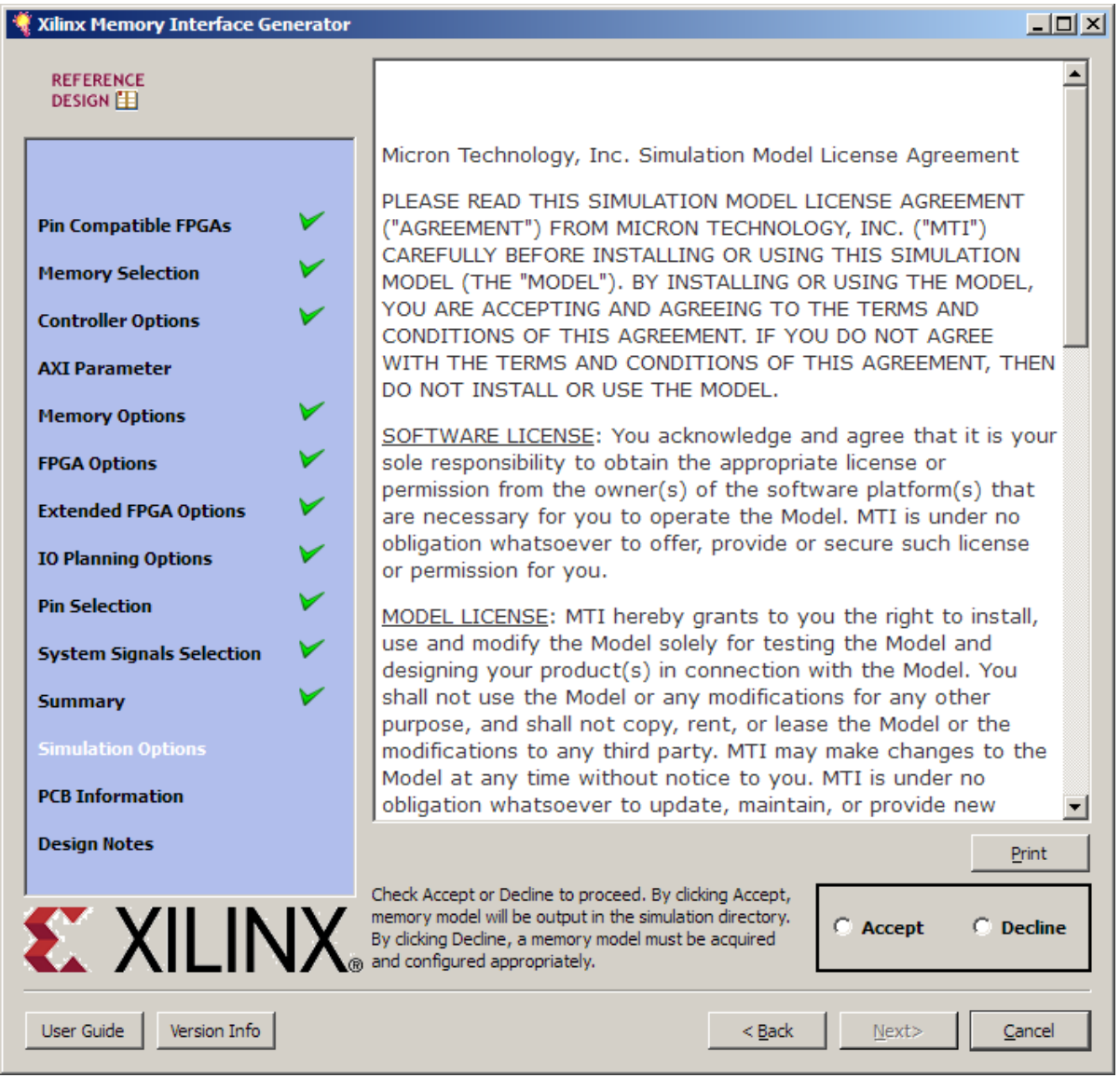
# Generate MIG Example Design




- Leave this page as is
  - Click Next

**Note:** Presentation applies to the AC701

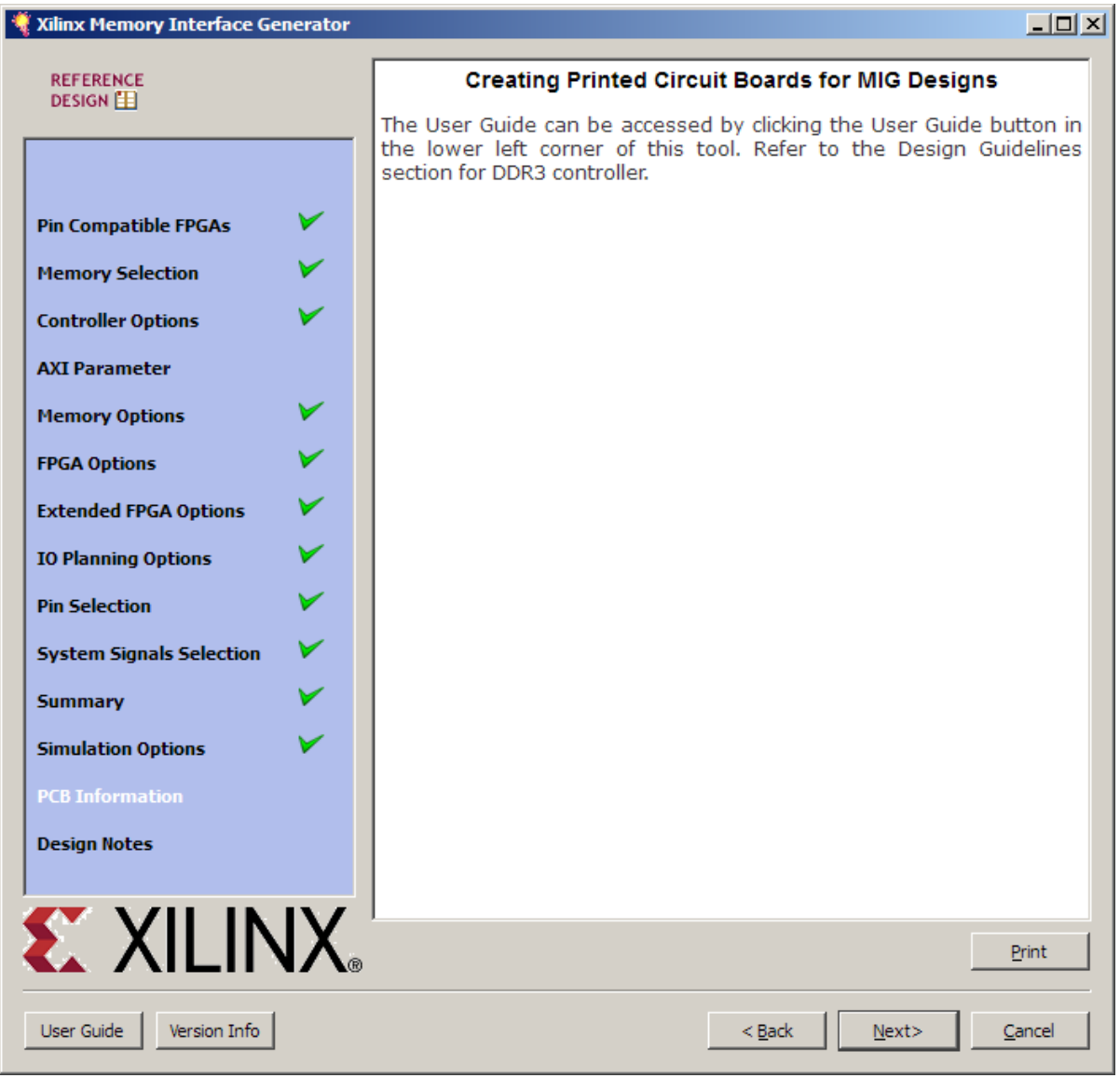
# Generate MIG Example Design




- **Accept Simulation license, if desired**
  - Otherwise, Decline license
  - Click Next

**Note:** Presentation applies to the AC701

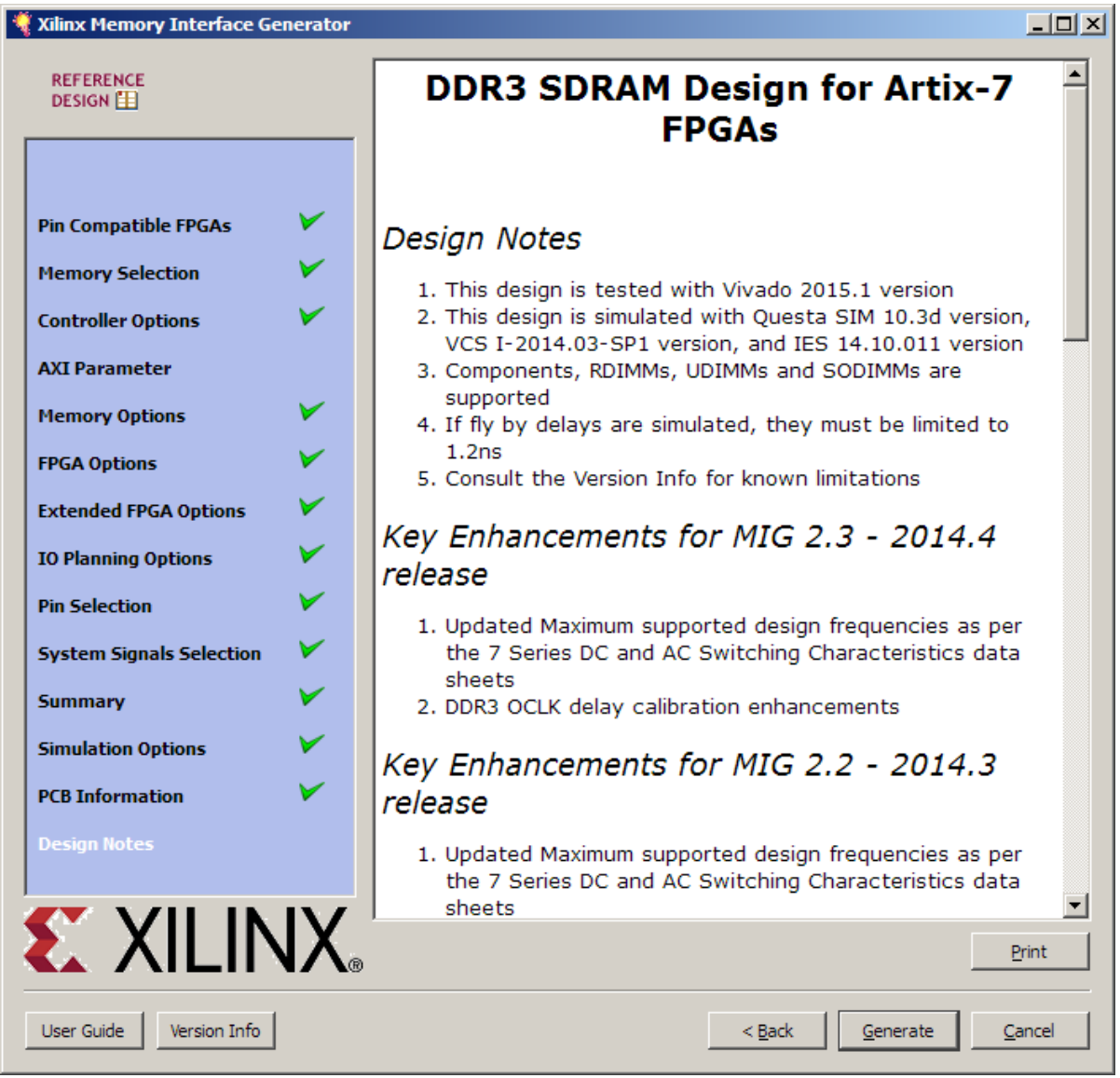
# Generate MIG Example Design




- Leave this page as is
  - Click Next

**Note:** Presentation applies to the AC701

# Generate MIG Example Design

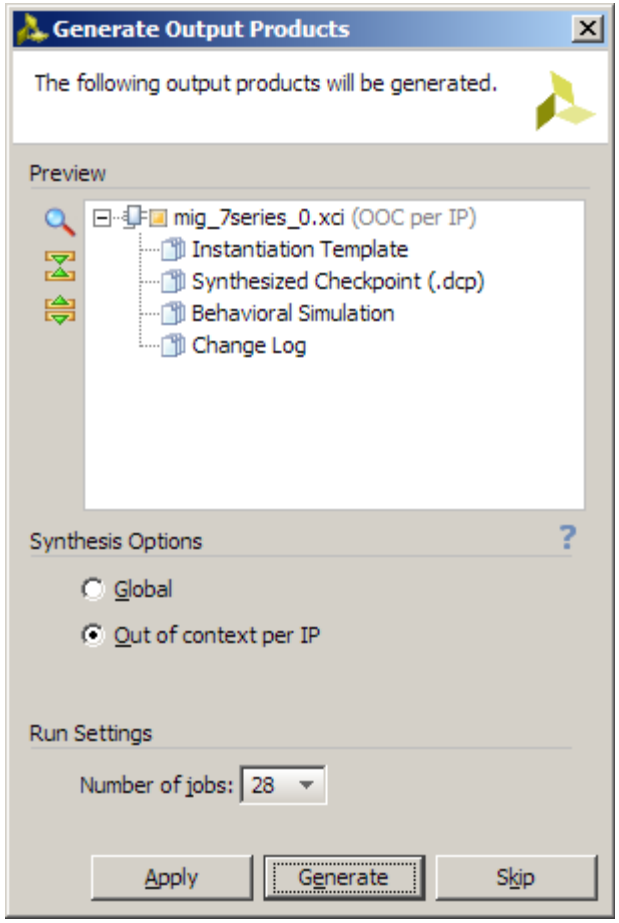



- Click Generate

**Note:** Presentation applies to the AC701

# Generate MIG Example Design

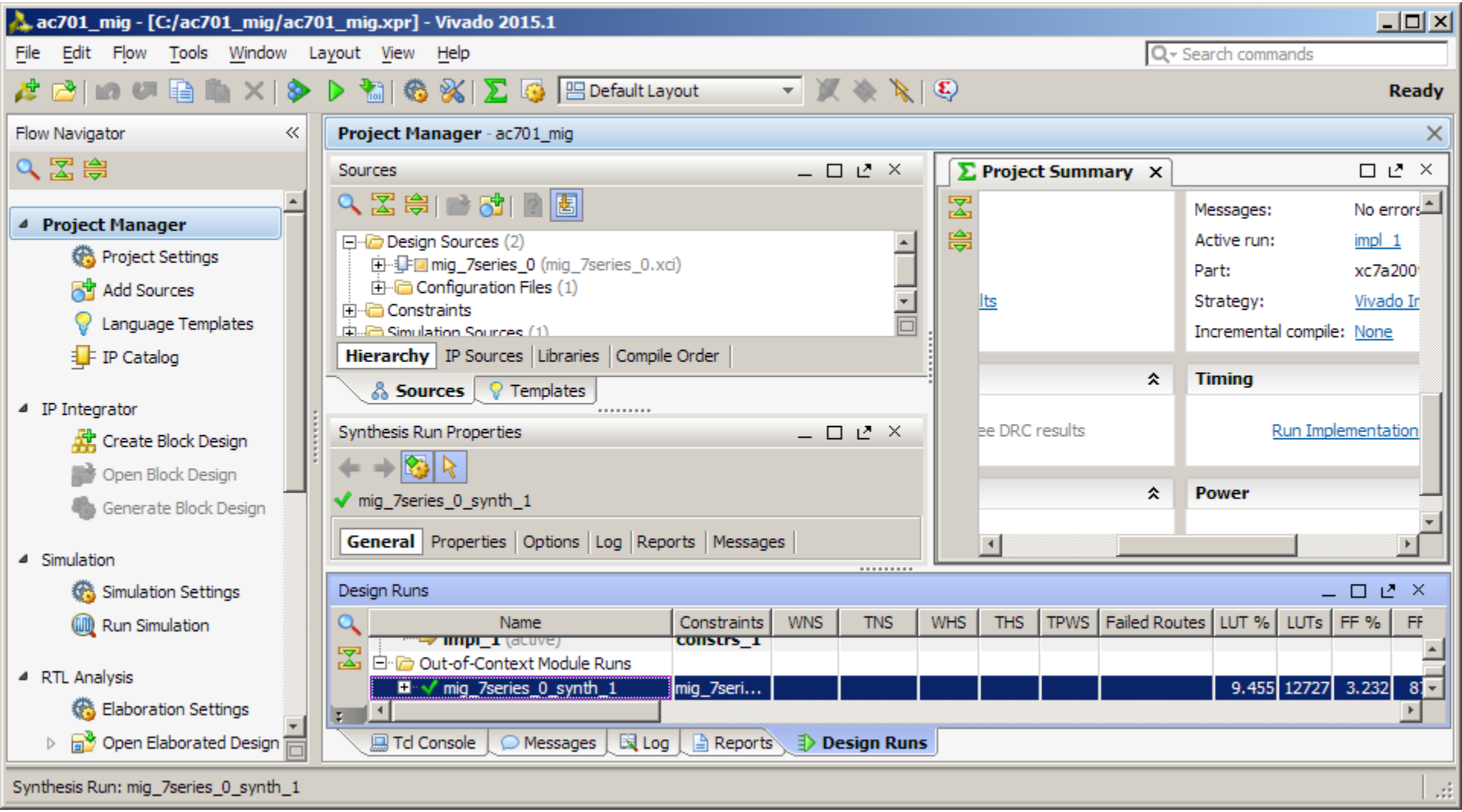
- Click Generate




**Note:** Presentation applies to the AC701

# Generate MIG Example Design

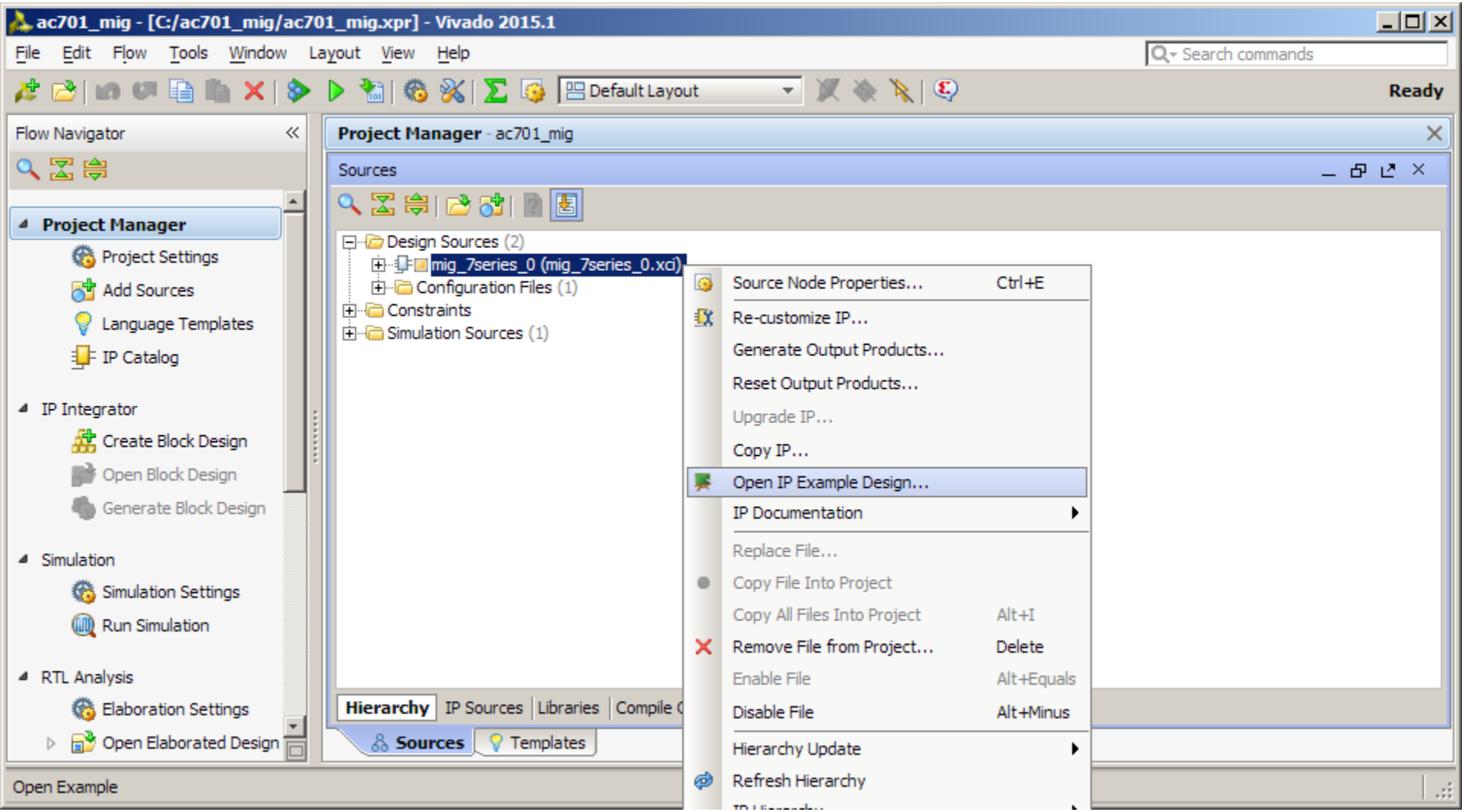
- **MIG design appears in Design Sources**
  - Wait until checkmark appears on **mig_7series_0_synth_1**




**Note:** Presentation applies to the AC701

# Compile Example Design

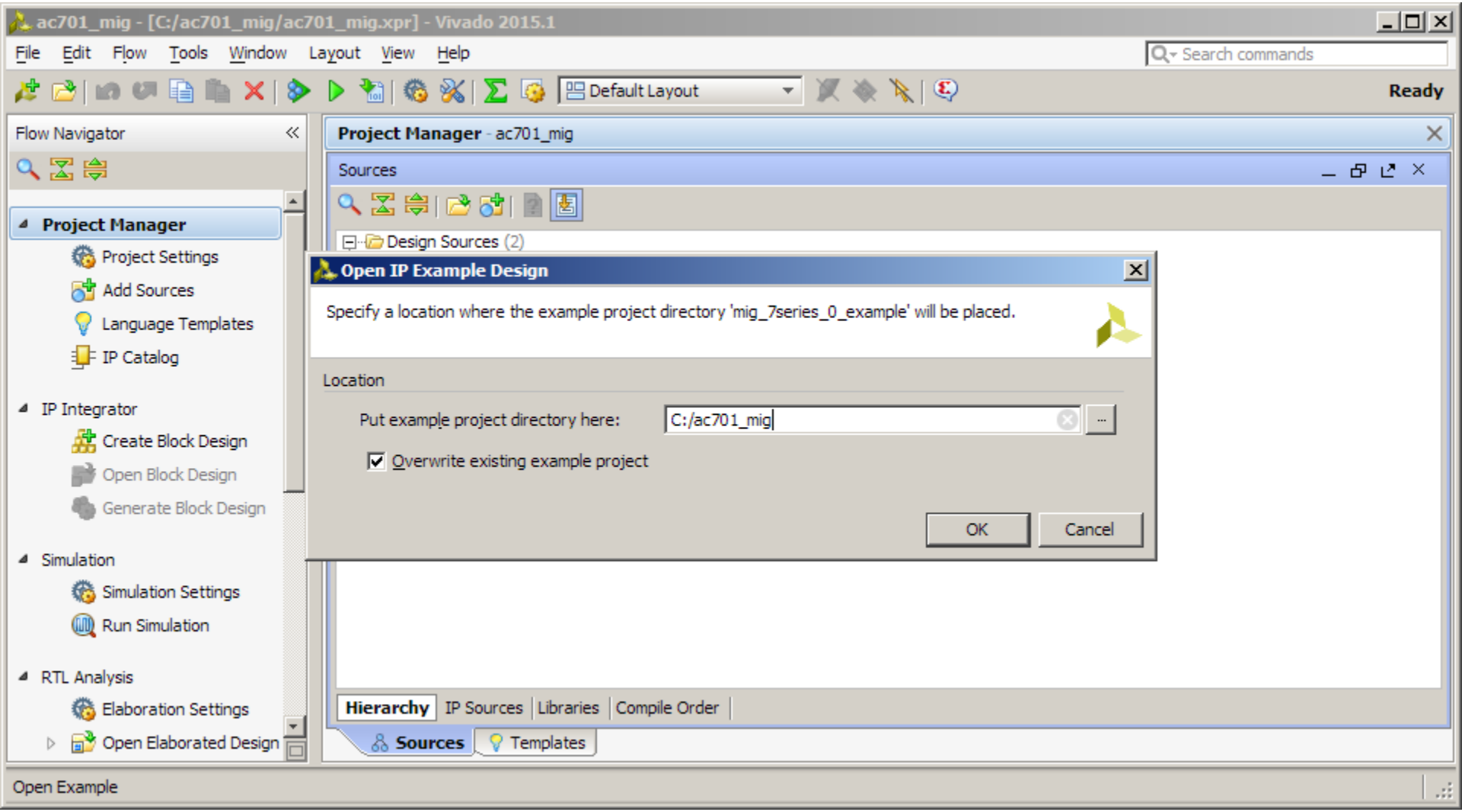
- Right click on mig_7series_0 and select Open IP Example Design…




**Note:** Presentation applies to the AC701

# Compile Example Design

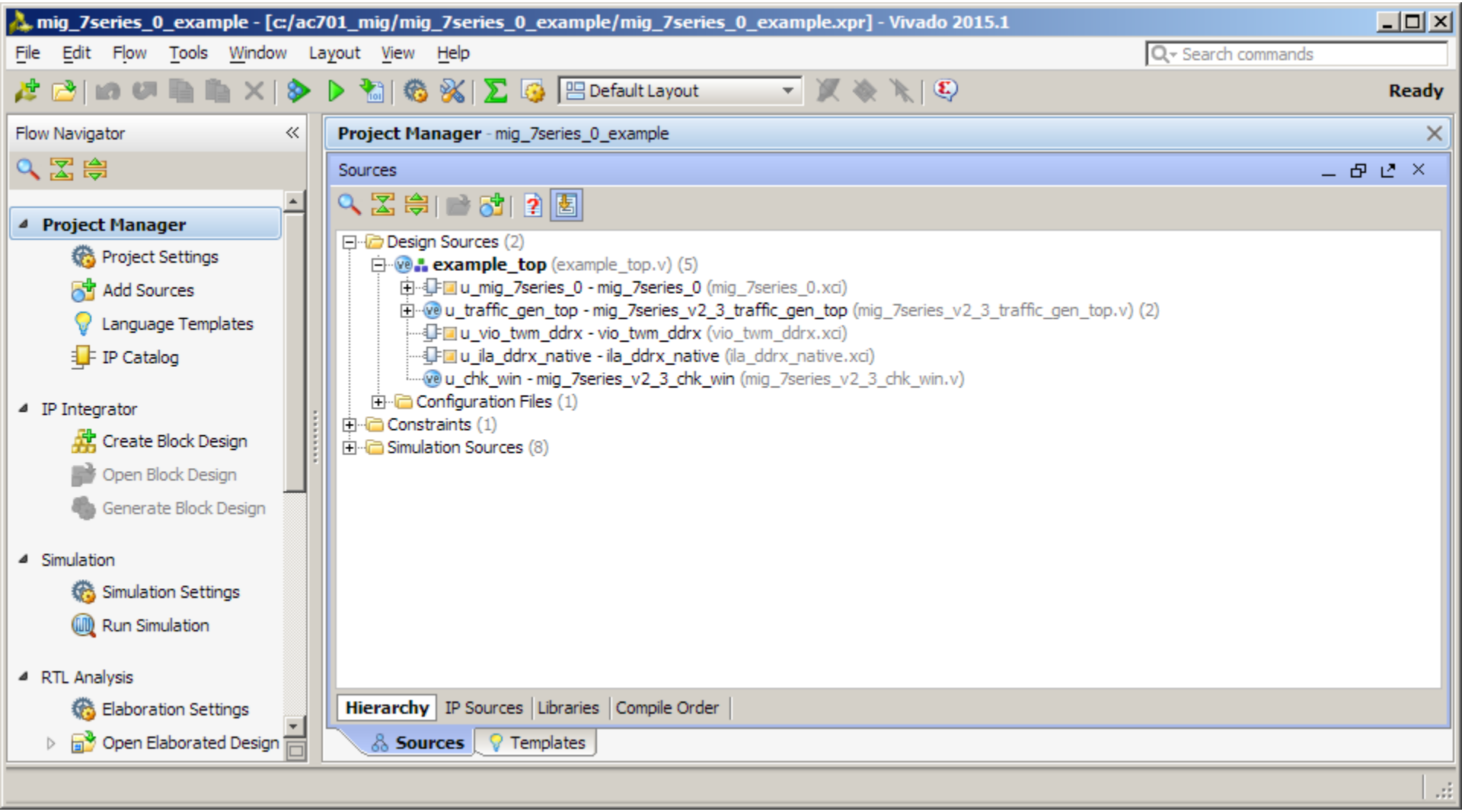
- Set the location to C:/ac701_mig and click OK




**Note:** Presentation applies to the AC701

# Compile Example Design

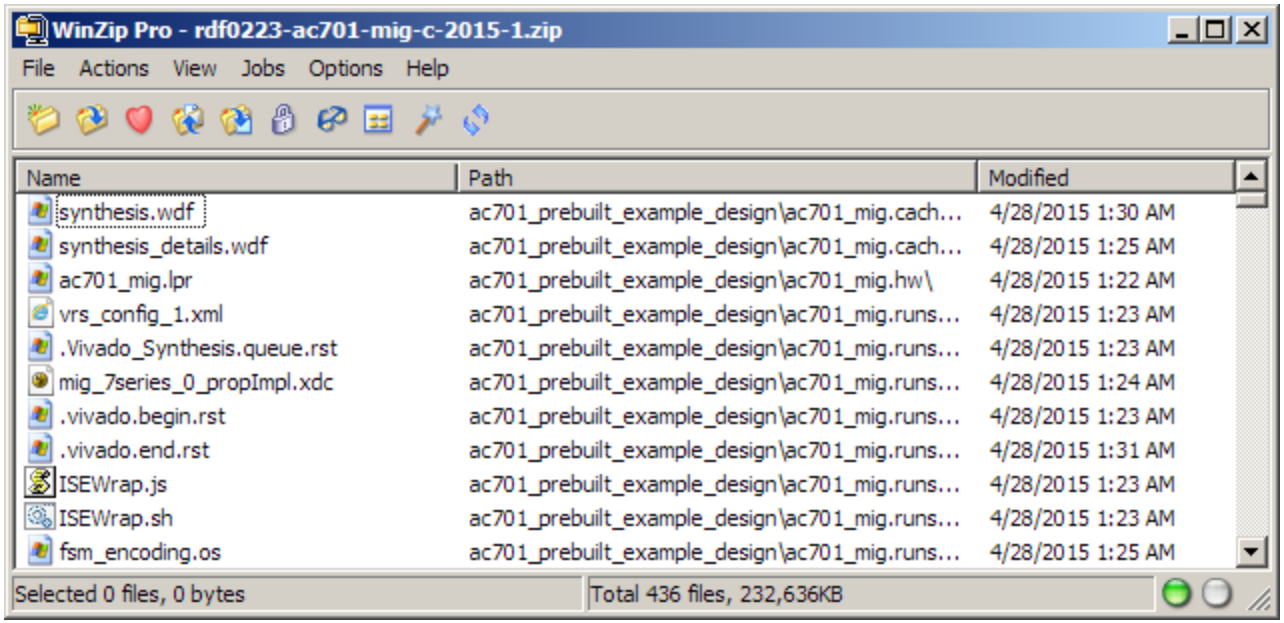
- A new project is created




**Note:** The original project window can be closed

# Modifications to Example Design

- **Unzip the AC701 MIG Design Files (2015.1 C) ZIP file to your C:\ac701_mig directory**
  - Contains several changes needed to support Artix-7 devices with MIG
  - Do this **after** creating the Example Design; changes only affect the Example Design




**Note:** Presentation applies to the AC701

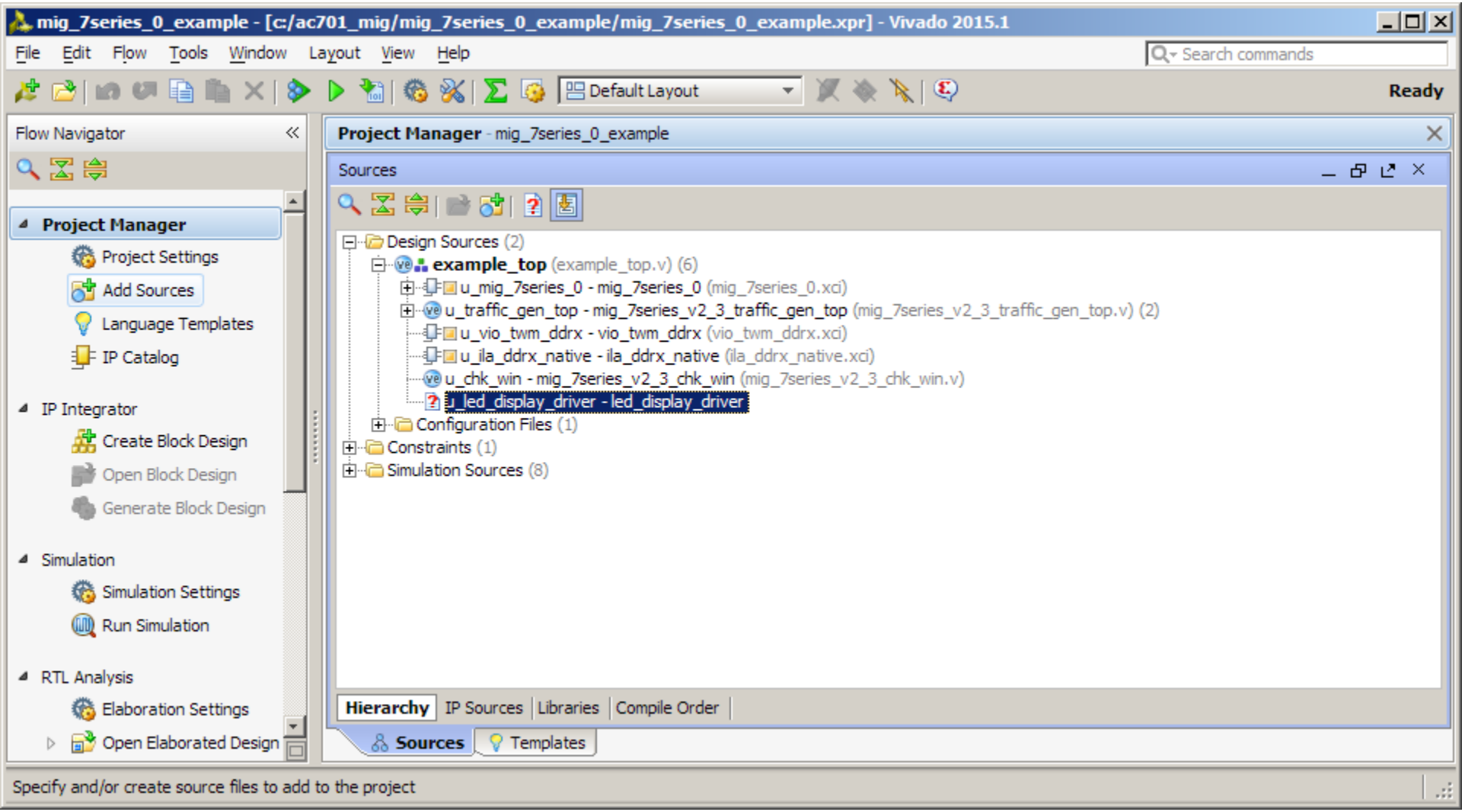
# Modifications to Example Design

- **Modifications to the example design**
  - Added RTL and XDC modifications to drive LEDs

**Note:** Presentation applies to the AC701

# Modifications to Example Design

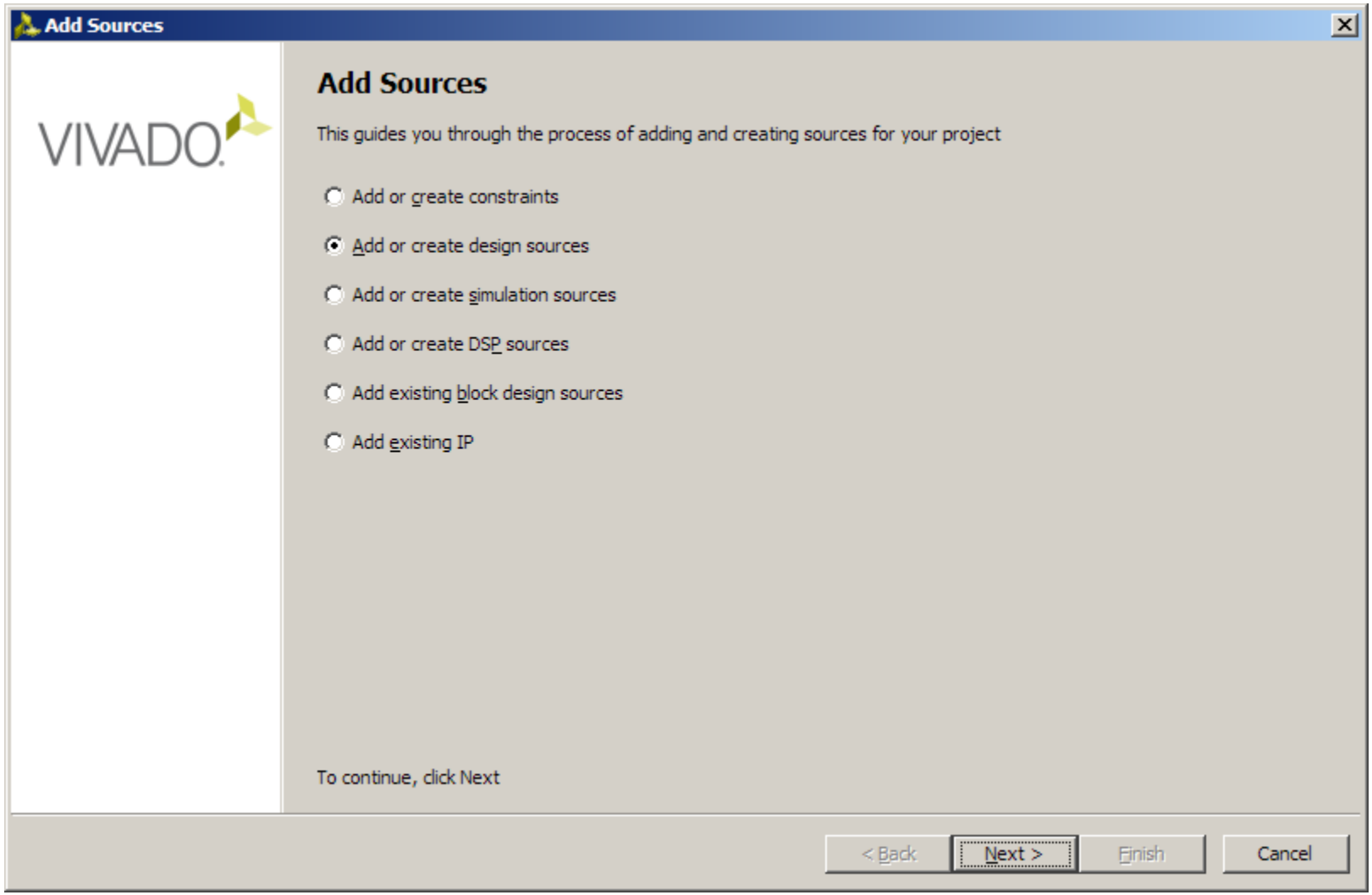
- The LED Display driver RTL file needs to be added manually
- Click on Add Sources




**Note:** Presentation applies to the AC701

# Modifications to Example Design

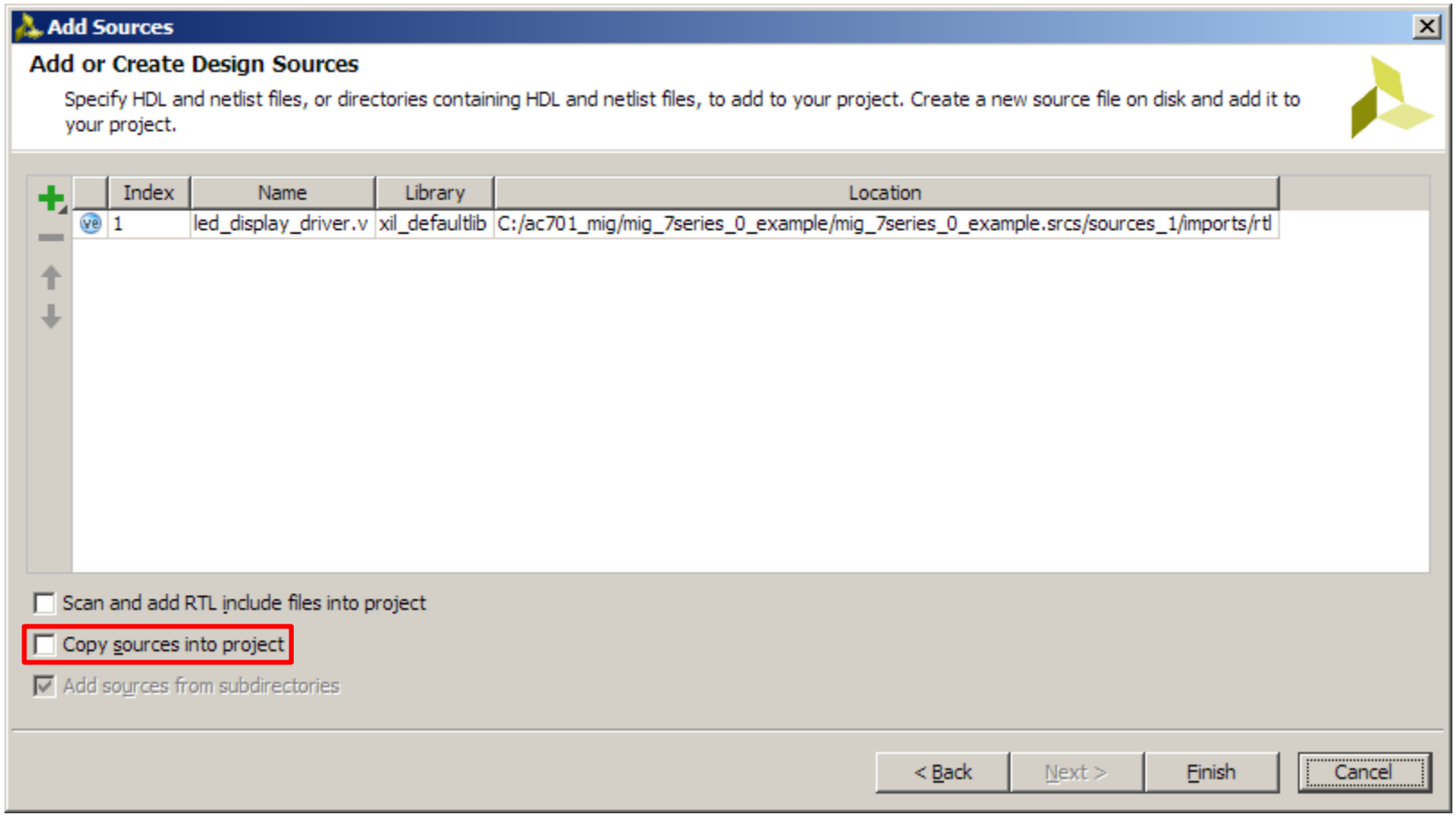
- Select Add or Create Design Sources and click Next




**Note:** Presentation applies to the AC701

# Modifications to Example Design

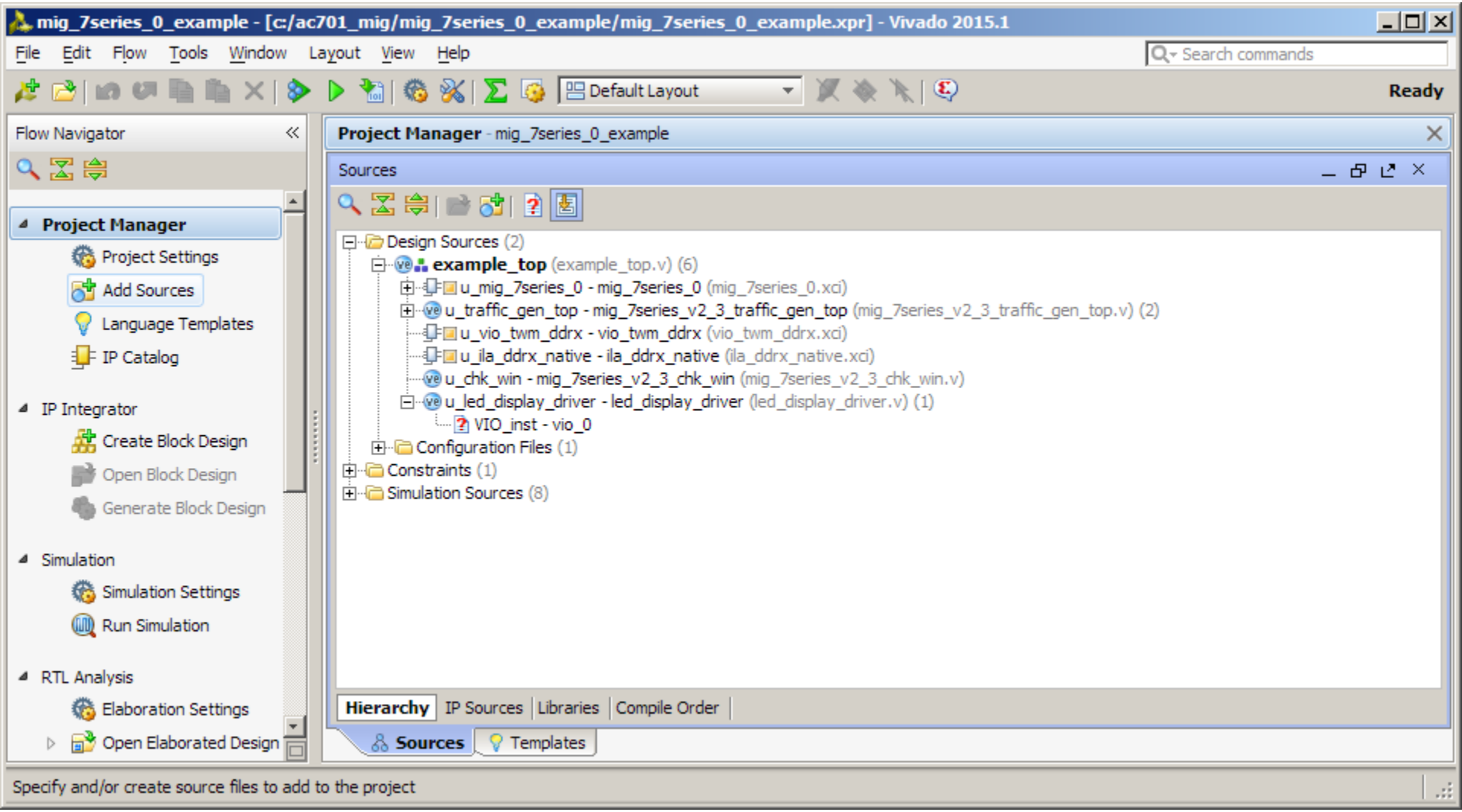
- Add led_display_driver.v from the example project
- Make sure Copy sources into project is deselected
- Click Finish




**Note:** Presentation applies to the AC701

# Compile Example Design

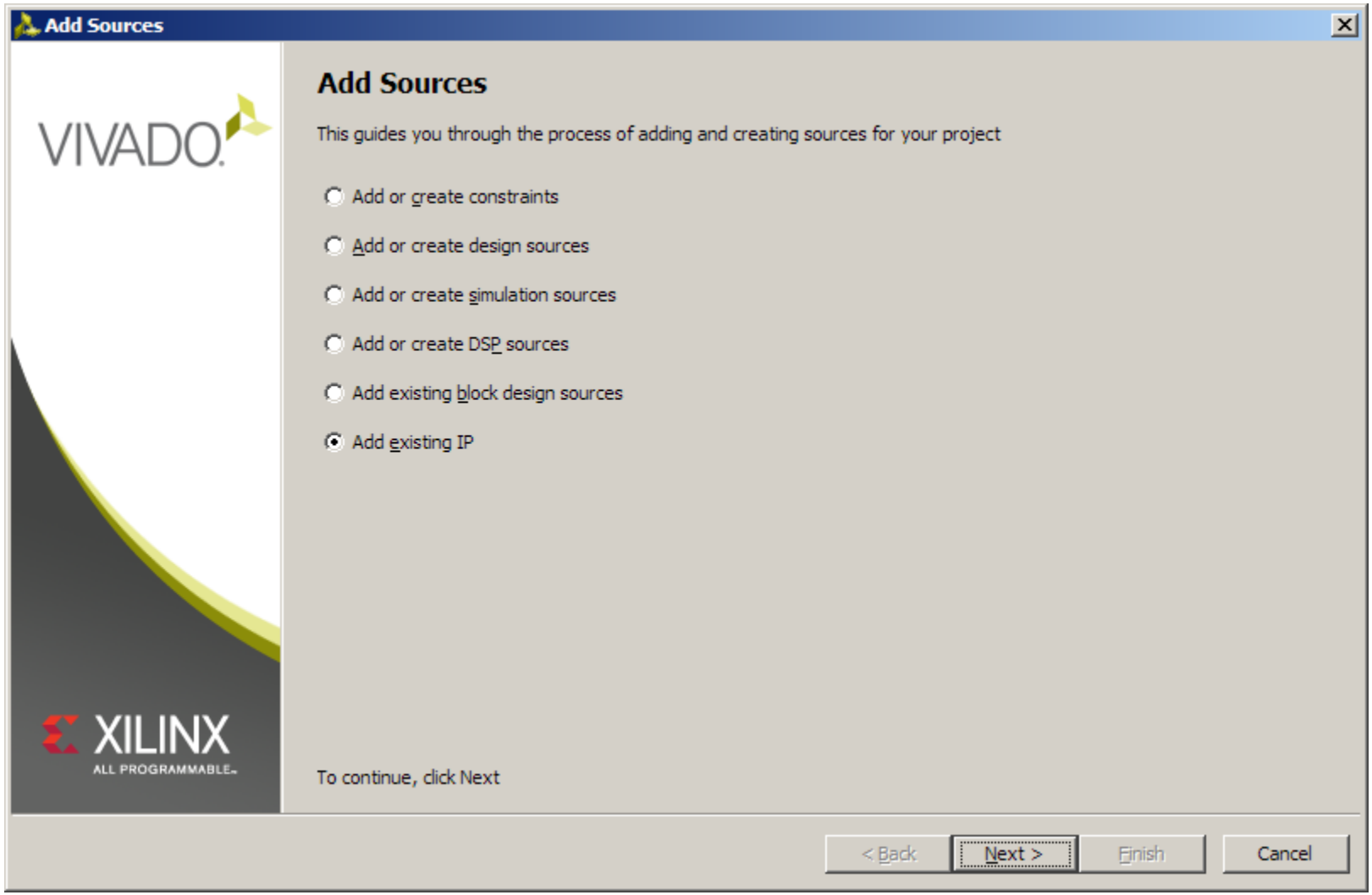
- Click on Add Sources




**Note:** Presentation applies to the AC701

# Modifications to Example Design

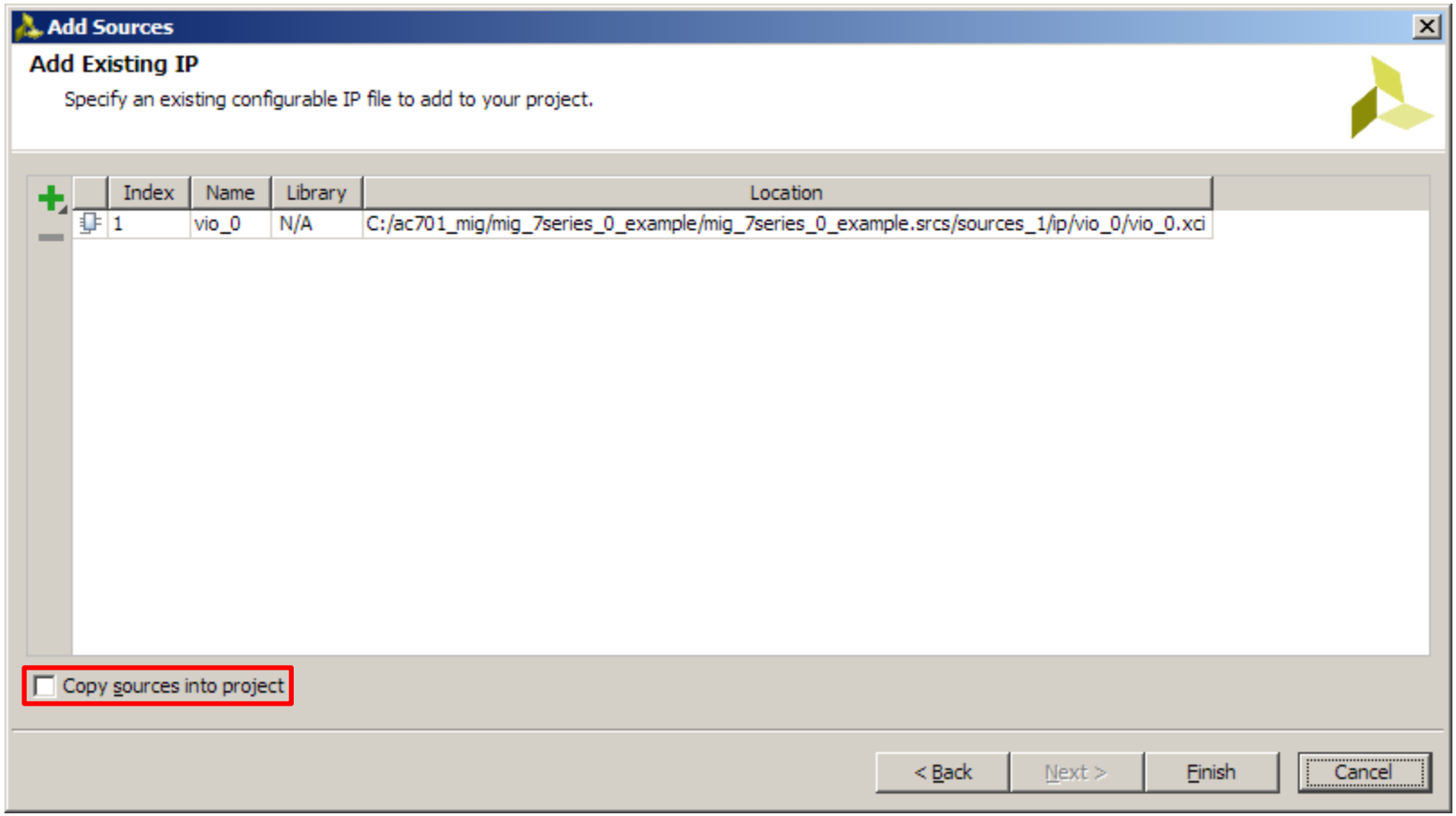
- Select Add Existing IP and click Next




**Note:** Presentation applies to the AC701

# Modifications to Example Design

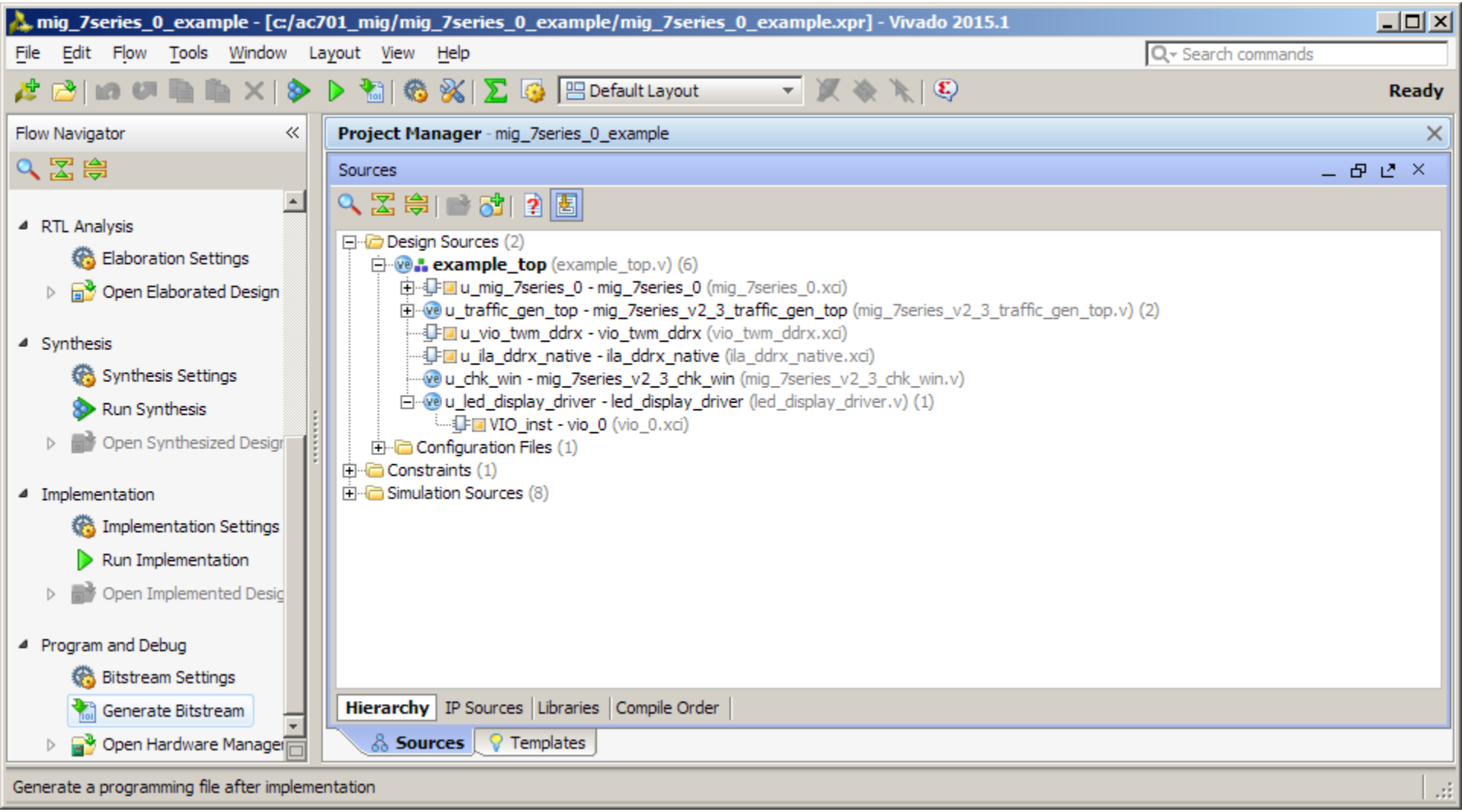
- Add vio_0.xci from the example project
- Make sure Copy sources into project is deselected
- Click Finish




**Note:** Presentation applies to the AC701

# Compile Example Design

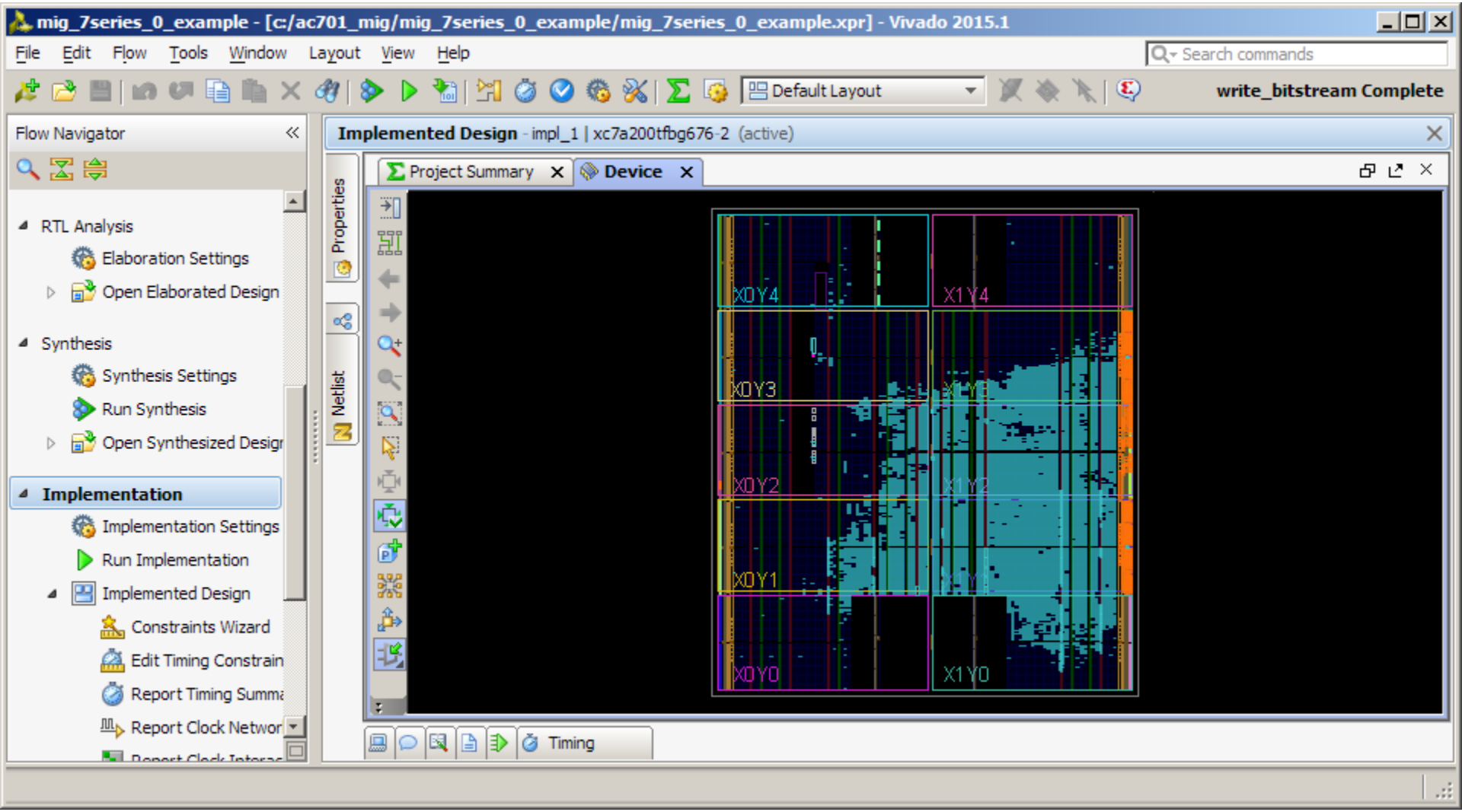
- Click on Generate Bitstream




**Note:** Presentation applies to the AC701

# Compile Example Design

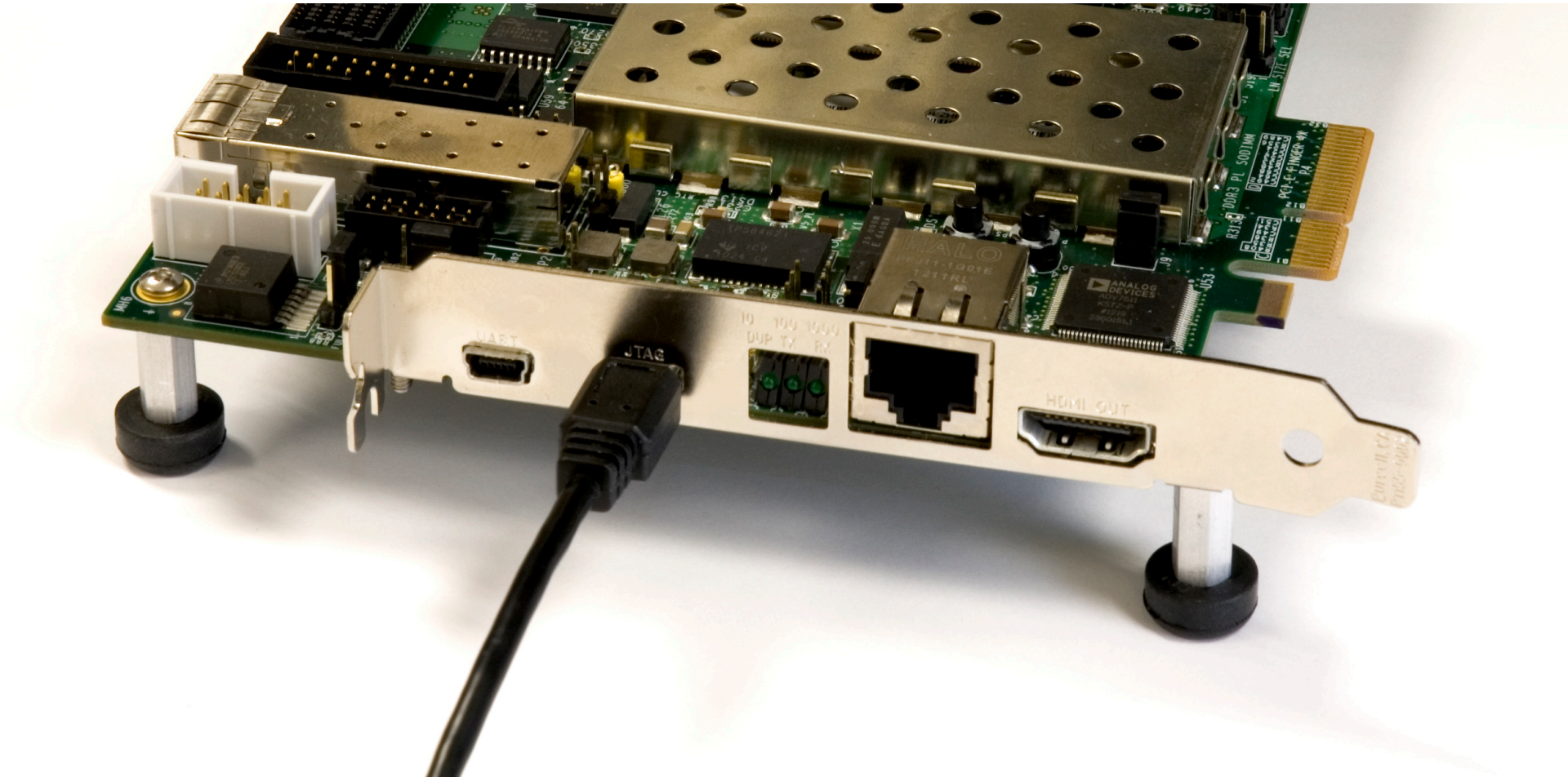
- Open and view the Implemented Design




**Note:** Presentation applies to the AC701

# AC701 Setup

- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the AC701 board**
  - Connect this cable to your PC
  - Power on the AC701 board

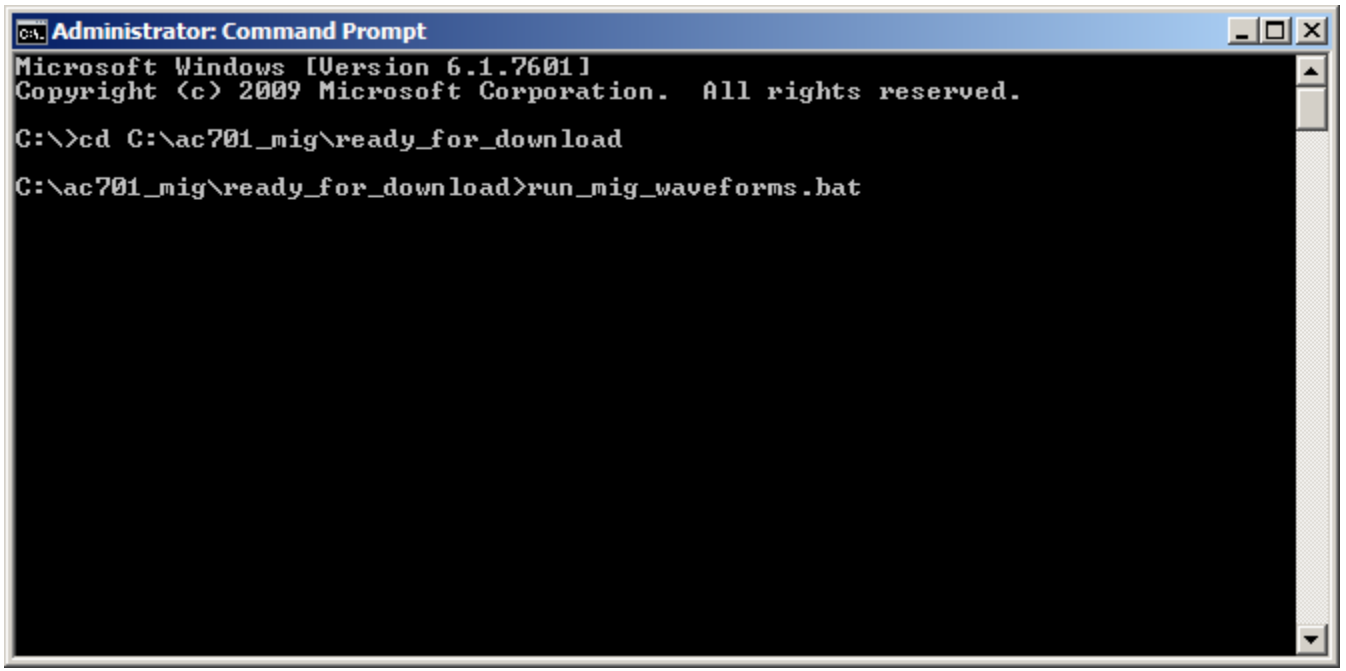


# Run MIG Example Design

- From a Command Prompt, type:

  **cd C:\ac701_mig\ready_for_download**

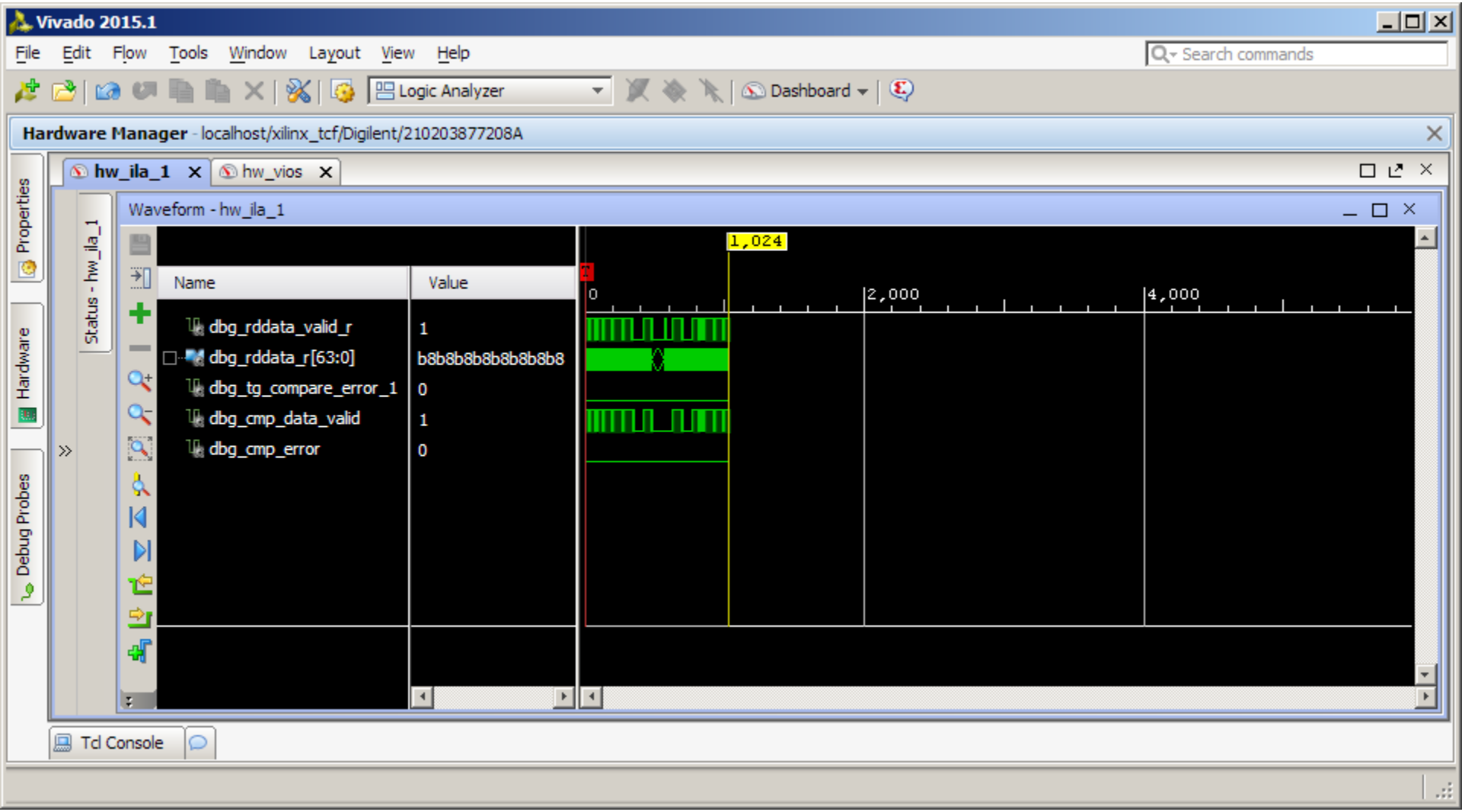
  **run_mig_waveforms.bat**




**Note:** Presentation applies to the AC701

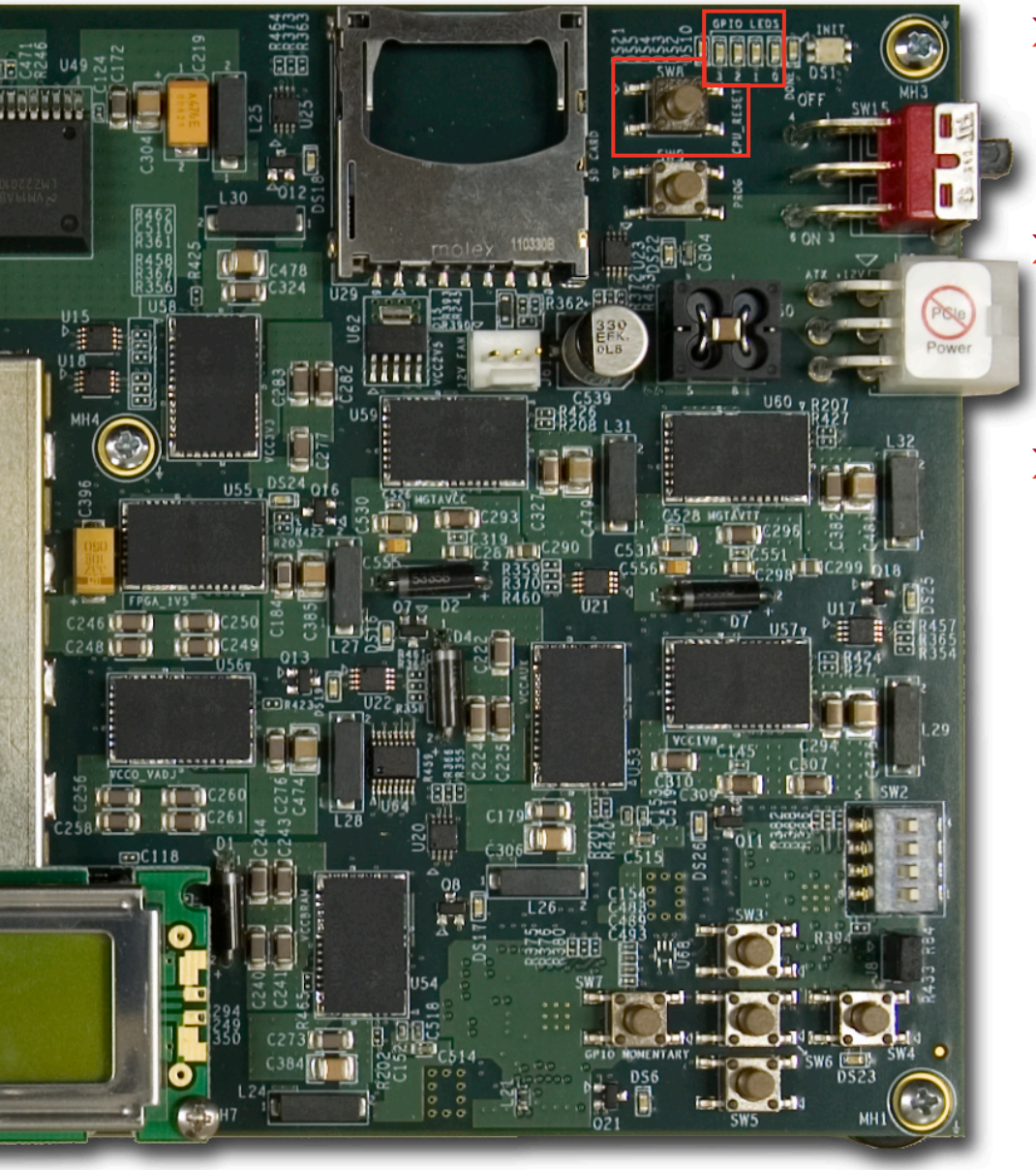
# Run MIG Example Design

- Under Tcl script control, Vivado opens, loads the bitstream and generates a MIG waveform




**Note:** Presentation applies to the AC701

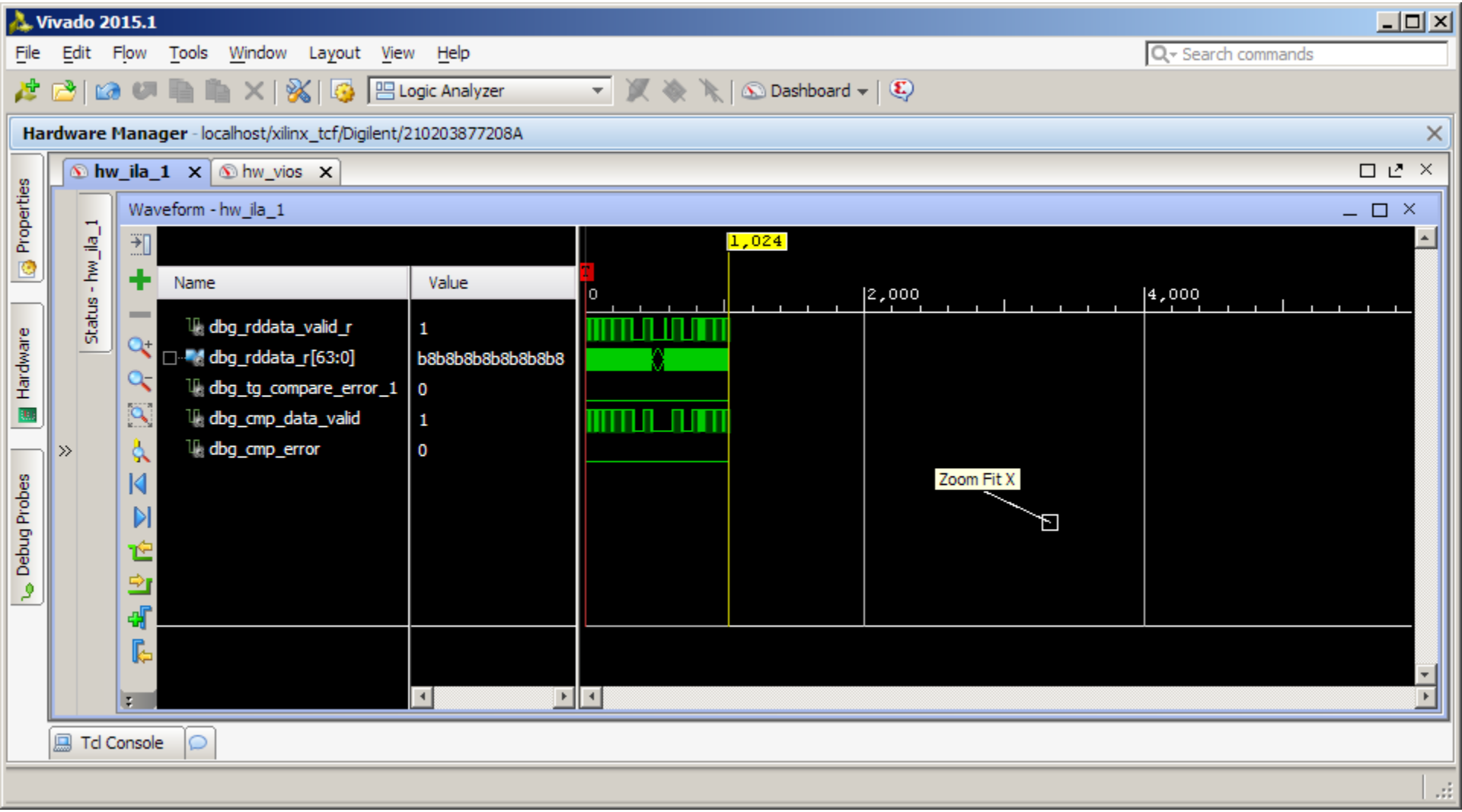
# Run MIG Example Design




- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - CPU_RESET, SW8, is the reset

# Run MIG Example Design

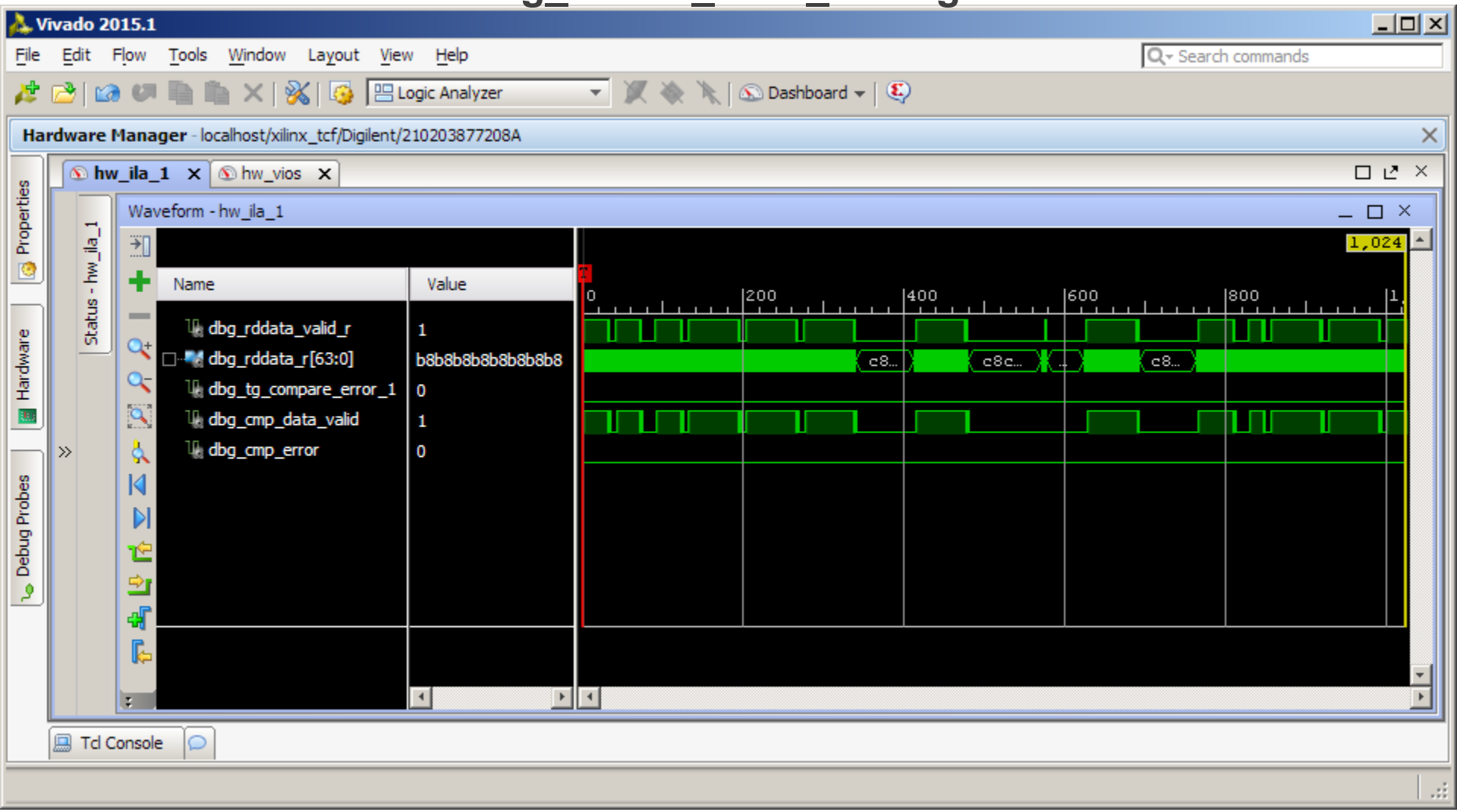
- Click and drag to the left to expand the waveform




**Note:** Presentation applies to the AC701

# Run MIG Example Design

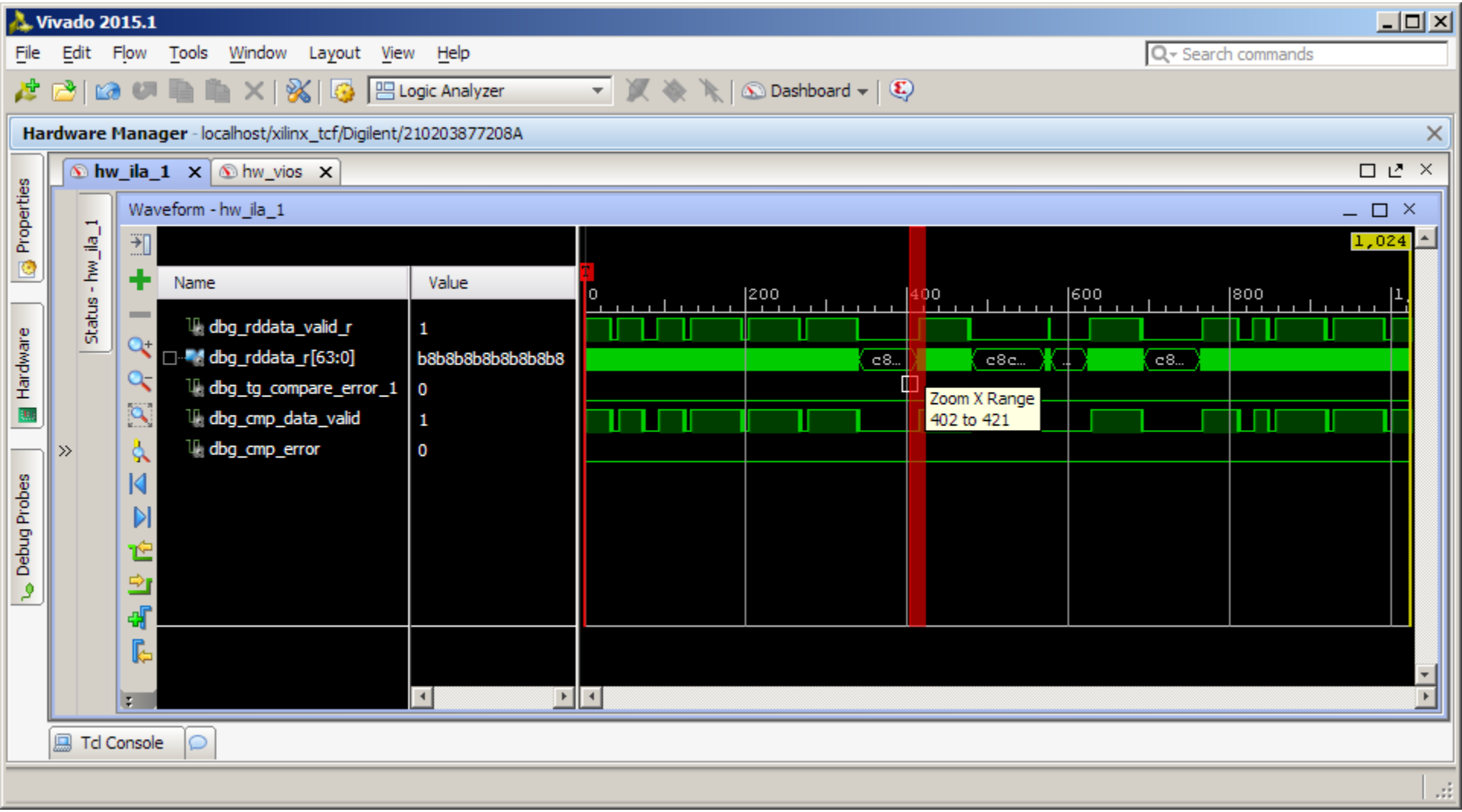
- View waveforms
- Data is valid when dbg_rddata_valid_r is high




**Note:** Presentation applies to the AC701

# Run MIG Example Design

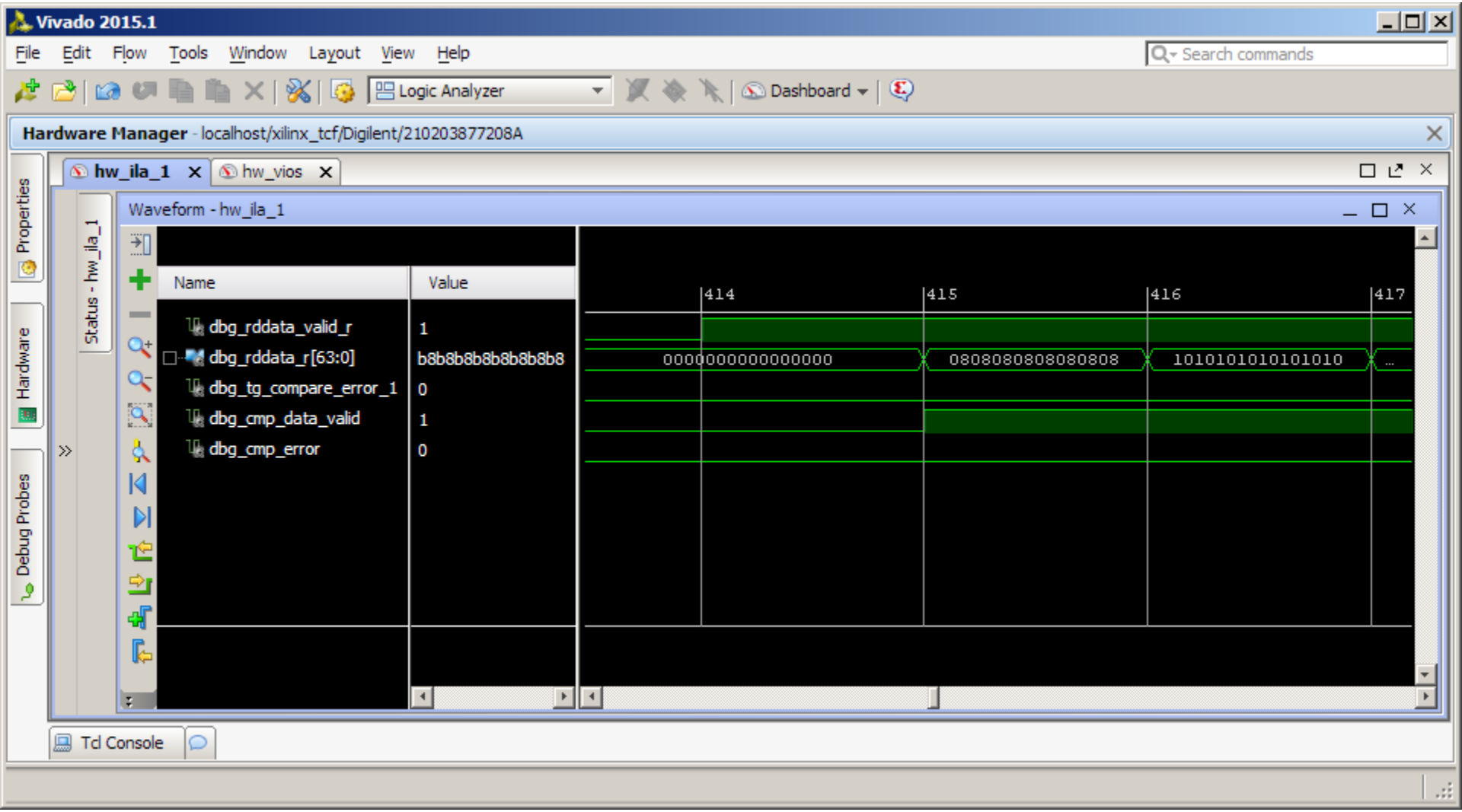
- Click and drag to the right to zoom in




**Note:** Presentation applies to the AC701

# Run MIG Example Design

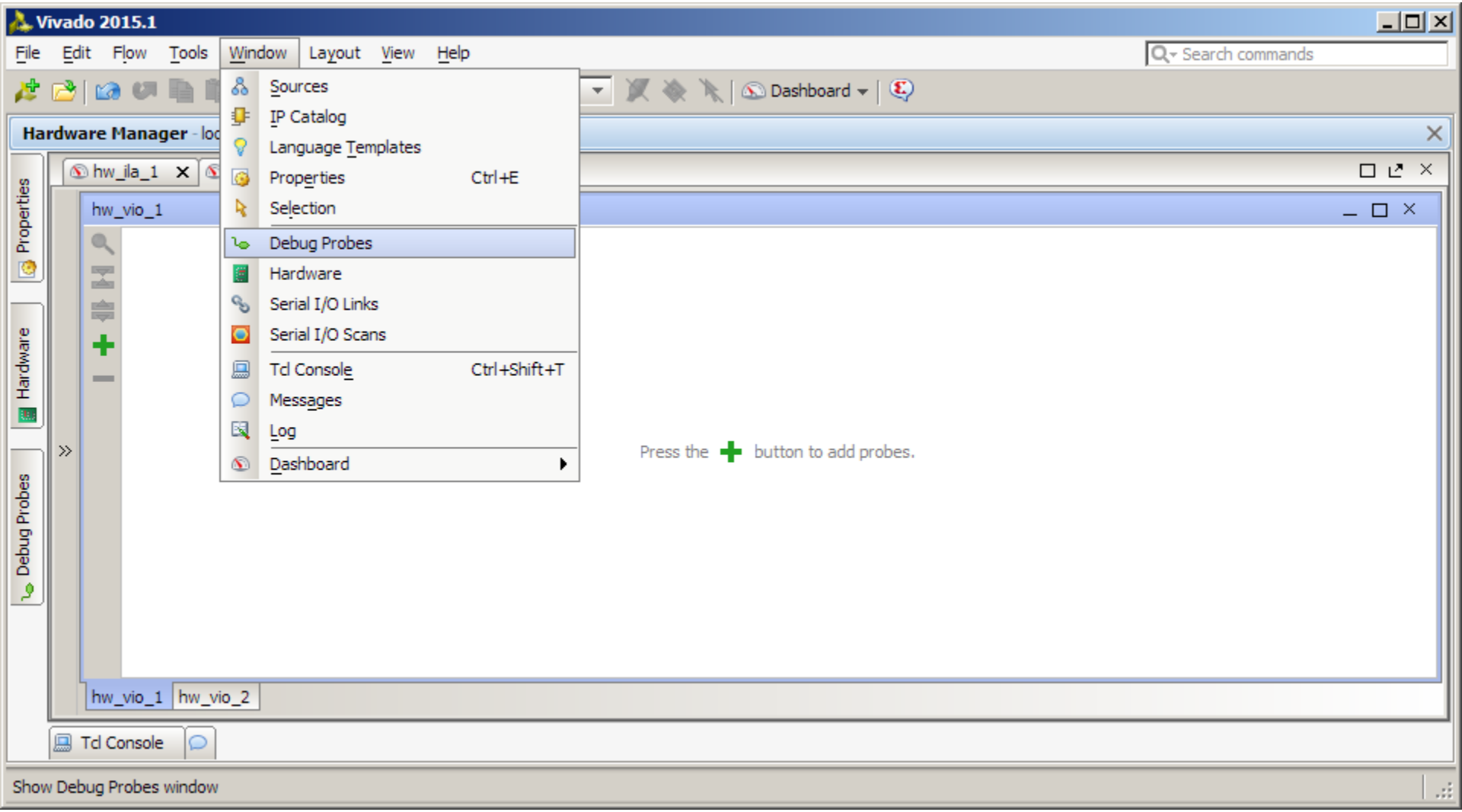
- View waveform details




**Note:** Presentation applies to the AC701

# Adjust Data Pattern using VIO Console

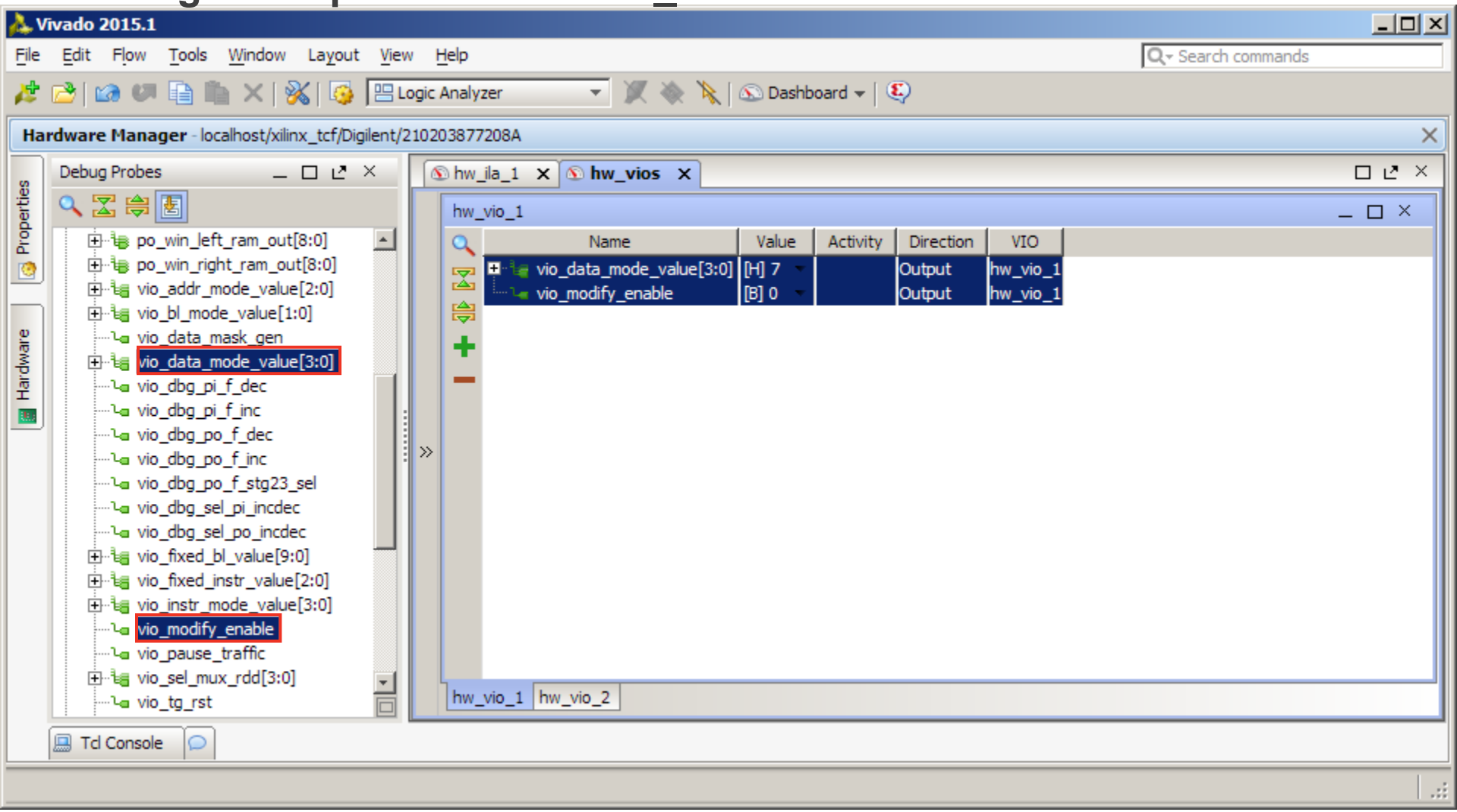
- Select the hw_vios tab and open the Debug Probes




**Note:** Presentation applies to the AC701

# Adjust Data Pattern using VIO Console

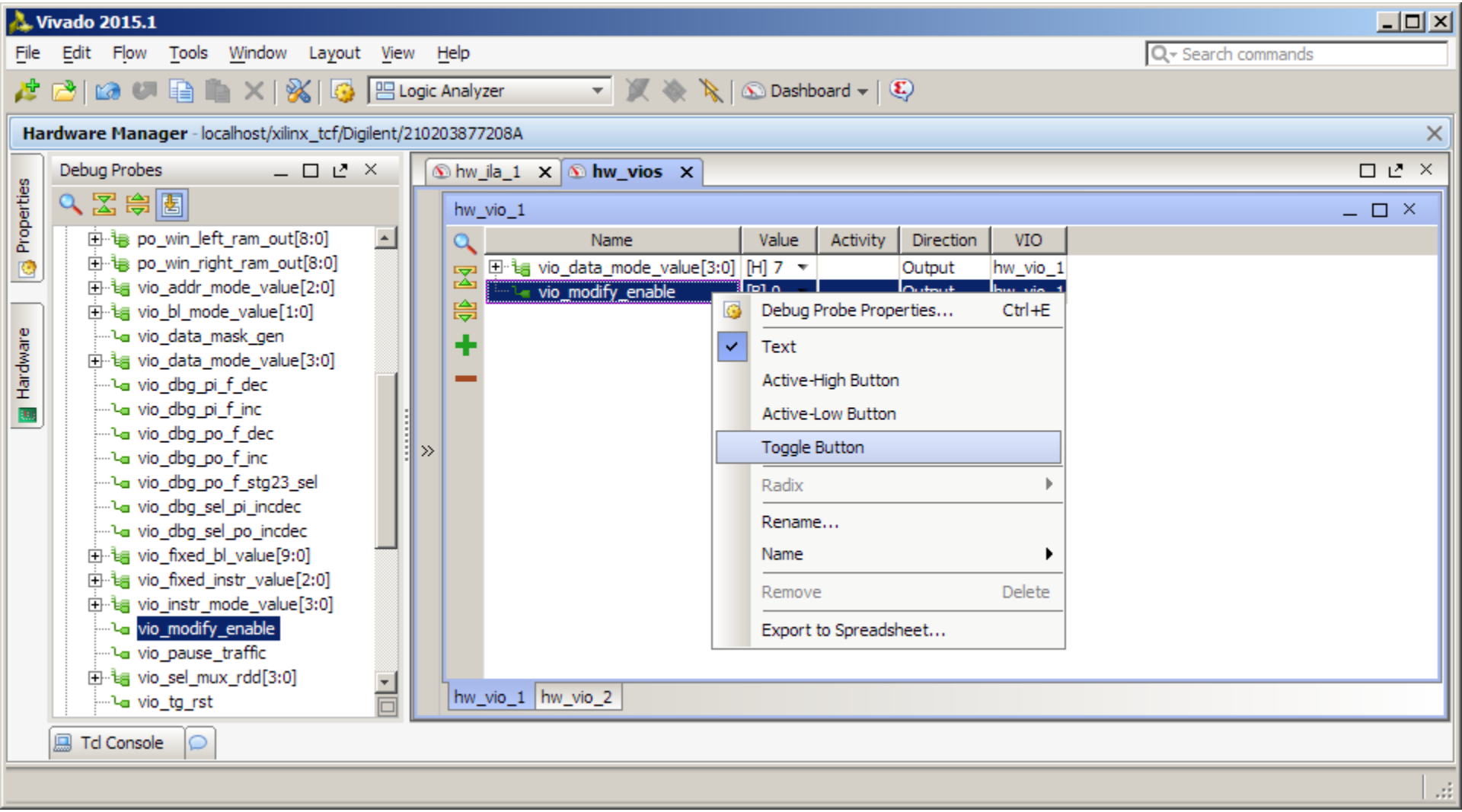
- Select the vio_data_mode_value and vio_modify_enable probes
- Drag these probes to the hw_vios tab




**Note:** Presentation applies to the AC701

# Adjust Data Pattern using VIO Console

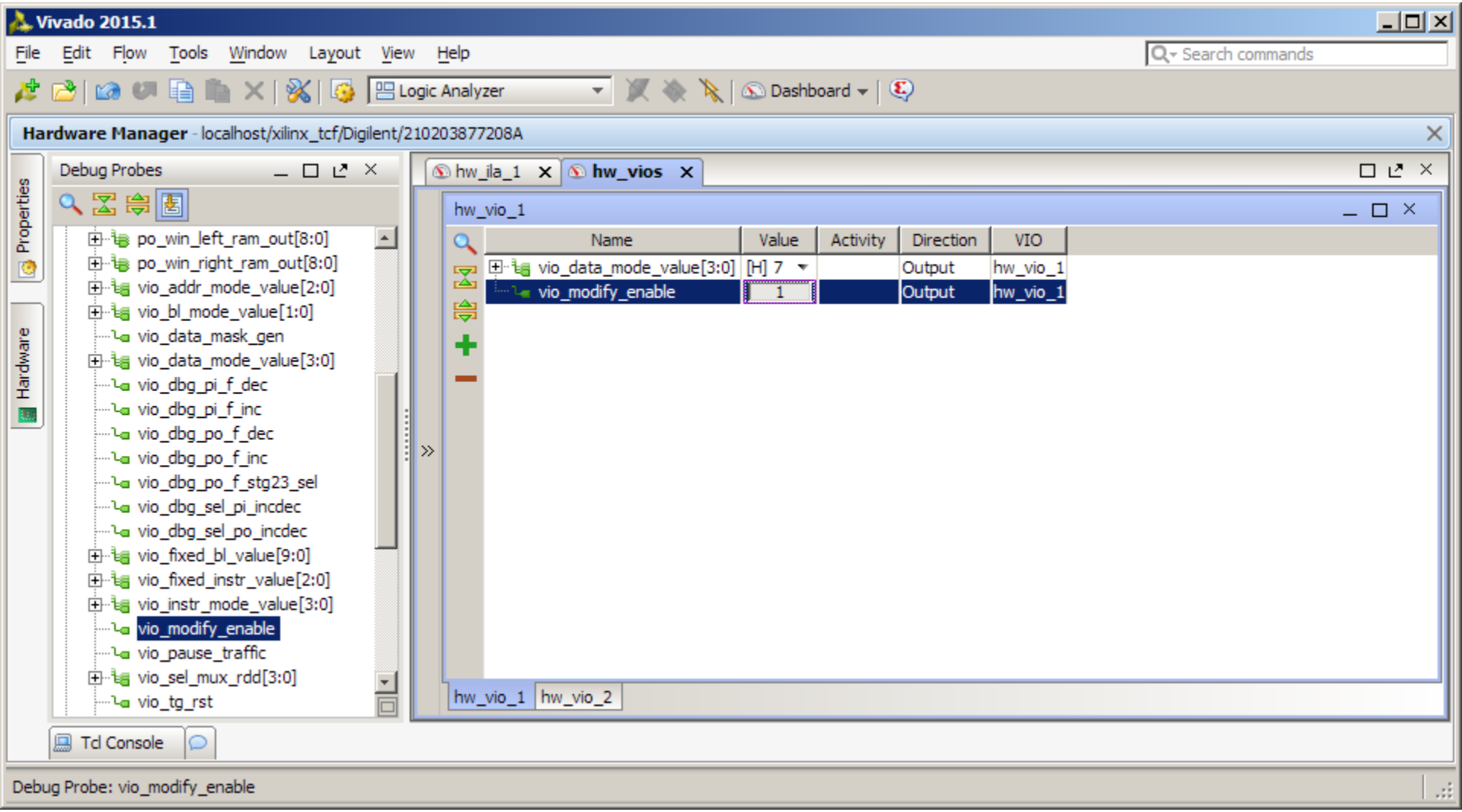
- Right click on vio_modify_enable and set to Toggle Button




**Note:** Presentation applies to the AC701

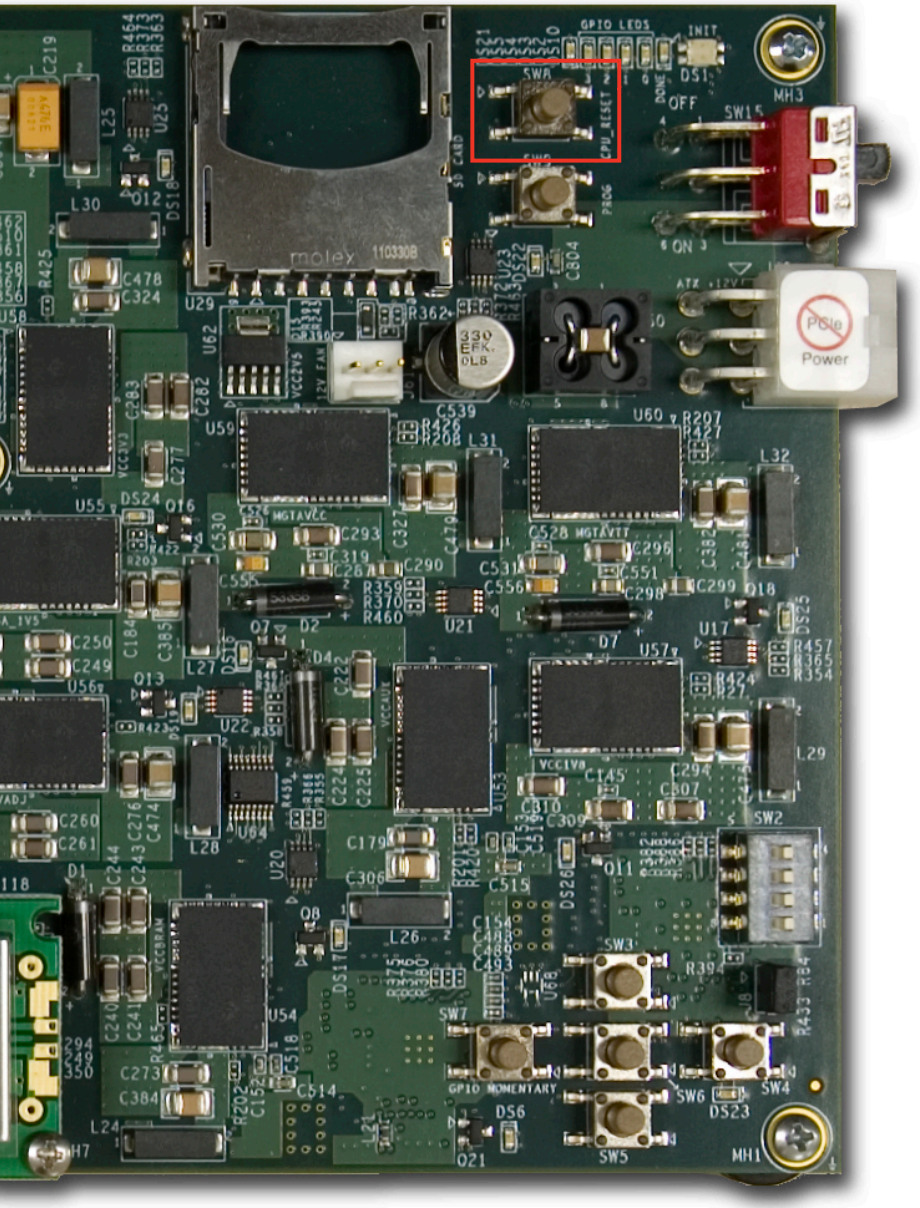
# Adjust Data Pattern using VIO Console

- Toggle the vio_modify_enable button to “1”




**Note:** Presentation applies to the AC701

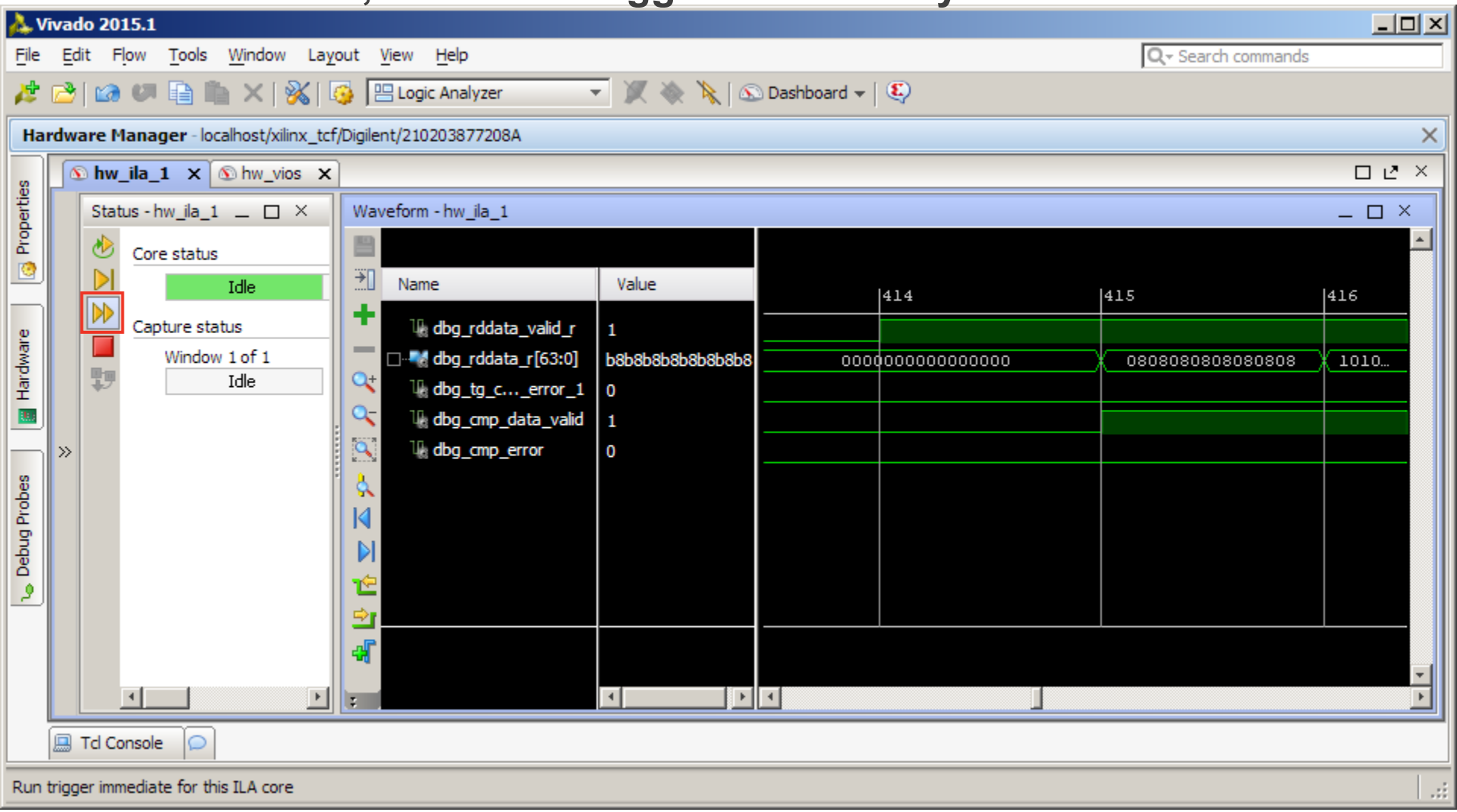
# Run MIG Example Design




- Press and release the CPU RESET switch, SW8, after each change to vio_modify_enable or vio_data_mode_value

# Adjust Data Pattern using VIO Console

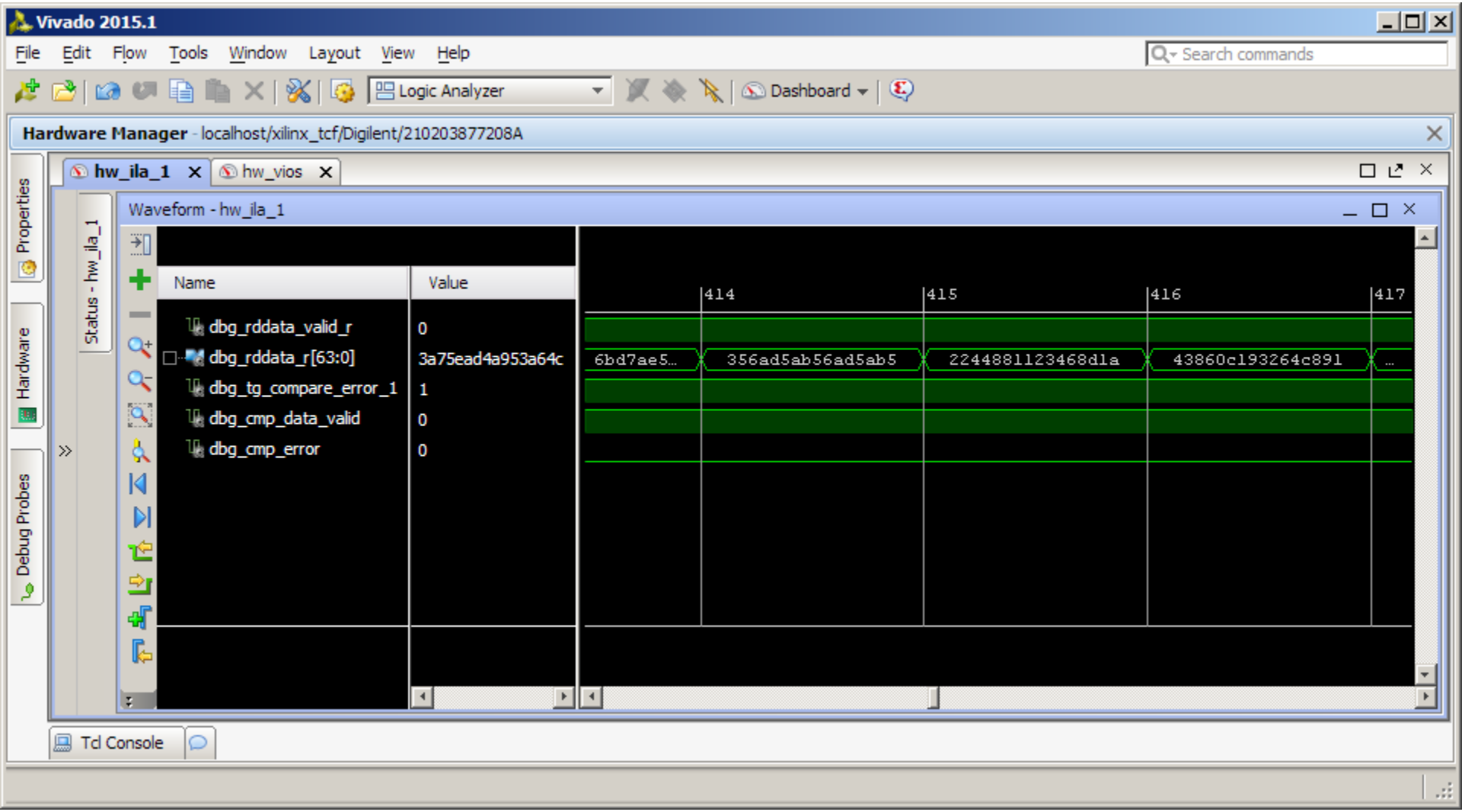
- Select the hw_ila_1 tab
- Under Status, click Run Trigger Immediately




**Note:** Presentation applies to the AC701

# Adjust Data Pattern using VIO Console

- View PRBS data




**Note:** Presentation applies to the AC701

# References

# References

- **Artix-7 Memory**
  - 7 Series FPGAs Memory Interface Solutions User Guide – UG586
    - http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v2_3/ug586_7Series_MIS.pdf
  - MIG 7 Series – Release Notes
    - http://www.xilinx.com/support/answers/54025.htm
- **Vivado Programming and Debugging**
  - Vivado Design Suite Programming and Debugging User Guide – UG908
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf

# Documentation

# Documentation

- **Artix-7**
  - Artix-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm
  - Design Advisory Master Answer Record for Artix-7 FPGAs
    - http://www.xilinx.com/support/answers/51456.htm
- **AC701 Documentation**
  - Artix-7 FPGA AC701 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html
  - AC701 Getting Started Guide – UG967
    - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/2014_3/ug967-ac701-eval-kit-getting-started.pdf
  - AC701 User Guide – UG952
    - http://www.xilinx.com/support/documentation/boards_and_kits/ac701/ug952-ac701-a7-eval-bd.pdf